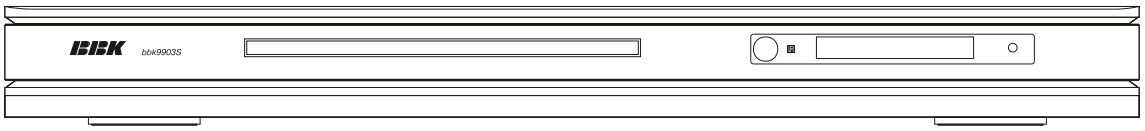
SERVICE MANUAL

bbk9903S



CONTENTS

1. SAFETY PREAUTIONS

1.1 GENERAL GUIDELINES

1. When servicing, observe the original lead dress. if a short circuit is found, replace all parts which have been overheated or damaged by the short circuit.

2. After servicing, see to it that all the protective devices such as insulation barrier, insulation papers shields are properly installed.

3. After servicing, make the following leakage current checks to prevent the customer from being exposed to shock hazards.

2.PREVENTION OF ELECTRO STATIC DISCHARGE(ESD)TO ELECTROSTATICALLY SENSITIVE(ES)DEVICES

Some semiconductor(solid state)devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive(ES)Devices. Examples of typical ES devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by electro static discharge(ESD).

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any ESD on your body by touching a known earth ground. Alternatively, obtain and wear a commercially availabel discharging ESD wrist strap, which should be removed for potential shock reasons prior to applying power to the unit under test.

2. After removing an electrical assembly equipped with ES devices,place the assembly on a conductive surface such as alminum foil, to prevent electrostatic charge buildup or exposure of the assembly.

3. Use only a grounded-tip soldering iron to solder or unsolder ES devices.

4. Use only an anti-static solder removal device. Some solder removal devices not classified as anti-static (ESD protected)can generate electrical charge sufficient to damage ES devices.

5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ES devices.

6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (Most replacement ES devices are packaged with leads electrically shorted together by conductive foam, alminum foil or comparable conductive material).

7. Immediately before removing the protective material from the leads of a replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

Caution

Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

8. Minimize bodily motions when handling unpackaged replacement ES devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity(ESD).

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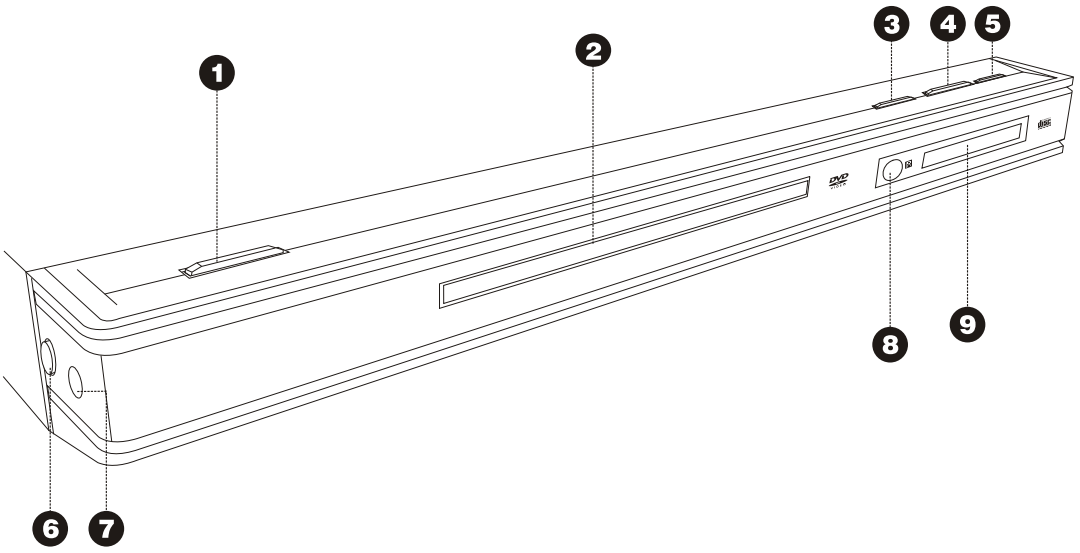
IMPORTANT SAFETY NOTICE

There are special components used in this equipment which are imporant for safety.
These parts are marked by ⚠ in the schematic diagrams, Exploded Views and replacement parts list. It is essential that these critical parts should be replaced with manufacturer's specified parts to prevent shock, fire, or other hazards. Do not modify the original design without permission of manufacturer.

3. Control Button Locations and Explanations

■ Front Panel Illustration



❶ POWER switch

❷ Disc tray

❸ OPEN/CLOSE button

❹ PLAY/PAUSE button

❺ STOP button

❻ MIC VOLUME knob

❼ MIC jack

❽ IR SENSOR

❾ Display window

4.PREVENTION OF STATIC ELECTRICITY DISCHARGE

The laser diode in the traverse unit (optical pickup)may brake down due to static electricity of clothes or human body. Use due caution to electrostatic breakdown when servicing and handling the laser diode.

4.1.Grounding for electrostatic breakdown prevention

Some devices such as the DVD player use the optical pickup(laser diode)and the optical pickup will be damaged by static electricity in the working environment.Proceed servicing works under the working environment where grounding works is completed.

4.1.1. Worktable grounding

1. Put a conductive material(sheet)or iron sheet on the area where the optical pickup is placed,and ground the sheet.

4.1.2.Human body grounding

1 Use the anti-static wrist strap to discharge the static electricity from your body.

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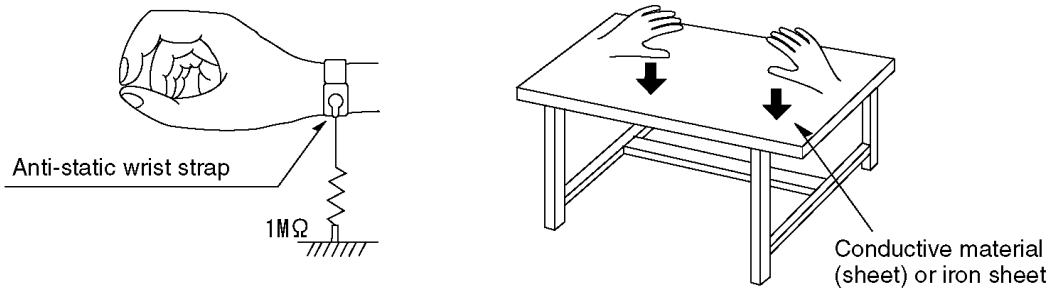


4.1.3.Handling of optical pickup

1. To keep the good quality of the optical pickup maintenance parts during transportation and before installation, the both ends of the laser diode are short-circuited.After replacing the parts with new ones, remove the short circuit according to the correct procedure. (See this Technical Guide).

2. Do not use a tester to check the laser diode for the optical pickup .Failure to do so willdamage the laser diode due to the power supply in the tester.

4.2. Handling precautions for Traverse Unit (Optical Pickup)

1. Do not give a considerable shock to the traverse unit(optical pickup)as it has an extremely high-precise structure.

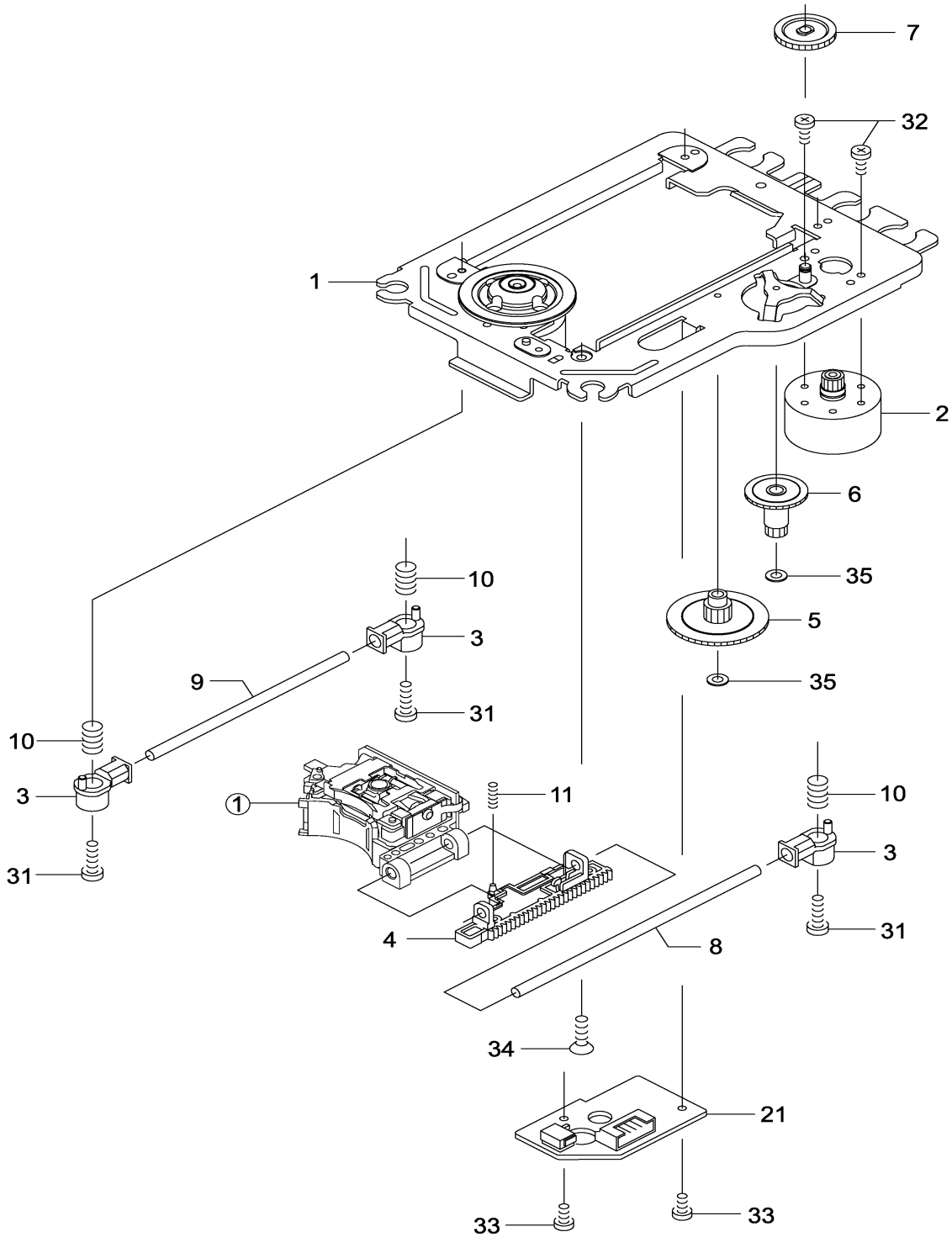
2. When replacing the optical pickup, install the flexible cable and cut is short land with a nipper. See the optical pickup replacement procedure in this Technical Guide. Before replacing the traverse unit, remove the short pin for preventingstatic electricity and install a new unit.Connect the connector as short times as possible.

3. The flexible cable may be cut off if an excessive force is applied to it.Use caution when handling the cable

4. The half-fixed resistor for laser power adjustment cannot be adjusted. Do not turn the resistor.

5. Assembling and disassembling the mechanism unit

5.1 Optical pickup Unit Explosed View and Part List



Pic (1)

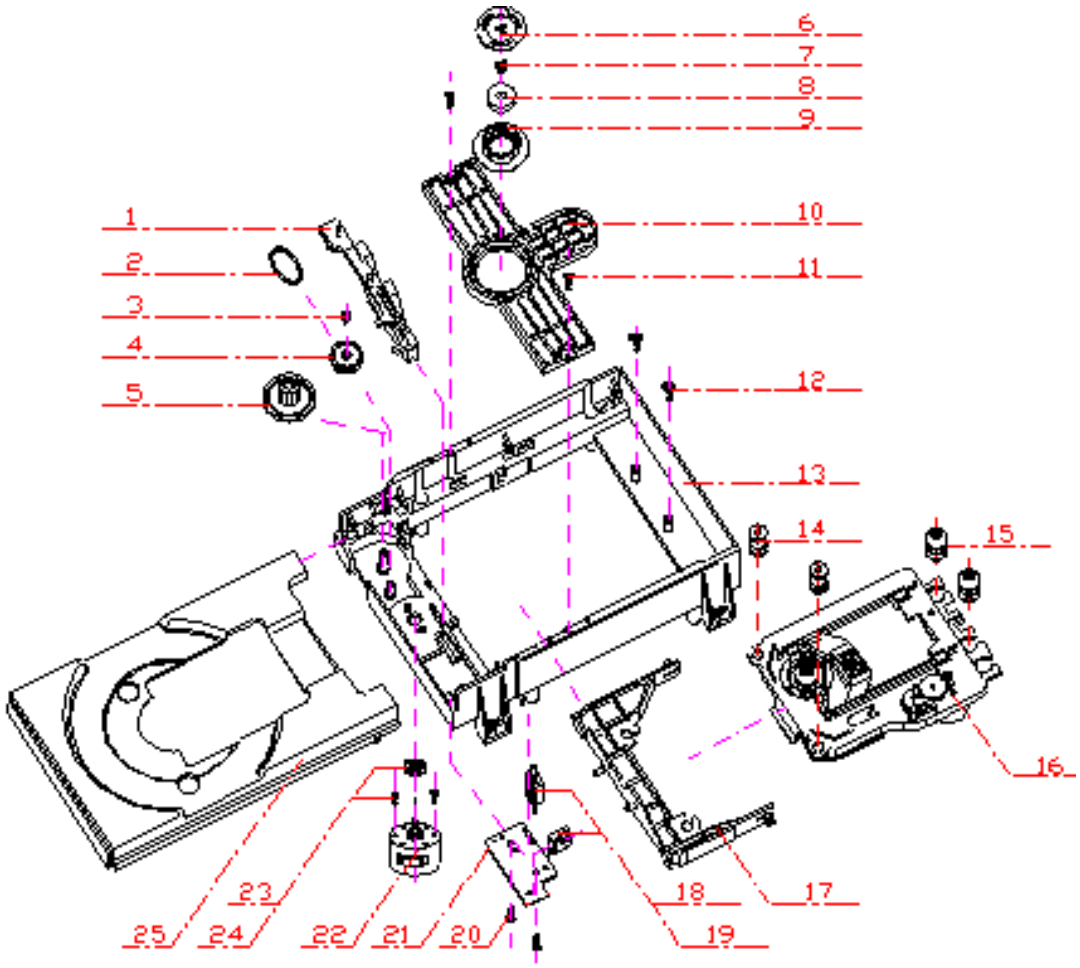
Materials to Pic (1)

No.	PARTS CODE	PARTS NAME	Q'ty
①	14692200	SF-HD60	1
1	1EA0311A06300	ASSY, CHASSIS, COMPLETE	1
2	1EA0M10A15500	ASSY, MOTOR, SLED	1
Or	1EA0M10A15501	ASSY, MOTOR, SLED	1
3	1EA2451A24700	HOLDER, SHAFT	3
4	1EA2511A29100	GEAR, RACK	1
5	1EA2511A29200	GEAR, DRIVE	1
6	1EA2511A29300	GEAR, MIDDLE, A	1
7	1EA2511A29400	GEAR, MIDDLE, B	1
8	1EA2744A03000	SHAFT, SLIDE	1
9	1EA2744A03100	SHAFT, SLIDE, SUB	1
10	1EA2812A15300	SPRING, COMP, TYOUSEI	3
11	1EA2812A15400	SPRING, COMP, RACK	1
21	1EA0B10B20100	ASSY, PWB	1
Or	1EA0B10B20200	ASSY, PWB	1
31	SEXEA25700---	SPECIAL SCREW BIN+-M2X11	3
32	SEXEA25900---	SPECIAL SCREW M1.7X2.2	2
33	SFBPN204R0SE-	SCR S-TPG PAN 2X4	2
34	SFSFN266R0SE-	SCR S-TPG FLT 2.6X6	1
35	SWXEA15400---	SPECIAL WASHER 1.8X4 X0.25	2

□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□

Note : This parts list is not for service parts supply.

5.2 Bracket Explosed View and Part List



Pic (2)

Materials to Pic(2)

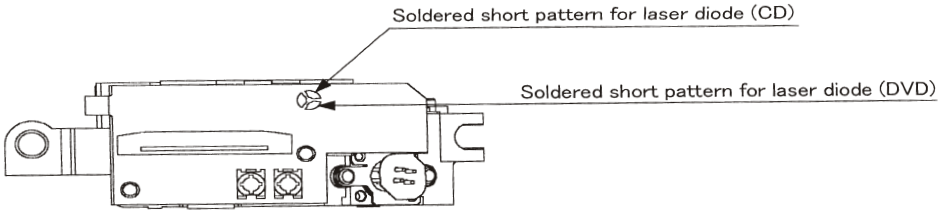
1.bracket
2.belt
3.screw
4.belt wheel
5.gearwheel
6.iron chip
7. Immobility mechanism equipment
8. Magnet
9. Platen
10. Bridge bracket
11. screw
12. screw
13. Big bracket
14. front silicon rubber
15. Back silicon rubber
16. Pick-up
17. Pick-up
18. switch
19. Five-pin flat plug
20. screw
21. PCB
22. motor
23. Motor wheel
24. screw
25.tray

Before going process with disassembly and installation, please carefully both peruse the chart and confirm the materials.

5.3 MISCELLANEOUS

5.3.1 Protection of the LD(Laser diode)

Short the parts of LD circuit pattern by soldering.



5.3.2 Cautions on assembly and adjustment

Make sure that the workbenches,jigs,tips,tips of soldering irons and measuring instruments are grounded,and that personnel wear wrist straps for ground.

Open the LD short lands quickly with a soldering iron after a circuit is connected.

Keep the power source of the pick-up protected from internal and external sources of electrical noise.

Refrain from operation and storage in atmospheres containing corrosive gases (such as H2S,SO2, NO2 and Cl2)or toxic gases or in locations containing substances(especially from the organic silicon,cyan, formalin and phenol groups)which emit toxic gases.It is particularly important to ensure that none of the above substances are present inside the unit.Otherwise,the motor may no longer run.

6.Electrical Confirmation

6.1. Video Output (Luminance Signal) Confirmation

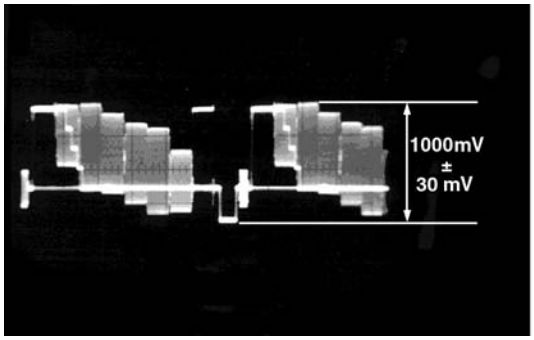
DO this confirmation after replacing a P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
200mV/dir,10 μ sec/dir	1000mVp-p±30mV	

Purpose:To maintain video signal output compatibility.

1.Connect the oscilloscope to the video output terminal and terminate at 75 ohms.

2.Confirm that luminance signal(Y+S)level is 1000mVp-p±30mV



6.2 Video Output(Chrominance Signal) Confirmation

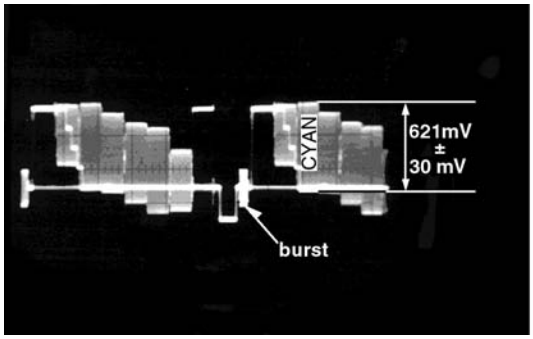
Do the confirmation after replacing P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
Screwdriver,Oscilloscope 200mV/dir,10 μ sec/dir	621mVp-p±30mV	

Purpose:To maintain video signal output compatibility.

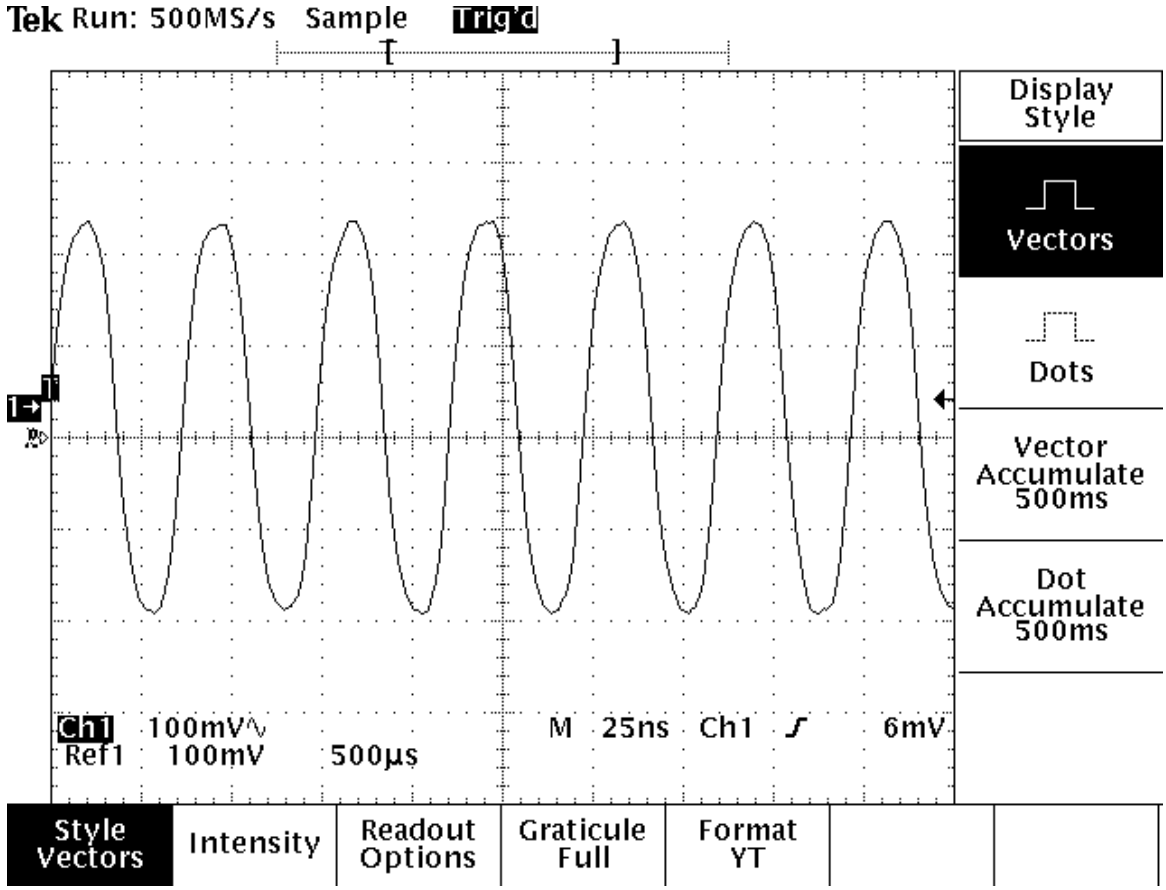
1.Connect the oscilloscope to the video output terminal and terminate at 75 ohme.

2.Confirm that the chrominance signal(C)level is 621 mVp-p±30mV

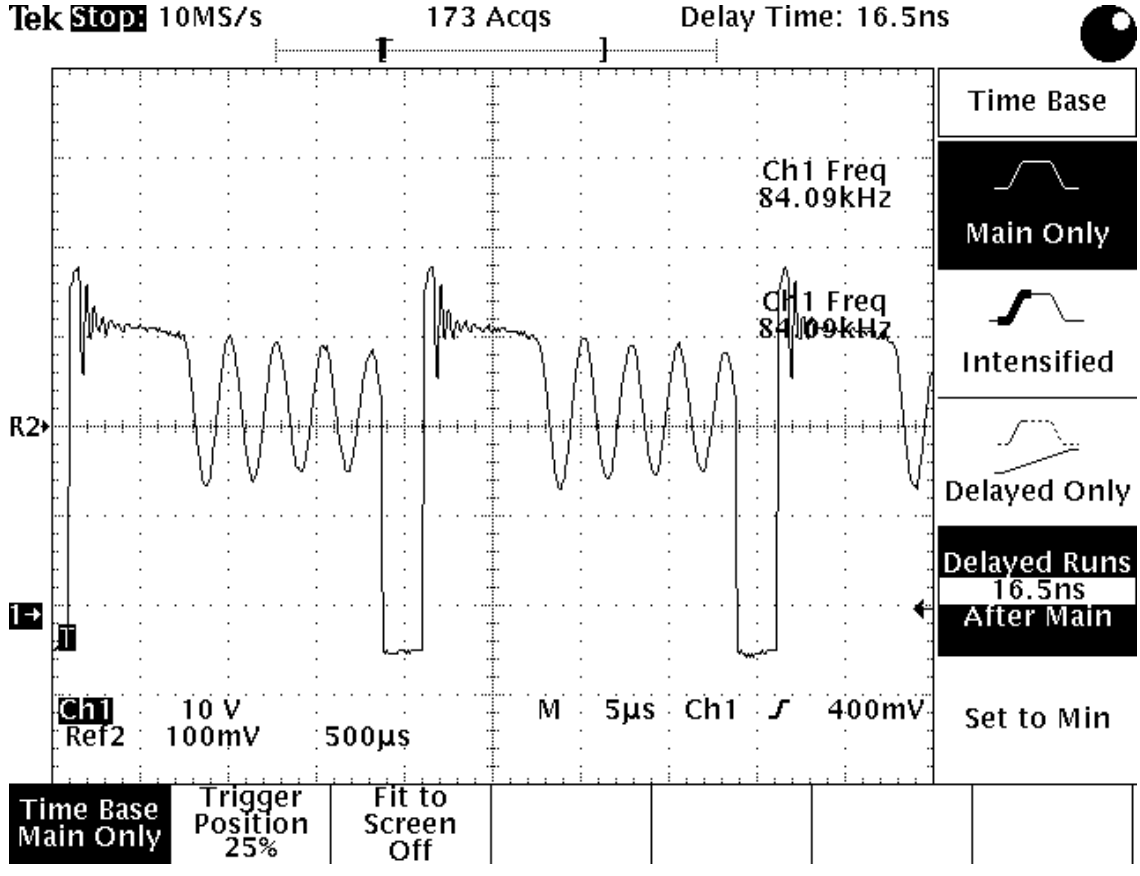


7.MPEG BOARD CHECK WAVEFORM

7.1 27MHz WAVEFORM



7.2 IC5L0380R PIN.2 WAVEFORM DIAGRAM



8. IC BLOCK DIAGRAM & DESCRIPTION

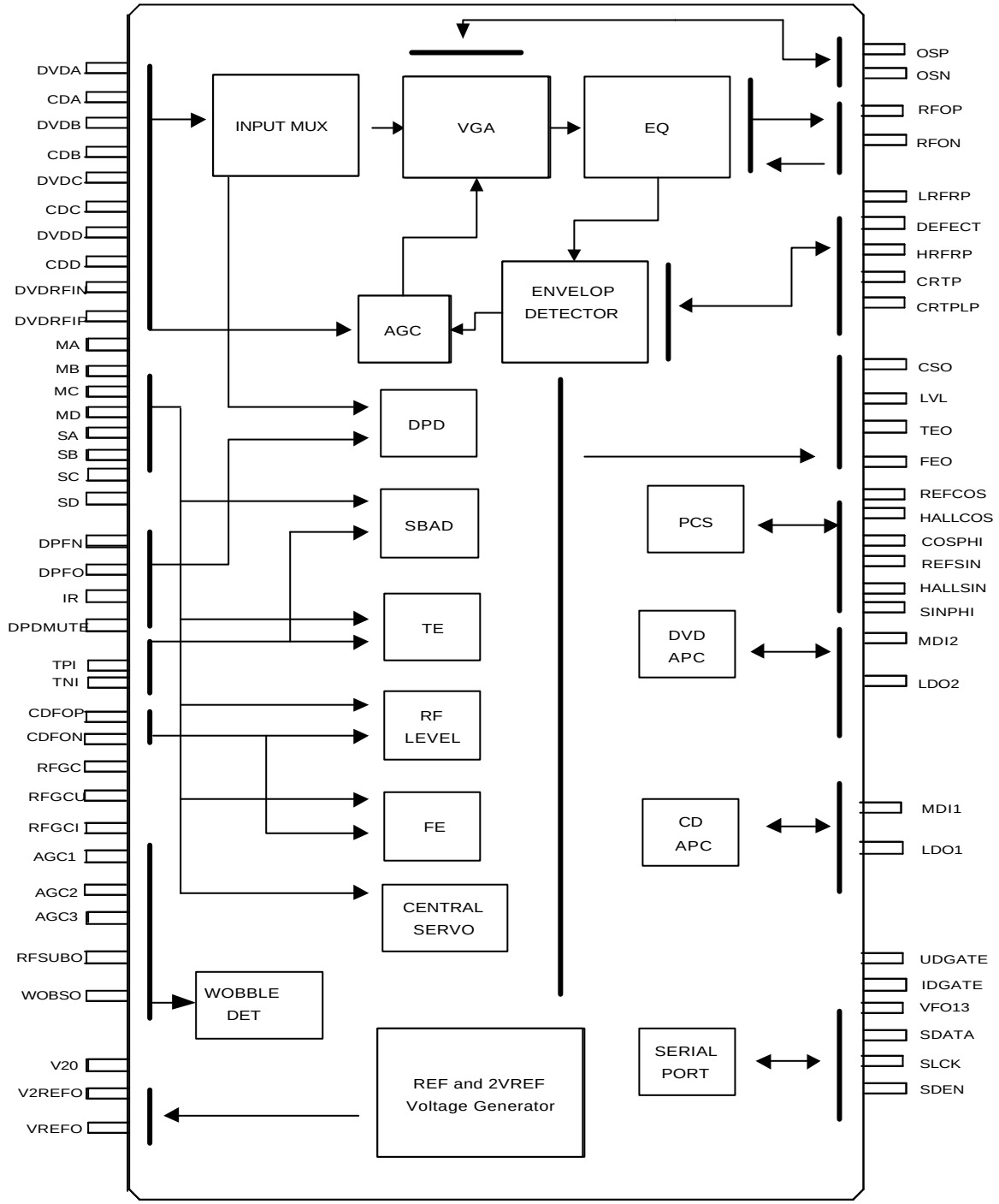
8.1 MT1336

GENERAL DESCRIPTION

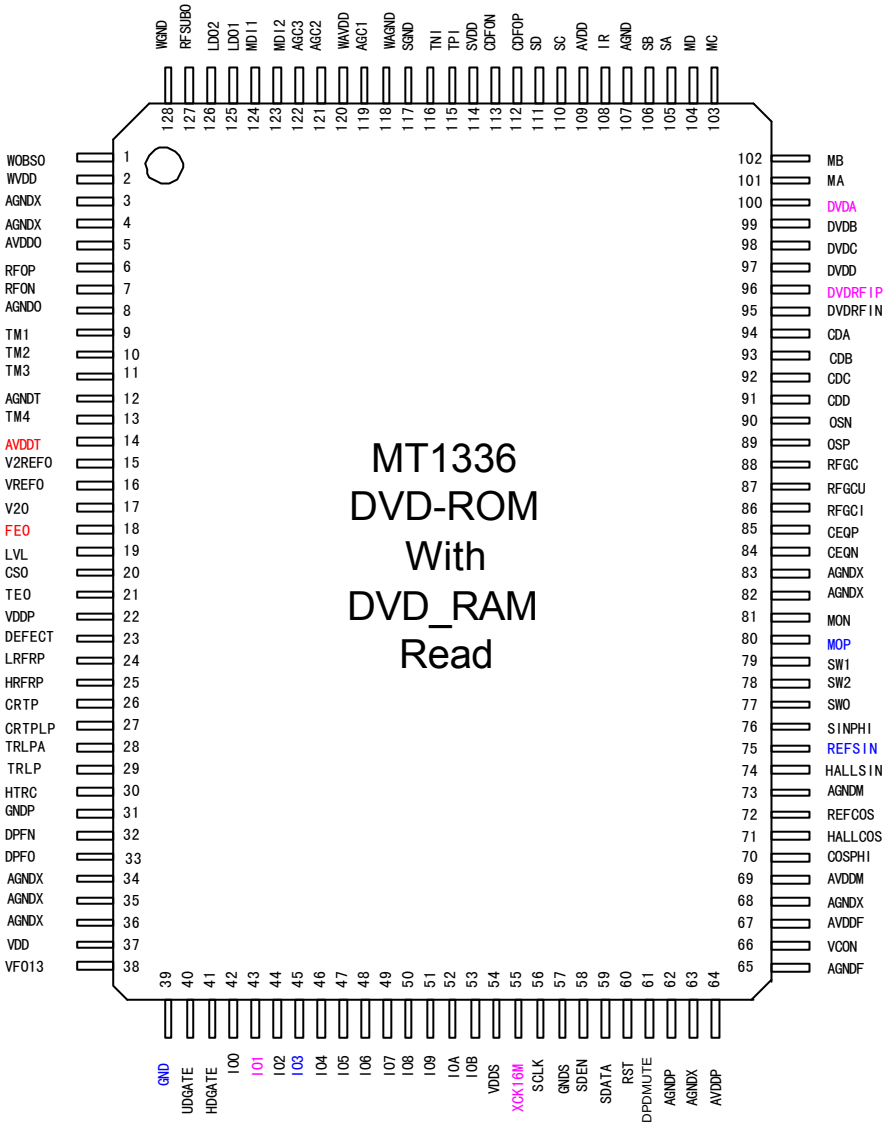
MT1336 is a high performance CMOS analog front-end IC for both CD_ROM driver up to 48XS and DVD-ROM driver up to 16XS. It also supports DVD-RAM read up to 4XS Version 2. It contains servo amplifiers to generate focusing error, 3-beam tracking error, 1 beam radial push-pull signal, RF level and SBAD for servo functions. It also includes DPD tracking error signal for DVD_ROM application. For DVD-RAM disks, there are also Differential Push-Pull (DPP) method for generating tracking signal and Differential Astigmatic Detection (DAD) for processing focusing signal. Programmable equalizer and AGC circuits are also incorporated in this chip to optimize read channel performance. In addition, this chip has dual automatic laser power control circuits for DVD-ROM (DVD-RAM) and CD-ROM seperately and reference voltage generators to reduce external components. Programmable functions are implemented by the access of internal register through bi-directional serial port to configure modes selection.

FEATURES

- RF equalizer with programmable f_c from 3MHz to 70 MHz and programmable boost from 3dB to 13dB.
- MT1336 supports at least eight different kinds of pick-up heads with versatile input configuration for both RF input stages and servo signal blocks.
- Versatile on-line AGC.
- 3 beams tracking error signal generator for CD_ROM application.
- One beam differential phase tracking error (DPD) generator for DVD_ROM application.
- Differential push pull tracki ng error (DPP) generator for DVD_RAM application.
- Focusing error signal generator for CD-ROM, DVD-ROM and DVD-RAM (DAD method).
- RF level signal generator.
- Sub-beam added signal for 3 beams CD_ROM.
- One beam push-pull signal generator for central servo application.
- High speed RF envelop detection circuit with bandwidth up to 400KHz for CD-ROM.
- Defect and Blank detection circuits.
- Dual automatic laser power control circuits with programmable level of LD monitor voltage.
- Vref=1.4V voltage and V2ref=2.8V voltage generators.
- V20=2.0V voltage for pick-up head reference.
- Bi-directional serial port to access internal registers.



MT1336 FUNCTION BLOCKS DIAGRAM



MT1336 PIN ASSIGNMENT

MT1336 PIN DESCRIPTIONS

Pin Numbers	Symbol	Type	Description
LQFP128			
RF Flag Interface			
23	DEFECT	Digital Output	Flag of bad data output status
RF SIO interface			
56	SCLK	Digital Input	RF serial clock input
58	SDEN	Digital Input	RF serial data enable
59	SDATA	Digital IO	RF serial data IO
60	RST	Digital input	Reset (active high)
55	XCK16M	Digital Input	16.9MHz for verification
RF SERVO interface			
40	UDGATE	Digital Input	Control signal for DVD-RAM
41	IDGATE	Digital Input	Control signal for DVD-RAM
38	VFO13	Digital Input	DVD-RAM Header signal
RF			
100	DVDA	Analog input	AC coupled DVD RF signal input A
99	DVDB	Analog Input	AC coupled DVD RF signal input B
98	DVDC	Analog Input	AC coupled DVD RF signal input C
97	DVDD	Analog Input	AC coupled DVD RF signal input D
95	DVDRFIN	Analog Input	AC coupled DVD RF signal input RFIN
96	DVDRFIP	Analog Input	AC coupled DVD RF signal input RFIP
94	CDA	Analog Input	AC coupled CD RF signal input A
93	CDB	Analog Input	AC coupled CD RF signal input B
92	CDC	Analog Input	AC coupled CD RF signal input C
91	CDD	Analog Input	AC coupled CD RF signal input D
90	OSN	Analog	RF Offset cancellation capacitor connecting
89	OSP	Analog	RF Offset cancellation capacitor connecting
85	CEQP	Analog	RF Offset cancellation capacitor connecting
84	CEQN	Analog	RF Offset cancellation capacitor connecting
88	RFGC	Analog	RF AGC loop capacitor connecting for DVD-ROM

87	RFGCU	Analog	RF AGC loop capacitor connecting for DVD-RAM
86	RFGCI	Analog	RF AGC loop capacitor connecting for DVD-RAM
101	MA	Analog Input	DC coupled DVD-RAM main-beam RF signal input A
102	MB	Analog Input	DC coupled DVD-RAM main-beam RF signal input B
103	MC	Analog Input	DC coupled DVD-RAM main-beam RF signal input C
104	MD	Analog Input	DC coupled DVD-RAM main-beam RF signal input D
105	SA	Analog Input	DC coupled DVD-RAM sub-beam RF signal input A
106	SB	Analog Input	DC coupled DVD-RAM sub-beam RF signal input B
110	SC	Analog Input	DC coupled DVD-RAM sub-beam RF signal input C
111	SD	Analog Input	DC coupled DVD-RAM sub-beam RF signal input D
108	IR	Analog	External current bias resistor (R=20K)
119	AGC1	Analog	Wobble AGC loop1 capacitor
121	AGC2	Analog	Wobble AGC loop2 capacitor
122	AGC3	Analog	Wobble AGC loop3 capacitor
127	RFSUBO	Analog output	Header push-pull RF output signal
1	WOBSO	Digital output	Wobble signal output
6	RFOP	Analog output	RF positive output
7	RFON	Analog output	RF negative output
TRACKING ERROR			
32	DPFN	Analog	DPD amplifier negative input
33	DPFO	Analog	DPD amplifier output
61	DPDMUTE	Digital input	DPD mute control input
116	TNI	Analog Input	3 beam satellite PD signal negative input
115	TPI	Analog Input	3 beam satellite PD signal positive input
21	TEO	Analog Output	Tracking error output
FOCUSING ERROR & RF LEVEL & CENTRAL SERVO SIGNAL			
112	CDFOP	Analog Input	CD focusing error positive input
113	CDFON	Analog Input	CD focusing error negative input
18	FEO	Analog Output	Focusing error output
19	LVL	Analog Output	RF level output
20	CSO	Analog output	Central servo signal output
ALPC			

124	MDI1	Analog Input	Laser power monitor input
125	LDO1	Analog Ou tput	Laser driver output
123	MDI2	Analog Input	Laser power monitor input
126	LDO2	Analog Output	Laser driver output
RF RIPPLE			
26	CRTP	Analog	RF top envelop filter capacitor connecting
27	CRTPLP	Analog	Defect level filter capacitor connecting
25	HRFRP	Analog output	High frequency RF ripple output or Blank detector' s output
24	LRFRP	Analog output	Low frequency RF ripple output
POWER			
67, 69	AVDD	Power	Master PLL Filter power
65, 73	AGND	GND	GND for Master PLL Filter
64	AVDD	Power	DPD Power
62	AGND	GND	DPD GND
109	AVDD	Power	RF path Power
107	AGND	GND	RF path GND
114	SVDD	Power	Servo Power
117	SGND	GND	Servo GND
2,120	WAVDD	Power	Wobble Power
128,118	WAGND	GND	Wobble GND
5	AVDDO	Power	Power for RF output
8	AGNDO	GND	GND for RF output
14	AVDDT	Power	Power for Trimming PAD
12	AGNDT	GND	GND for Trimming PAD
22	VDDP	Power	Peak Detection Power
31	GNDP	GND	Peak Detection GND
37,54	VDD	Power	Serial I/O Power
39,57	GND	GND	Serial I/O GND
REFERENCE VOLTAGE			
16	VREFO	Analog output	Reference voltage 1.4V
15	V2REFO	Analog output	Reference voltage 2.8V
17	V20	Analog Output	Reference voltage 2.0V

ALPC TRIMMING			
9	TM1	Analog input	Trimming pin for ALPC1
10	TM2	Analog input	Trimming pin for ALPC1
11	TM3	Analog input	Trimming pin for ALPC2
13	TM4	Analog input	Trimming pin for ALPC2
HIGH SPEED TRACK COUNTING			
29	TRLP	Analog	Low-pass filter capacitor connecting
28	TRLPA	Analog	Low-pass filter capacitor connecting
30	HTRC	Digital output	High speed track counting digital output
PCS			
74	HALLSIN	Analog input	Negative input of amplifier for hall sensor signal
75	REFSIN	Analog input	Positive input of amplifier for hall sensor signal
76	SINPHI	Analog output	Amplifier output for hall sensor signal
71	HALLCOS	Analog input	Negative input of amplifier for hall sensor signal
72	REFCOS	Analog input	Positive input of amplifier for hall sensor signal
70	COSPHI	Analog output	Amplifier output for hall sensor signal
FOR MONITOR ONLY			
81	MON	Analog output	
80	MOP	Analog output	
66	VCON	Analog output	
77	SWO	Analog output	Output from mux of SW1 & SW2
78	SW2	Analog input	External input for servo input select
79	SW1	Analog input	External input for servo input select
FOR SERIAL I/O			
42	IO0		
43	IO1		
44	IO2		
45	IO3		
46	IO4		
47	IO5		

48	IO6		
49	IO7		
50	IO8		
51	IO9		
52	IOA		
53	IOB		

8.2 MT1379

- Super Integration DVD player single chip
  - Servo controller and data channel processing
  - MPEG-1/MPEG-2/JPEG video decoding
  - Dolby AC-3/DTS/DVD-Audio audio decoding
  - Unified track buffer and A/V decoding buffer
  - Video processing for scaling and video quality enhancement
  - OSD & Sub-picture decoding
  - Built-in clock generator
  - Built-in TV encoder
  - Built-in progressive video output
  - Video input port and audio/SPDIF input port
- Speed Performance on Servo and Decoding
  - DVD-ROM up to 8XS
  - CD-ROM up to 24XS
  - Built-in a frequency programmable clock to µP and RSPC Decoder to optimize the performance over power
- Channel Data Processor
  - Provides interface with analog front-end processor
  - Analog data slicer for small jitter capability
  - Built-in high performance data PLL for channel data demodulation
  - EFM/EFM+ data demodulation
  - Enhanced channel data frame sync protection & DVD-ROM sector sync protection
- Servo Control and Spindle Motor Control
  - Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
  - Provide a varipitch speed control for CLV and CAV mode
  - Built-in ADCs and DACs for digital servo control
  - Provide 2 general PWM
  - Tray control can be PWM output or digital output
  - Built-in DSP for digital servo control
- Host Micro controller
  - Built-in 8032 micro controller
  - Built-in internal 373 and 8-bit programmable lower address port
  - 1024-bytes on-chip RAM
  - Up to 2M bytes FLASH-programming interface
  - Supports 5/3.3-Volt. FLASH interface
  - Supports power-down mode
  - Supports additional serial port
- DVD-ROM/CD-ROM Decoding Logic
  - Supports CD-ROM Mode 1, CD-ROM XA Mode 2 Form 1, CD-ROM XA Mode 2 Form 2, and CD-DA formats
  - High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
  - Automatic sector Mode and Form detection
  - Automatic sector Header verification
  - 8-bit counter for decode completion check
  - Programmable descrambling and error correction schemes
  - Automatically repeated error corrections
  - 8-bit C2 Pointer counter
  - Decoder Error Notification Interrupt that signals various decoder errors
  - Provide error correction acceleration
- Buffer Memory Controller
  - Supports 16Mb/32Mb/64Mb/128Mb SDRAM
  - Supports 16-bit/32-bit SDRAM data bus interface
  - Build in a DRAM interface programmable clock to optimize the DRAM performance
  - Provide the self-refresh mode SDRAM
  - Programmable DRAM access cycle and refresh

cycle timings
- Block-based sector addressing
- Programmable buffering counter for buffer status tracking
- Maximum DRAM speed is 133MHz
- Support 5/3.3-Volt. DRAM Interface

■ Video Decode
- Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
- Maximum input bit-rate of 15Mbits/sec
- Smooth digest view function with I, P and B picture decoding
- Baseline, extended-sequential and progressive JPEG image decoding
- RLE and non-RLE BMP image decoding
- Support CD-G titles

■ Video/OSD/SPU/HLI Processor
- Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
- 65535/256/16/4/2-color bitmap format OSD,
- 256/16 color RLC format OSD
- Automatic scrolling of OSD image
- Provides 4-color/32x32-pixel hardware cursor
- Fade-in, Fade out, and Wipe functions as specified in the DVD-Audio Specification and other slide show transition effects
- Progressive scan output

■ Audio Processing
- Decoder format supports:
  - Dolby Digital (AC-3) decoding
  - DTS decoding
  - MLP decoding for DVD-Audio
  - MPEG-1 layer 1/layer 2 audio decoding
  - MPEG-2 layer1/layer2 2-channel audio decoding
  - Dolby Pro Logic decoding
  - High Definition Compatible Digital (HDCD) decoding
- Up to 6 channel linear PCM output for DVD Audio / DVD Video
- Downmix function
- Support IEC 60958/61937 output
  - PCM / bit stream / mute mode
  - Custom IEC latency up to 2 frames
- Pink noise and white noise generator
- Karaoke functions
  - Microphone echo with adjustable echo level, echo -depth and delay length
  - Microphone tone control with three custom second-order IIR filter
  - Vocal mute/vocal assistant
  - Key shift up to +/- 8 keys controlled by 1/2 key
- Channel equalizer
- 3D surround processing include virtual surround and speaker separation
- Power-down control
- HDCD certified

■ TV Encoder
- Six 54MHz/12bit DA converters
- Support NTSC, PAL-BDGHI, PAL-N, PAL-M interlace TV format and 480p, 576p progressive TV format
- Automatically turn off unconnected channel(s).
- Support PC monitor (VGA)
- Support Macrovision 7.1

■ Progressive Output
- Automatic detect film or video source
- 3:2 pull down source detection
- Advanced Motion adaptive de-interlace
- Minimum external memory requirement

■ Audio/Video Output
- Line-in/SPDIF-in for versatile audio processing
- CCIR601/656 video input port
- Support picture-in-picture for video decoding and input source

■ Outline
- 216-pin LQFP package
- 3.3/2.5-Volt. Dual operating voltages

PIN DEFINITIONS

Pin Number	Symbol	Type	Description
1	IREF	Analog Input	Current reference input. It generates reference current for data PLL. Connect an external 100K resistor to this pin and PLLVSS.
2	PLLVSS	Ground	Ground pin for data PLL and related analog circuitry
3	LPIOP	Analog Output	Positive output of the low pass filter
4	LPION	Analog Output	Negative output of the low pass filter
5	LPFON	Analog output	Negative output of loop filter amplifier
6	LPFIP	Analog Input	Positive input of loop filter amplifier
7	LPFIN	Analog Input	Negative input of loop filter amplifier
8	LPFOP	Analog Output	Positive output of loop filter amplifier
9	JITFO	Analog Output	RF jitter meter output
10	JITFN	Analog Input	Negative input of the operation amplifier for RF jigger meter
11	PLLVDD3	Power	3.3V power pin for data PLL and related analog circuitry
12	FOO	Analog Output	Focus servo output. PDM output of focus servo compensator
13	TRO	Analog Output	Tracking servo output. PDM output of tracking servo compensator
14	TROPENPWM	Analog Output	Tray open output, controlled by microcontroller. This is PWM output for TRWMEN27hRW2=1 or is digital output for TRWMEN27hRW2=0
15	PWMOUT1	Analog Output	The 1st general PWM output
16	PWMOUT2	Analog Output	The 2nd general PWM output
17	DVDD2	Power	2.5V power pin for internal fully digital circuitry
18	DMO	Analog Output	Disk motor control output. PWM output
19	FMO	Analog Output	Feed motor control. PWM output
20	DVSS	Ground	Ground pin for internal fully digital circuitry
21	FG	Input	Motor Hall sensor input
22	HIGHA0	Inout 2~16MA, SR PU	Microcontroller address 8
23	HIGHA1	Inout 2~16MA, SR PU	Microcontroller address 9
24	HIGHA2	Inout 2~16MA, SR PU	Microcontroller address 10
25	HIGHA3	Inout 2~16MA, SR PU	Microcontroller address 11
26	HIGHA4	Inout 2~16MA, SR PU	Microcontroller address 12
27	HIGHA5	Inout 2~16MA, SR PU	Microcontroller address 13
28	DVSS	Ground	Ground pin for internal digital circuitry

Pin Number	Symbol	Type	Description
29	HIGHA6	Inout 2~16MA, SR PU	Microcontroller address 14
30	HIGHA7	Inout 2~16MA, SR PU	Microcontroller address 15
31	AD7	Inout 2~16MA, SR	Microcontroller address/data 7
32	AD6	Inout 2~16MA, SR	Microcontroller address/data 6
33	AD5	Inout 2~16MA, SR	Microcontroller address/data 5
34	AD4	Inout 2~16MA, SR	Microcontroller address/data 4
35	DVDD3	Power	3.3V power pin for internal digital circuitry
36	AD3	Inout 2~16MA, SR	Microcontroller address/data 3
37	AD2	Inout 2~16MA, SR	Microcontroller address/data 2
38	AD1	Inout 2~16MA, SR	Microcontroller address/data 1
39	AD0	Inout 2~16MA, SR	Microcontroller address/data 0
40	IOA0	Inout 2~16MA, SR PU	Microcontroller address 0 / IO
41	IOA1	Inout 2~16MA, SR PU	Microcontroller address 1 / IO
42	DVDD2	Power	2.5V power pin for internal digital circuitry
43	IOA2	Inout 2~16MA, SR PU	Microcontroller address 2 / IO
44	IOA3	Inout 2~16MA, SR PU	Microcontroller address 3 / IO
45	IOA4	Inout 2~16MA, SR PU	Microcontroller address 4 / IO
46	IOA5	Inout 2~16MA, SR PU	Microcontroller address 5 / IO
47	IOA6	Inout 2~16MA, SR PU	Microcontroller address 6 / IO

Pin Number	Symbol	Type	Description
48	IOA7	Inout 2~16MA, SR PU	Microcontroller address 7 / IO
49	A16	Output 2~16MA, SR	Flash address 16
50	A17	Output 2~16MA, SR	Flash address 17
51	IOA18	Inout 2~16MA, SR SMT	Flash address 18 / IO
52	IOA19	Inout 2~16MA, SR SMT	Flash address 19 / IO
53	IOA20	Inout 2~16MA, SR SMT	Flash address 20 / IO OR Videoin Data PortB 0
54	APLLVSS	Ground	Ground pin for audio clock circuitry
55	APLLVDD3	Power	3.3V Power pin for audio clock circuitry
56	ALE	Inout 2~16MA, SR PU, SMT	Microcontroller address latch enable
57	IOOE#	Inout 2~16MA, SR SMT	Flash output enable, active low / IO
58	IOWR#	Inout 2~16MA, SR SMT	Flash write enable, active low / IO
59	IOCS#	Inout 2~16MA, SR PU, SMT	Flash chip select, active low / IO
60	DVSS	Ground	Ground pin for internal digital circuitry
61	UP1_2	Inout 4MA, SR PU, SMT	Microcontroller port 1-2
62	UP1_3	Inout 4MA, SR PU, SMT	Microcontroller port 1-3
63	UP1_4	Inout 4MA, SR PU, SMT	Microcontroller port 1-4
64	UP1_5	Inout 4MA, SR PU, SMT	Microcontroller port 1-5
65	UP1_6	Inout 4MA, SR PU, SMT	Microcontroller port 1-6
66	DVDD3	Power	3.3V power pin for internal digital circuitry

Pin Number	Symbol	Type	Description
67	UP1_7	Inout 4MA, SR PU, SMT	Microcontroller port 1-7
68	UP3_0	Inout 4MA, SR PU, SMT	Microcontroller port 3-0
69	UP3_1	Inout 4MA, SR PU, SMT	Microcontroller port 3-1
70	INT0#	Inout 2~16MA, SR PU, SMT	Microcontroller interrupt 0, active low
71	IR	Input SMT	IR control signal input
72	DVDD2	Power	2.5V power pin for internal digital circuitry
73	UP3_4	Inout	Microcontroller port 3-4
74	UP3_5	Inout	Microcontroller port 3-5
75	UWR#	Inout 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
76	URD#	Inout 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
77	DVSS	Ground	Ground pin for internal digital circuitry
78	RD7	Inout	DRAM data 7
79	RD6	Inout	DRAM data 6
80	RD5	Inout	DRAM data 5
81	RD4	Inout	DRAM data 4
82	DVDD2	Power	2.5V power pin for internal digital circuitry
83	RD3	Inout	DRAM data 3
84	RD2	Inout	DRAM data 2
85 86	RD1 RD0	Inout Inout	DRAM data 1 DRAM data 0
87	RWE#	Output 2~16MA, SR	DRAM Write enable, active low
88	CAS#	Output 2~16MA, SR	DRAM columnaddress strobe, active low
89	RAS#	Output 2~16MA, SR	DRAM row address strobe, active low
90	RCS#	Output 2~16MA, SR	DRAM chip select, active low
91	BA0	Output 2~16MA, SR	DRAM bank address 0
92	DVSS	Ground	Ground pin for internal digital circuitry
93	RD15	Inout 2~16MA, SR PU/PD, SMT	DRAM data 15

Pin Number	Symbol	Type	Description
94	RD14	Inout 2~16MA, SR PU/PD, SMT	DRAM data 14
95	RD13	Inout 2~16MA, SR PU/PD, SMT	DRAM data 13
96	RD12	Inout 2~16MA, SR PU/PD, SMT	DRAM data 12
97	DVDD3	Power	3.3V power pin for internal digital circuitry
98	RD11	Inout 2~16MA, SR PU/PD, SMT	DRAM data 11
99	RD10	Inout 2~16MA, SR PU/PD, SMT	DRAM data 10
100	RD9	Inout 2~16MA, SR PU/PD, SMT	DRAM data 9
101	RD8	Inout 2~16MA, SR PU/PD, SMT	DRAM data 8
102	DVSS	Ground	Ground pin for internal digital circuitry
103	CLK	Output 2~16MA, SR	DRAM clock
104	CLE	Output 2~16MA, SR	DRAM clock enable
105	RA11	Output 2~16MA, SR	DRAM address bit 11 or audio serial data 3 (channel 7/8)
106	RA9	Output 2~16MA, SR	DRAM address 9
107	RA8	Output 2~16MA, SR	DRAM address 8
108	DMVDD3	Power	3.3V Power pin for DRAM clock circuitry
109	DMVSS	Ground	Ground pin for DRAM clock circuitry
110	RA7	Output 2~16MA, SR	DRAM address 7
111	DVDD3	Power	3.3V power pin for internal digital circuitry
112	RA6	Output 2~16MA, SR	DRAM address 6
113	RA5	Output 2~16MA, SR	DRAM address 5
114	RA4	Output 2~16MA, SR	DRAM address 4
115	DVSS	Ground	Ground pin for internal digital circuitry
116	DQM1	Output 2~16MA, SR	Mask for DRAM input/output byte 1

Pin Number	Symbol	Type	Description
117	DQM0	Output 2~16MA, SR	Mask for DRAM input/output byte 0
118	BA1	Output 2~16MA, SR	DRAM bank address 0
119	RA10	Output 2~16MA, SR	DRAM address10
120	DVDD2	Power	2.5V power pin for internal digital circuitry
121	RA0	Output 2~16MA, SR	DRAM address 0
122	RA1	Output 2~16MA, SR	DRAM address 1
123	RA2	Output 2~16MA, SR	DRAM address 2
124	RA3	Output 2~16MA, SR	DRAM address 3
125	DVSS	Ground	Ground pin for internal digital circuitry
126	RD31	Inout 2~16MA, SR PU/PD, SMT	DRAM data 31
127	RD30	Inout 2~16MA, SR PU/PD, SMT	DRAM data 30
128	RD29	Inout 2~16MA, SR PU/PD, SMT	DRAM data 29
129	RD28	Inout 2~16MA, SR PU/PD, SMT	DRAM data 28
130	DVDD3	Power	3.3V power pin for internal digital circuitry
131	RD27	Inout 2~16MA, SR PU/PD, SMT	DRAM data 27
132	RD26	Inout 2~16MA, SR PU/PD, SMT	DRAM data 26
133	RD25	Inout 2~16MA, SR PU/PD, SMT	DRAM data 25
134	RD24	Inout 2~16MA, SR PU/PD, SMT	DRAM data 24
135	DVSS	Ground	Ground pin for internal digital circuitry
136	DQM3	Output 2~16MA, SR	Mask for DRAM input/output byte 3
137	DQM2	Output 2~16MA, SR	Mask for DRAM input/output byte 2

Pin Number	Symbol	Type	Description
138	RD23	Inout 2~16MA, SR PU/PD, SMT	DRAM data 23 / Videoin Data PortA 7
139	RD22	Inout 2~16MA, SR PU/PD, SMT	DRAM data 22 / Videoin Data PortA 6
140	DVDD2	Power	2.5V power pin for internal digital circuitry
141	RD21	Inout 2~16MA, SR PU/PD, SMT	DRAM data 21 / Videoin Data PortA 5
142	RD20	Inout 2~16MA, SR PU/PD, SMT	DRAM data 20 / Videoin Data PortA 4
143	RD19	Inout 2~16MA, SR PU/PD, SMT	DRAM data 19 / Videoin Data PortA 3
144	RD18	Inout 2~16MA, SR PU/PD, SMT	DRAM data 18 / Videoin Data PortA 2
145	DVSS	Ground	Ground pin for internal digital circuitry
146	RD17	Inout 2~16MA, SR PU/PD, SMT	DRAM data 17 / Videoin Data PortA 1
147	RD16	Inout 2~16MA, SR PU/PD, SMT	DRAM data 16 / Videoin Data PortA 0
148	ABCK	Output 4MA	Audio bit clock
149	ALRCK	Inout 4MA, PD, SMT	(1) Audio left/right channel clock (2) Trap value in power-on reset : 1 : use external 373 0: use internal 373
150	DVDD3	Power	3.3V power pin for internal digital circuitry
151	ACLK	Inout 4MA	Audio DAC master clock (384/256 audio sample frequency)
152	MC_DATA	Input	Microphone serial input
153	SPDIF	Output 2~16MA, SR : ON/OFF	SPDIF output
154	ASDATA0	Inout 4MA PD SMT	(1) Audio serial data 0 (left/right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
155	ASDATA1	Inout 4MA PD SMT	(1) Audio serial data 1 (surround left/surround right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
156	ASDATA2	Inout 4MA PD SMT	(1) Audio serial data 2 (center/left channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation

Pin Number	Symbol	Type	Description
157	ASDATA3	Inout 4MA PD SMT	(1) Audio serial data 3 (surround left/surround right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation OR Videoin Data PortB 1
158	ASDATA4	Inout 4MA PD SMT	(1) Audio serial data 4 (center/left channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation OR Videoin Data PortB 2
159	DACVDDC	Power	3.3V power pin for VIDEO DAC circuitry
160	VREF	Analog input	Bandgap reference voltage
161	FS	Analog output	Full scale adjustment
162	YUV0/CIN	Output 4MA, SR	Video data output bit 0 / Compensation capacitor
163	DACVSSC	Ground	Ground pin for VIDEO DAC circuitry
164	YUV1/C	Output 4MA, SR	Video data output bit 1 / Analog chroma output
165	DACVDDB	Power	3.3V power pin for VIDEO DAC circuitry
166	YUV2/Y	Output 4MA, SR	Video data output bit 2 / Analog Y output
167	DACVSSB	Ground	Ground pin for VIDEO DAC circuitry
168	YUV3/CVBS	Output 4MA, SR	Video data output bit 3 / Analog composite output
169	DACVDDA	Power	3.3V power pin for VIDEO DAC circuitry
170	YUV4/G	Output 4MA, SR	Video data output bit 4 / Green or Y
171	DACVSSA	Ground	Ground pin for VIDEO DAC circuitry
172	YUV5/B	Output 4MA, SR	Video data output bit 5 / Blue or CB
173	YUV6/R	Output 4MA, SR	Video data output bit 6 / Red or CR
174	ICE	Input PD, SMT	Microcontroller ICE mode enable
175	BLANK#	Inout 4MA, SR SMT	Video blank area, active low / Videoin Field_601
176	VSYN	Inout 4MA, SR SMT	Vertical sync / Videoin Vsync_601
177	YUV7	Inout 4MA, SR SMT	Video data output bit 7 / Videoin Data PortB 3
178	DVSS	Ground	Ground pin for internal digital circuitry
179	HSYN	Inout 4MA, SR SMT	Horizontal sync / Videoin Hsync_601
180	SPMCLK	Input	Audio DAC master clock of SPDIF input / Videoin Data PortB 4

Pin Number	Symbol	Type	Description
181	SPDATA	Input	Audio data of SPDIF input / Videoin Data PortB 5
182	DVDD2	Power	2.5V power pin for internal digital circuitry
183	SPLRCK	Input	Audio left/right channel clock of SPDIF input / Videoin Data PortB 6
184	SPBCK	Input	Audio bit clock of SPDIF input / Videoin Data PortB 7
185	DVDD3	Power	3.3V power pin for internal digital circuitry
186	XTALO	Output	Crystal output
187	XTALI	Input	Crystal input
188	PRST	Input PD, SMT	Power on reset input, active high
189	DVSS	Ground	Ground pin for internal digital circuitry
190	VFO13	Output	The 1st, 3rd header VFO pulse output
191	IDGATE	Output	Header detect signal output
192	DVDD3	Power	3.3V power pin for internal digital circuitry
193	UDGATE	Output	DVD_RAM recording data gate signal output
194	WOBSI	Input	Wobble signal input
195	SDATA	Output	RF serial data output
196	SDEN	Output	RF serial data latch enable
197	SLCK	Output	RF serial clock output
198	BDO	Input	Flag of defect data input status
199	ADCVSS	Ground	Ground pin for ADC circuitry
200	ADIN	Analog Input	General A/D input
201	RFSUBI	Analog Input	RF subtraction signal input terminal
202	TEZISLV	Analog Input	Tracking error zero crossing low pass input
203	TEI	Analog Input	Tracking error input
204	CSO	Analog Input	Central servo input
205	FEI	Analog Input	Focus error input
206	RFLEVEL	Analog Input	Sub beam add input or RFRP low pass input
207	RFRP_DC	A Input	RF ripple detect input
208	RFRP_AC	Analog Input	RF ripple detect input (through AC coupling)
209	HRFZC	Analog Input	High frequency RF ripple zero crossing
210	PWMVREF	A Input	A reference voltage input for PWM circuitry. A typical value of 4.0 v
211	PWM2VREF	A Input	A reference voltage input for PWM circuitry. A typical value of 2.0 v
212	ADCVDD3	Power	3.3V power pin for ADC circuitry
213	RFDTSLVP	Analog Output	Positive RF data slicer level output
214	RFDTSLVN	Analog Output	Negative RF data slicer level output
215	RFIN	Analog Input	Negative input of RF differential signal
216	RFIP	Analog Input	Positive input of RF differential signal

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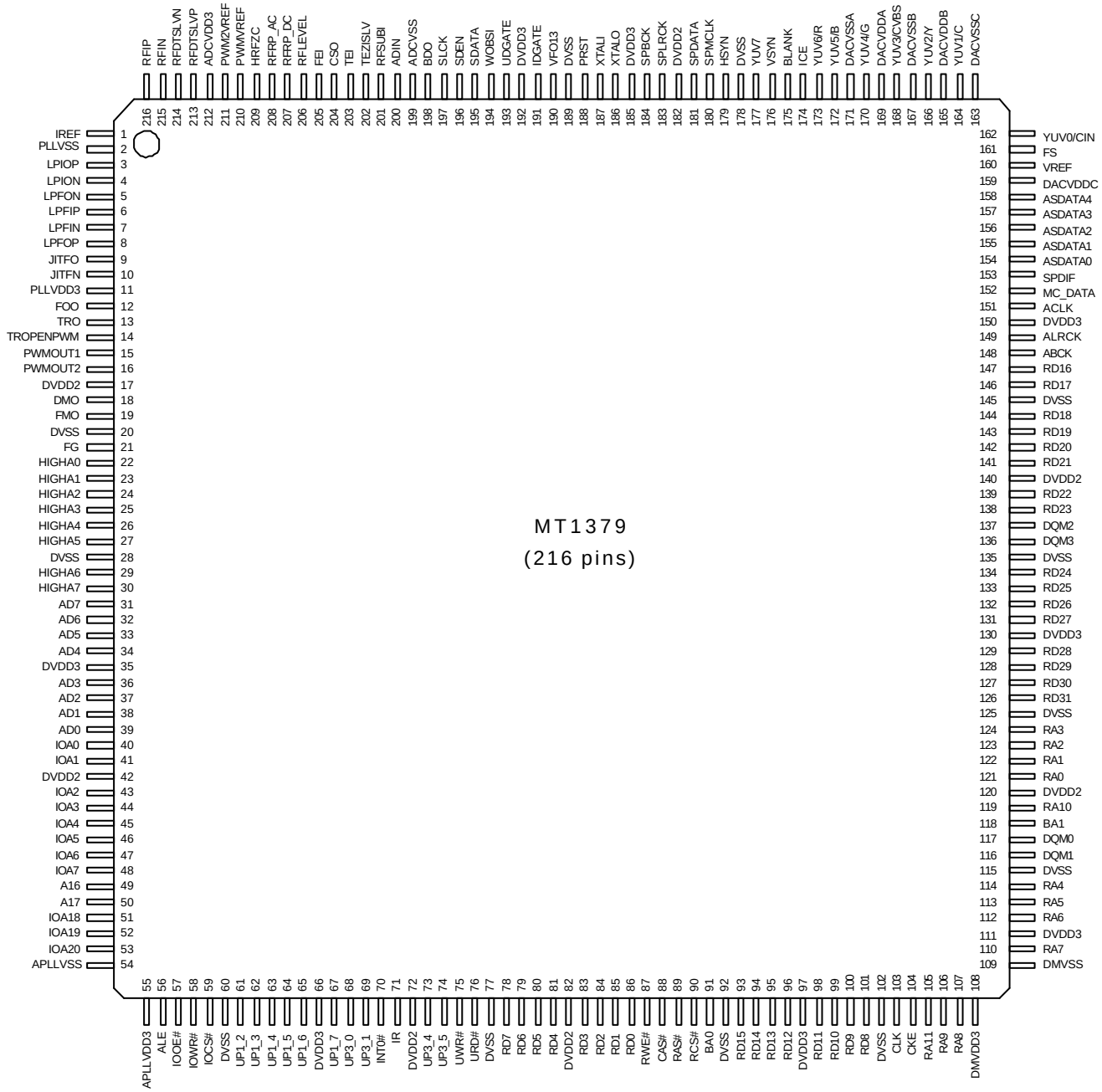
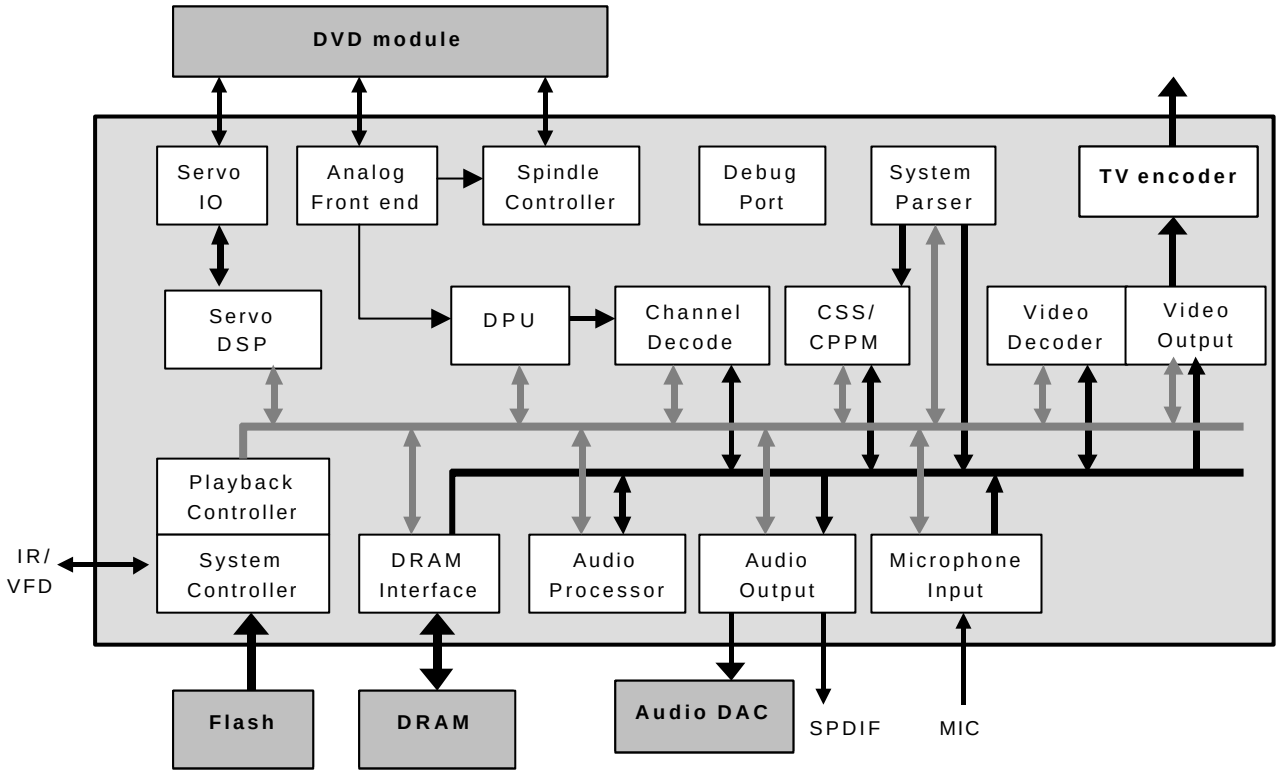


FUNCTIONAL BLOCK



Servo Controller

The servo control is accomplished through the servo DSP (Servo Digital Signal Processor) and its accessory I/O circuits. This servo DSP is capable of performing complex operations and also provides a friendly interface for the system controller. By issuing type 1 and type 2 commands from the system controller, the servo DSP can accomplish various complicated servo control functions, such as tracking, seeking and MT1336/MT1376 chip register programming. As for the servo I/O circuits, it provides interface between the input servo signals and the Servo DSP. It has built-in ADCs to digitize the servo control signal and DACs to provide signals for the actuator and sledge motor. It also has a serial interface to communicate with the MT1336/MT1376 chip.

Analog Front End

The analog front end contains a data slicer circuit and a data PLL circuit. The RF analog signal from MT1336/MT1376 is quantized by the data slicer to form the EFM/EFM+ bit stream, from which the channel bit clock is extracted by the data PLL.The EFM/EFM+bit stream and bit clock are then output to DPU for channel bit processing.

DPU

Data path unit (DPU) provides protection on data with lost synchronization patterns and demodulates EFM/EFM+ bit stream into the channel raw data that will be corrected by the decoder. The synchronization protection makes data after the synchronization pattern to be extracted even if the synchronization pattern is not found.

Spindle Controller

The spindle controller is used to control disc spindle motor. It includes a varipitch CLV clock generator, a CLV/CAV controller, and a PWM generator. The varipitch CLV clock enerator generates a reference colck for the speed of operation. The CLV/CAV

controller changes the mode and speed of operation according to servo register setting. The PWM generator generates pulse-width-modulated signal to drive disc spindle motor driver.

CSS/CPPM

The CSS/CPPM module provides functions necessary for decoding discs conforming to CSS/CPPM specification.

System Parser

The system parser is used to help the system controller to decode DVD/SVCD/VCD bitstream just after the channel decoder performing error correction. Acting as a DMA master, it moves bitstream data from RSPC buffer to video, audio, or sub-picture buffer according to system controller request. It also decrypts the scramble data of the CSS/CPPM sectors. Another function of system parser is providing system controller/DSP a DRAM memory copy controller to enhance system controller/DSP performance.

Video Decoder

The primary function of MT1379 is to support MPEG1 and MPEG2 video decoding. The video decode engine comprises of variable length decoder (VLD), inverse transformer (IT), motion compensator (MC), and block reconst ructor (BR). The video decode engine decodes the variable length encoded symbols in MPEG bitstream and performs inverse scan, inverse quantization, mismatch control and inverse discrete cosine transform onto the variable length decoded data. The motion compensator fetches prediction data from reference picture buffer according to motion vectors and motion prediciton mode for P and B pictures. Finally, the block reconstructor combines both the results of inverse transformer and motion compensator to derive the reconstructed image macroblock and write back to picture buffer.

The video decode engine can also support JPEG and BMP file decoding by common image compression hardware kernels.

Video Output

The Video Output unit contains Video Processor, SPU, OSD, Cursor, TV encoder units, it performs

- Reading decoded video from DRAM buffer
- Scaling the image
- Gamma/Brightness/Hue/Saturation adjustment and edge enhancement
- Reading and decoding SPU and OSD data from DRAM buffer
- Generating hardware cursor image
- Merging the video data, SPU, OSD and cursor

Video Processor

The Video Processor unit controls the transfer of video data stored in the DRAM to an internal or external TV encoder. It uses FIFOs to buffer outgoing luminance and chrominance data, and performs YUV420 to YUV422 conversion and arbitrary vertical/horizontal decimation/interpolation, from 1/4x to 256x. With this arbitrary ratio scaling capability, the Video Processor can perform arbitrary image conversion, such as PAL to NTSC, NTSC to PAL, MPEG1 to MPEG2, Letterbox, Pan-Scan conversion or zoom in, zoom out. It is also capible of interlace to progressive conversion.

The Video Processor unit performs the following functions:

- Requests and receives the decoded picture data from the picture buffer in external DRAM for display
- Resample vertical data to create 4:2:2 sample format
- Optionally performs vertical/horizontal resampling of both luminance and chrominance data
- Performs optional Gamma correction, luminance/chrominance adjustment, and edge enhancement

The Video Processor unit contains two 2-tap vertical filters for luminance and chrominance . These filters are used to interpolate and reposition luminance and chrominance line to improve picture quality. These filters are capble of generating up to eight, unique subline value between two consecutive scan lines. The generation of lines depends on the ratio between the height of the source image and the target image. In applications where DRAM bandwidth are critical the filters can be configured as simple line-repeating to reduce the DRAM bandwidth required.

The Video Processor unit integrates two separate horizontal postprocessing filter, a simple 2-tap linear horizontal filter and an 8-tap programmable filter. These filters are provided for scaling images horizontally along the scan line. These two filters is capable of generating up to eight, unique subpixel values between two consecutive pixels on a scan line. The generation of pixels depends on the ratio between the width of the source image and the target image.

SPU

This is a hardware sub-picture decoder. It decodes the compressed SPU image bitstream and CHG_COLCON commands according to SPU header information previously decoded by system controller. The SPU module also allows two SPU objects to be displayed at the same time. SPU image is blended with main video stream.

OSD

The OSD module can operate with 2/4/16/256 -color bitmap format (1/2/4/8 bits), and 16/256 color RLC format, all have 16 levels of transparency. In addition, it accepts an special WARP mode, which inserts one programmable RLC code in the bitmap to reduce the image size stored in DRAM. It also features automatic shadow/outline generation in 2-color mode, 2 Hilight areas, 1 ChangeColor area and 1 OSDVoid area. One OSD area can occupy the full or a partial screen, or multiple OSDs can occur in a screen at the same time, only if they don't occupy the same horizontal line. The output image is blended with the video-SPU mixed stream.

Cursor

A hardware cursor generator is integrated in Video Output Unit. The cursor image is a 32x32 4-color bitmap image, each colors are programmable. Cursor can be enlarged by 2 in both vertical and horizontal directions. Cursor image is multiplexed with video-SPU-OSD mixed stream.

Audio Interface

Audio interface consists of Audio Output Interface and Microphone Input Interface.

Audio Output Interface

The MT1379 can support up to 8 channel audio outputs. The output formats can be 16, 24, or 32-bit frames. Left alignment, right alignment, or I^2S formats are all supported.

With built-in PLL, MT1379 can provide the audio clock (ACLK) for external audio DAC at 384Fs, where Fs is usually 32KHz, 44.1KHz, 48KHz, 96KHz, or 192KHz. ACLK can also be programmed to be from outside MT1379. When ACLK is input to MT1379, the frequency could be 128**n* Fs, where *n* is from 1 to 7.

Audio raw (encoded) data or cooked (decoded) data can be output on a single line using S/PDIF interface. The output slew rate and driving force of this pad are programmable.

Microphone Input Interface

The MT1379 provides a microphone input interface. Two independent microphones' data could be input to the MT1379. There are two independent digital volume control for these two input channels. The input data formats can also be left alignment, right alignment, or I^2S formats.

System Controller

MT1379 uses an embedded Turbo-8032 as System Controller and provide ICE interface to increase the feasibility of F/W development. Also, MT1379 includes an build-in internal 373 to latch lower byte address from 8032 Port 0 and provide a glue-logic free solution. MT1379 supports up to 1M X 16 bits Flash ROM to store 8032 code, H/W related data, User data, etc. F/W upgrade can be achieved either by debug interface or by disk.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating

Symbol	Parameters	Value	Unit
VDD3	3.3V Supply voltage	-0.3 to 3.6	V
VDD2	2.5V Supply voltage	-0.3 to 3.0	V
VDDA	Analog Supply voltage	-0.3 to 3.6	V
V_{IN}	Input Voltage	-0.3 to 5.5	V
V_{OUT}	Output Voltage	-0.3 to VDD3+0.3	V
Ta	Ambient Temperature	0 to 70	°C

DC Charateristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{IH}	Input voltage high	2.4	-	3.6	V
V_{IL}	Input voltage low	-	-	0.8	V
V_{OH}	Output voltage high	3.0	-	VDD3	V
V_{OL}	Output voltage low	-	-	0.5	V
I_{IH}	High level input current			10	uA
I_{IL}	Low level input current	-10			uA
P_D	Power dissapation		1.0		W
P_{Down}	Power down mode			0.1	W

16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.23 µm process technology**
  - — Fully compatible with 0.32 µm Am29LV160B device
- **High performance**
  - — Access times as fast as 70 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 9 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Package option**
  - — 48-ball FBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **CFI (Common Flash Interface) compliant**
  - — Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

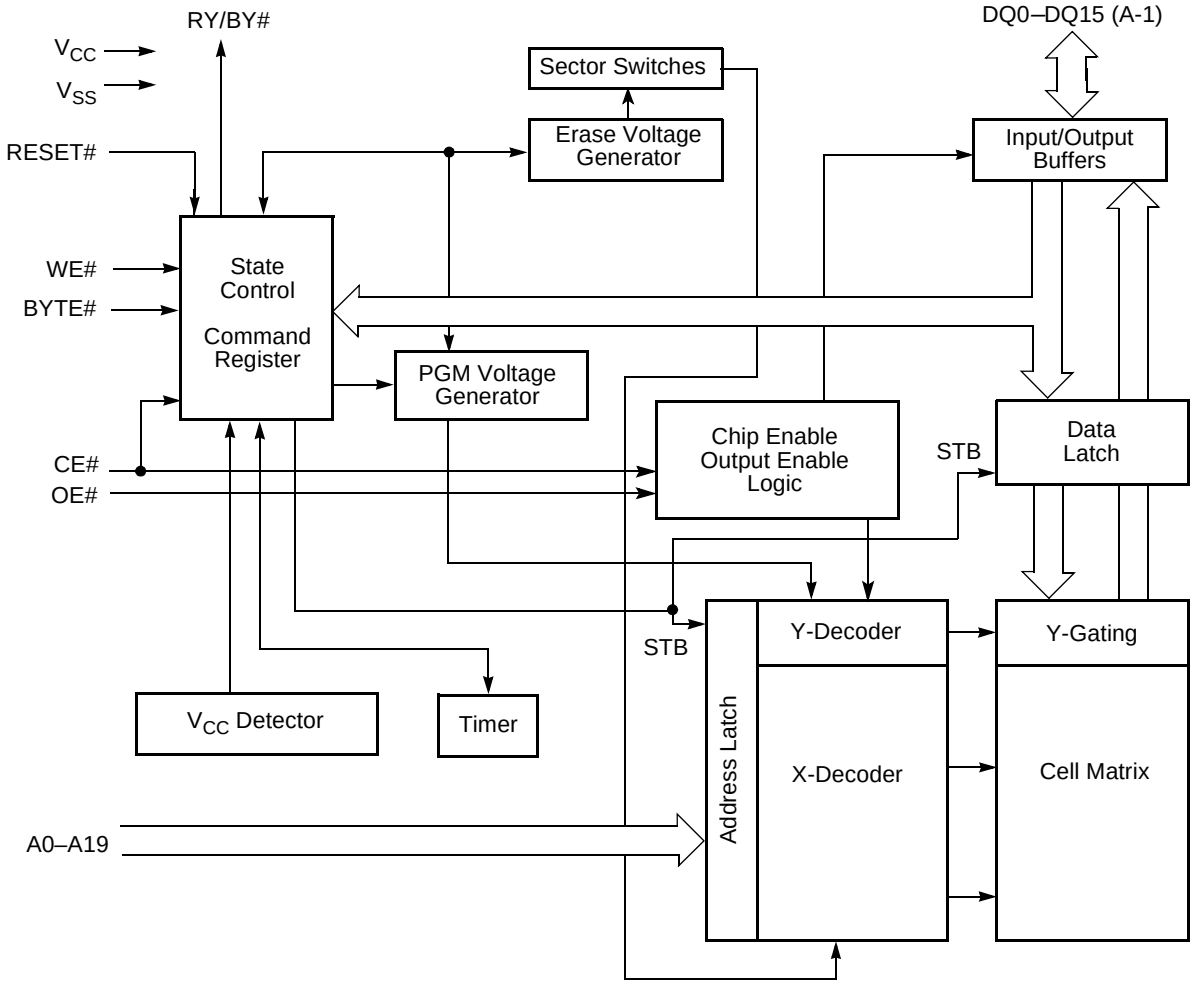
Publication# **22358** Rev: **B** Amendment/**+3**
Issue Date: **November 10, 2000**

PRODUCT SELECTOR GUIDE

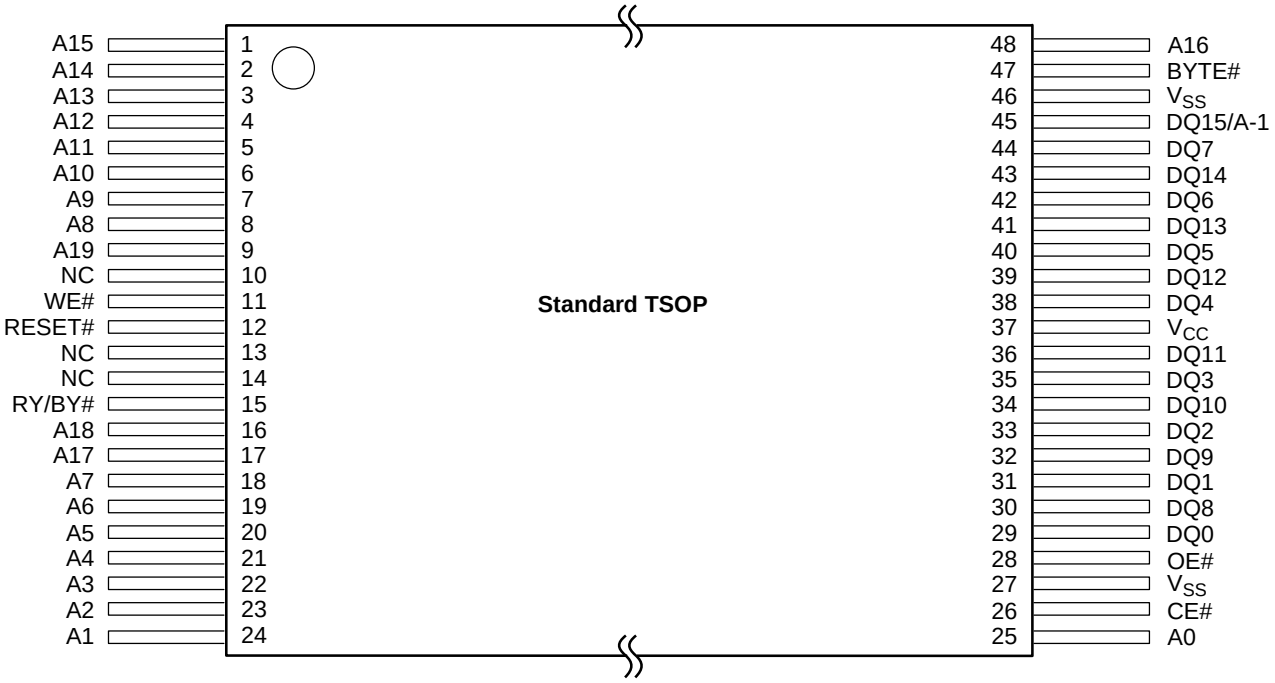
Family Part Number		Am29LV160D		
Speed Option	Voltage Range: V_{CC} = 2.7–3.6 V	**-70**	**-90**	**-120**
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	50

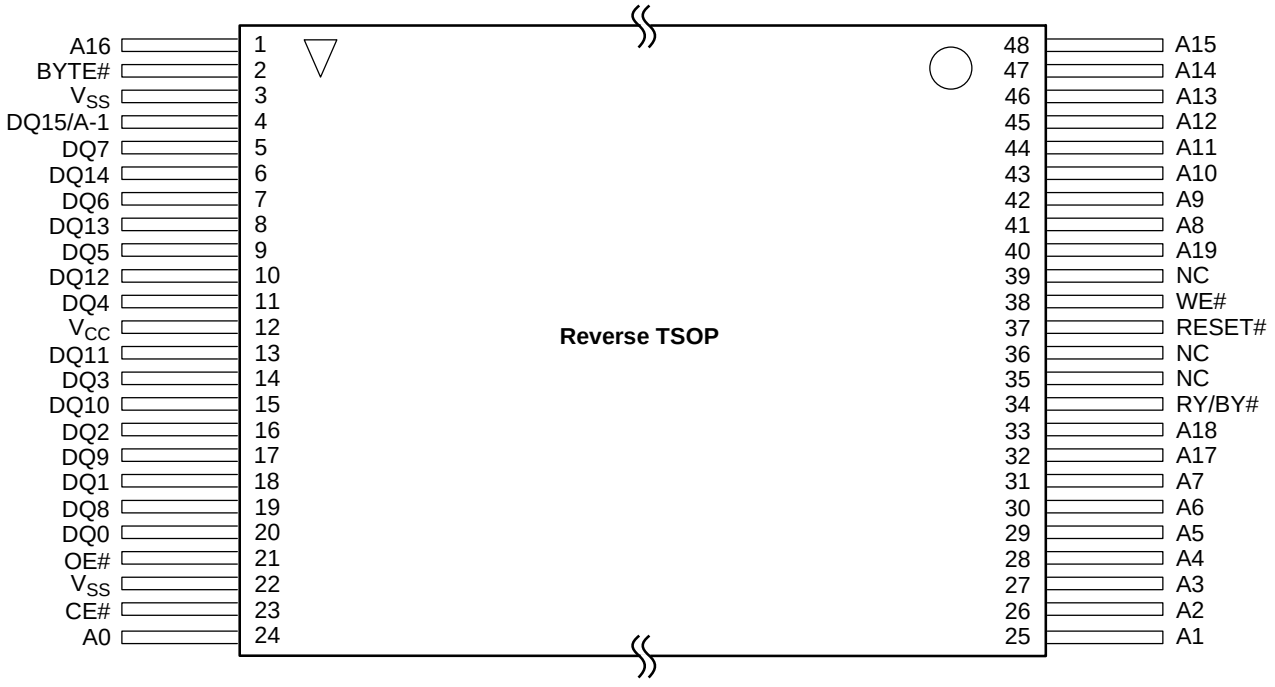
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM

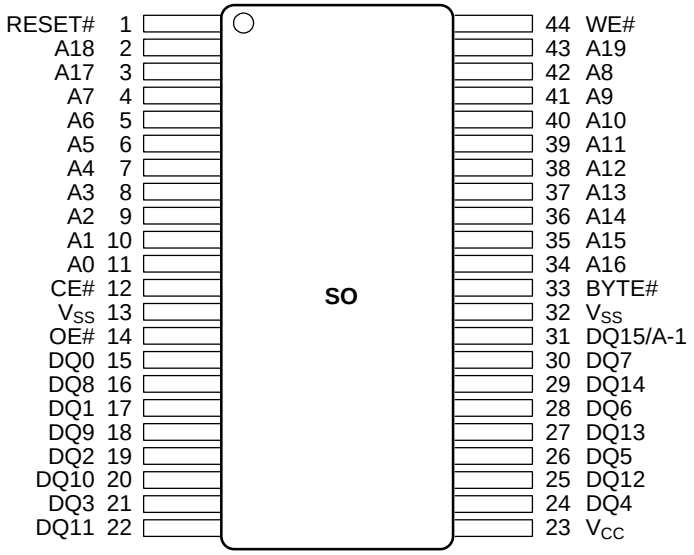


CONNECTION DIAGRAMS





CONNECTION DIAGRAMS



FBGA
Top View, Balls Facing Down

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	A19	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Special Handling Instructions

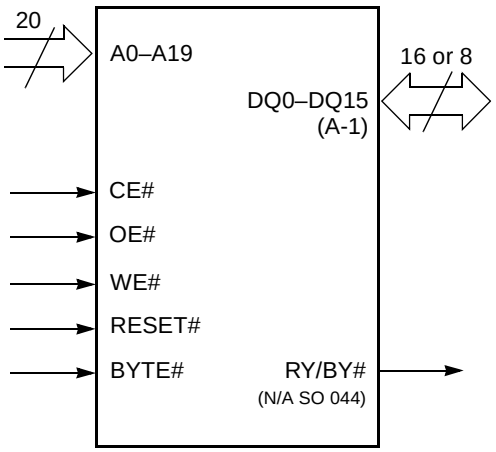
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A19	=	20 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output (N/A SO 044)
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



8.4 HY57V641620HG

DESCRIPTION

The Hyundai HY57V641620HG is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V641620HG is organized as 4banks of 1,048,576x16.

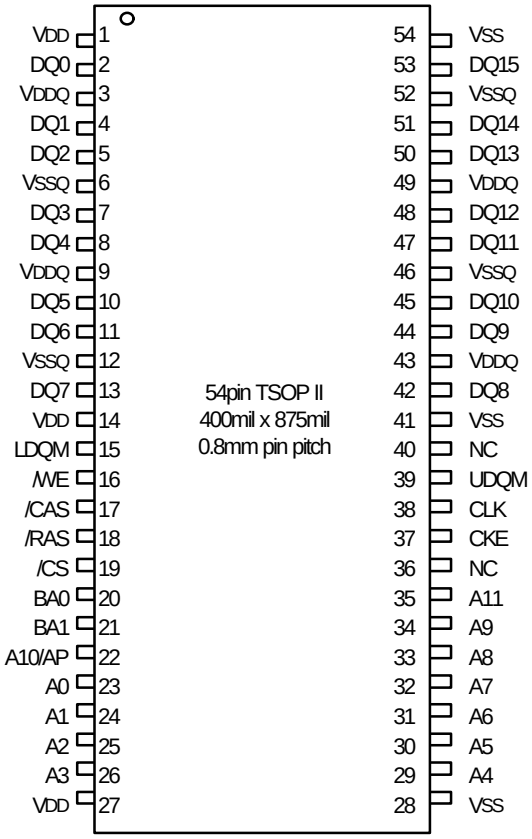
HY57V641620HG is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

- Single 3.3±0.3V power supply Note)
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

PIN CONFIGURATION

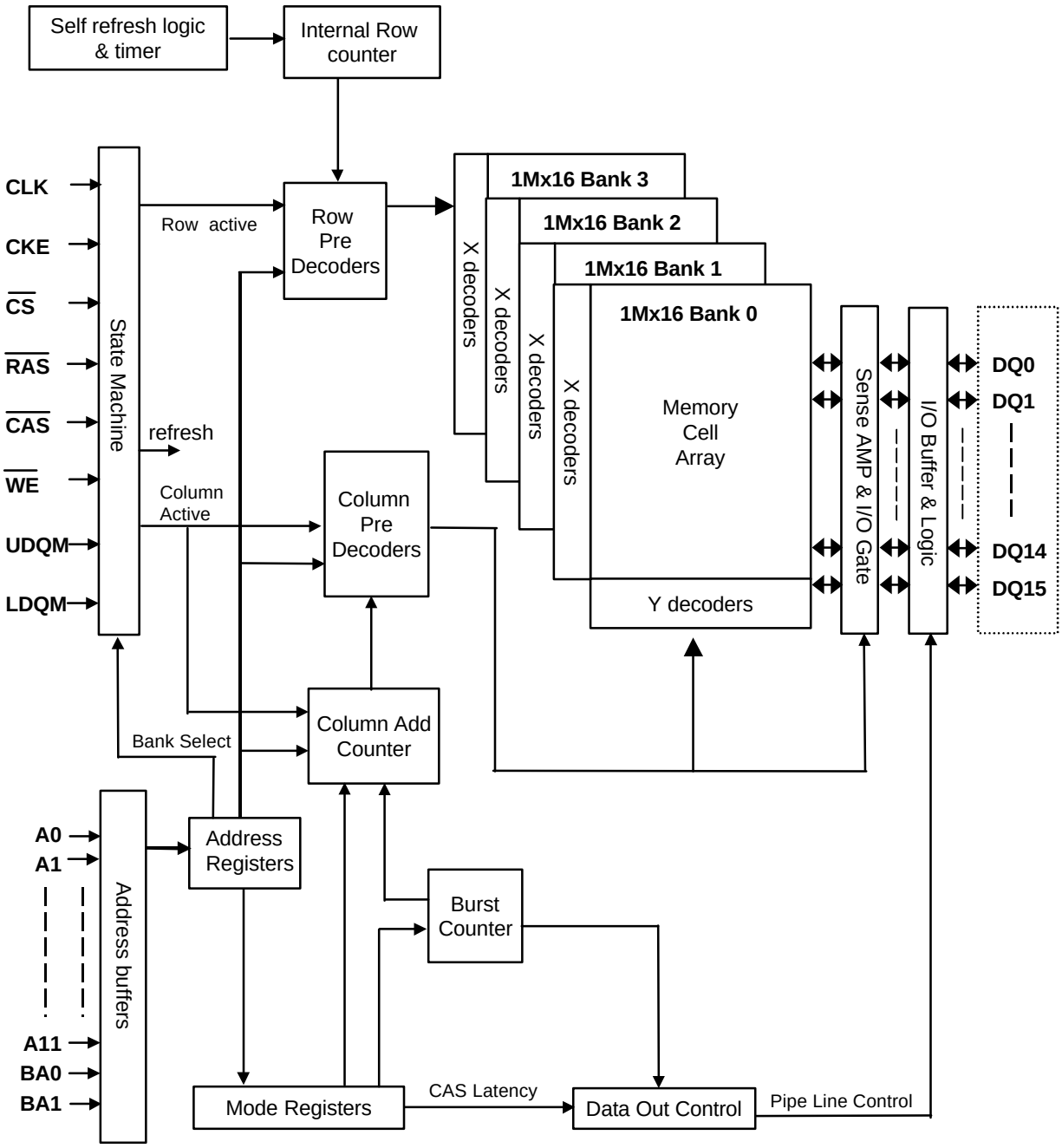


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



Data sheet acquired from Harris Semiconductor
SCHS047D

August 1998 - Revised March 2000

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to $20V_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic “1” is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the “CHANNEL IN/OUT” terminals are the outputs and the “COMMON OUT/IN” terminals are the inputs.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

Features

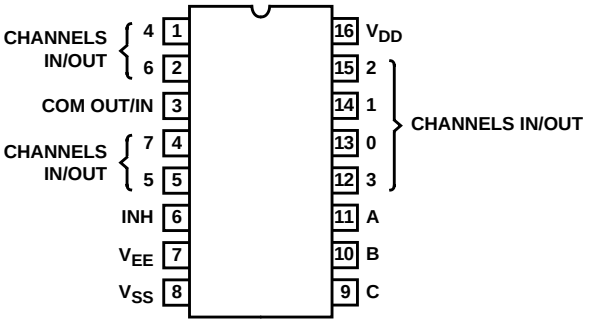
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . $\leq 20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25^oC
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

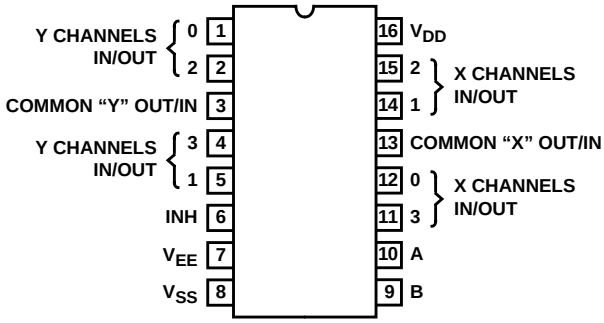
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Pinouts

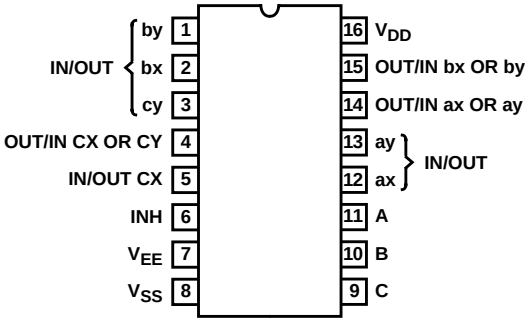
CD4051B (PDIP, CDIP, SOIC, TSSOP)
TOP VIEW



CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW

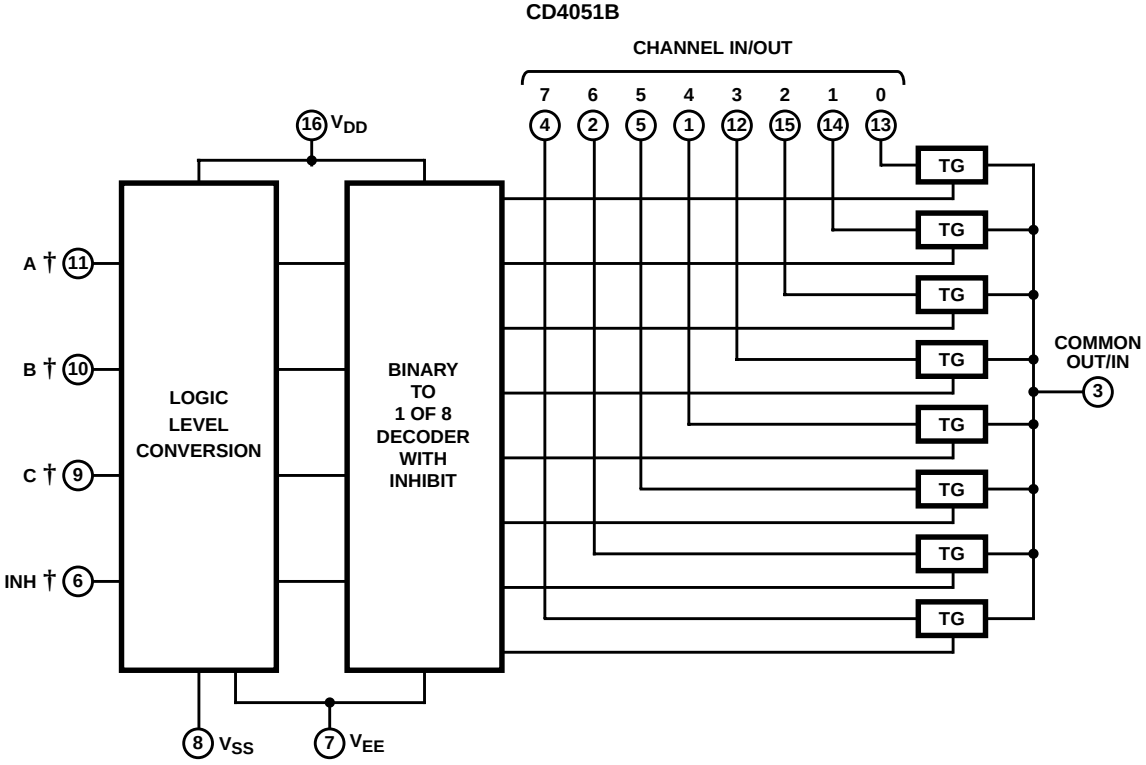


CD4053B (PDIP, CDIP, TSSOP)
TOP VIEW



Functional Block Diagrams

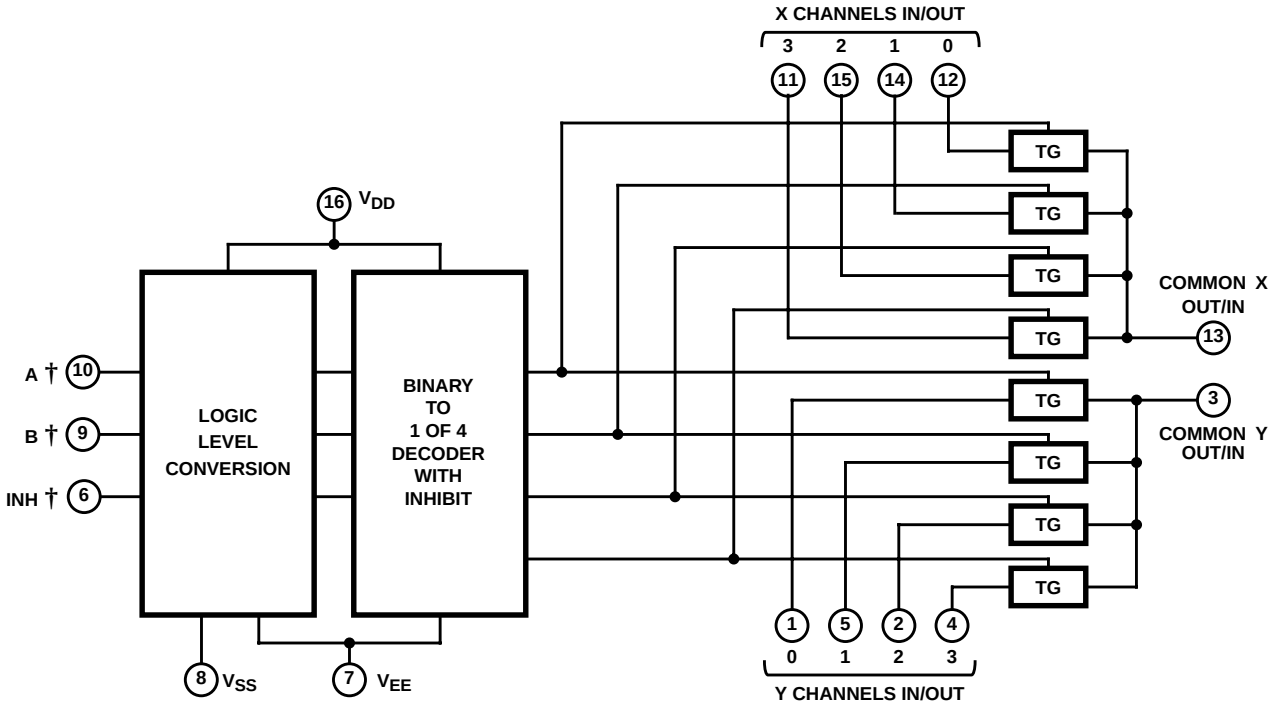
CD4051B



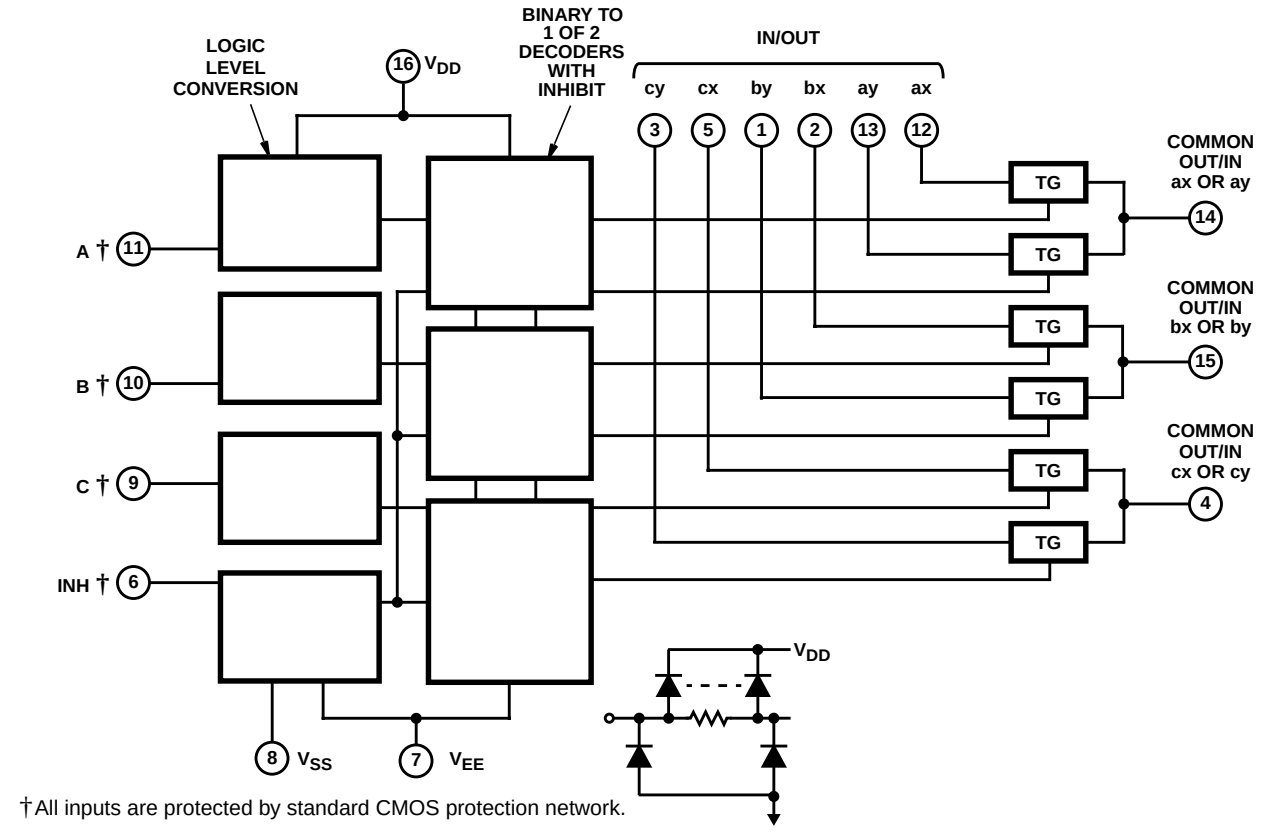
†All inputs are protected by standard CMOS protection network.

Functional Block Diagrams (Continued)

CD4052B



CD4053B



†All inputs are protected by standard CMOS protection network.

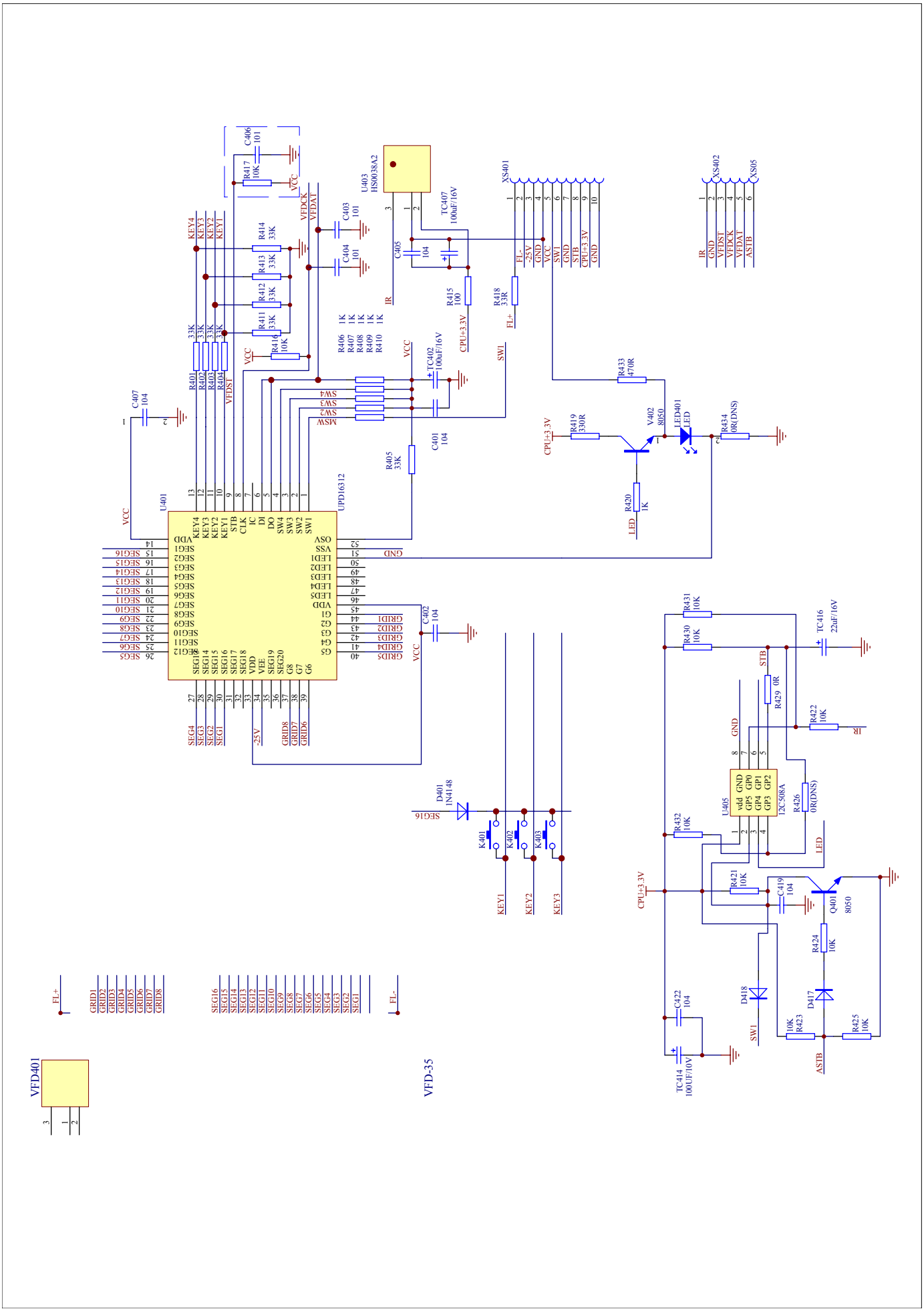
TRUTH TABLES

INPUT STATES				
INHIBIT	**C**	**B**	**A**	**“ON” CHANNEL(S)**
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
INHIBIT	**B**		**A**	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
CD4053B				
INHIBIT	**A OR B OR C**			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

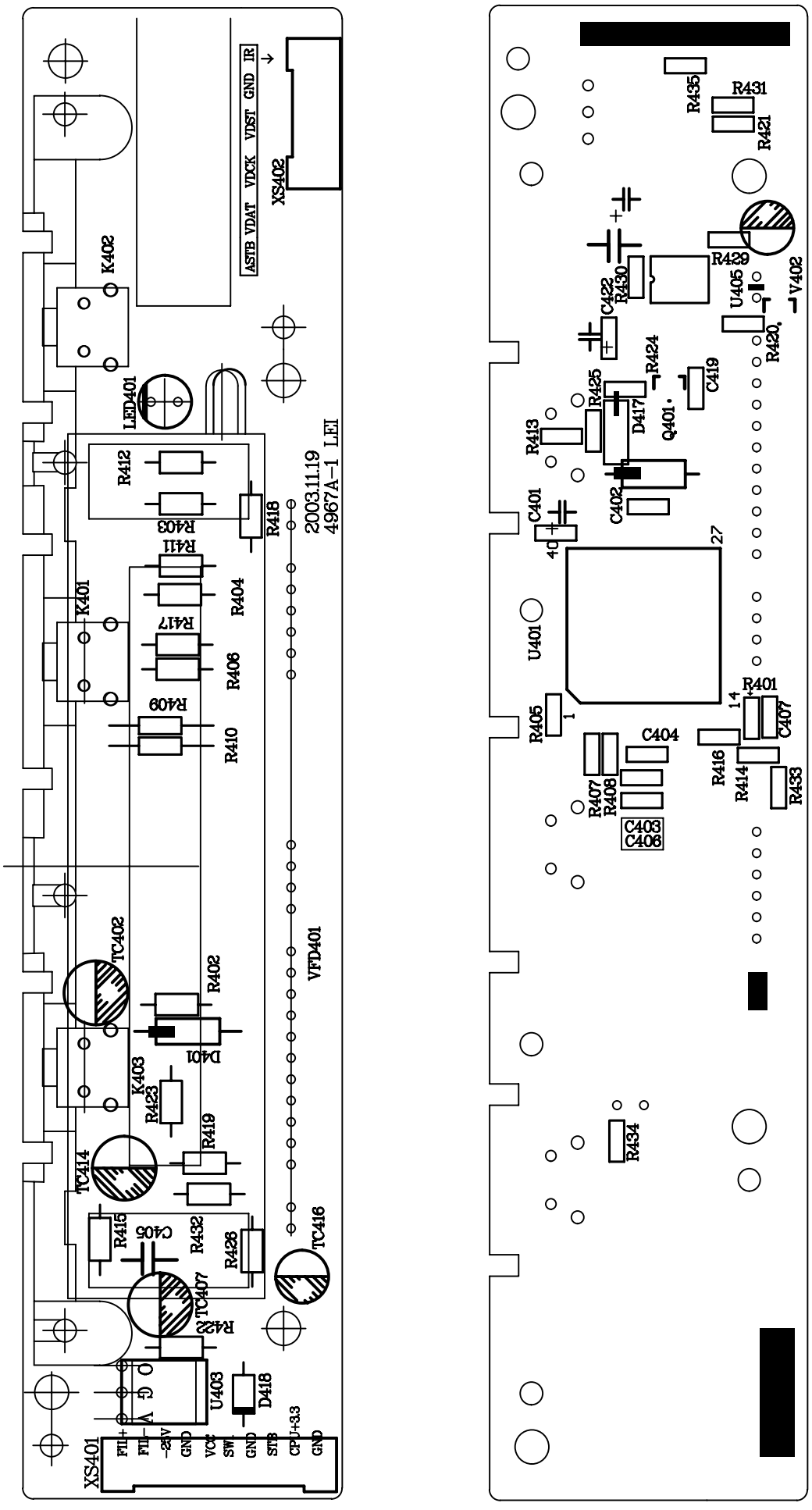
X = Don’t Care

9. SCHEMATIC & PCB WIRING DIAGRAM

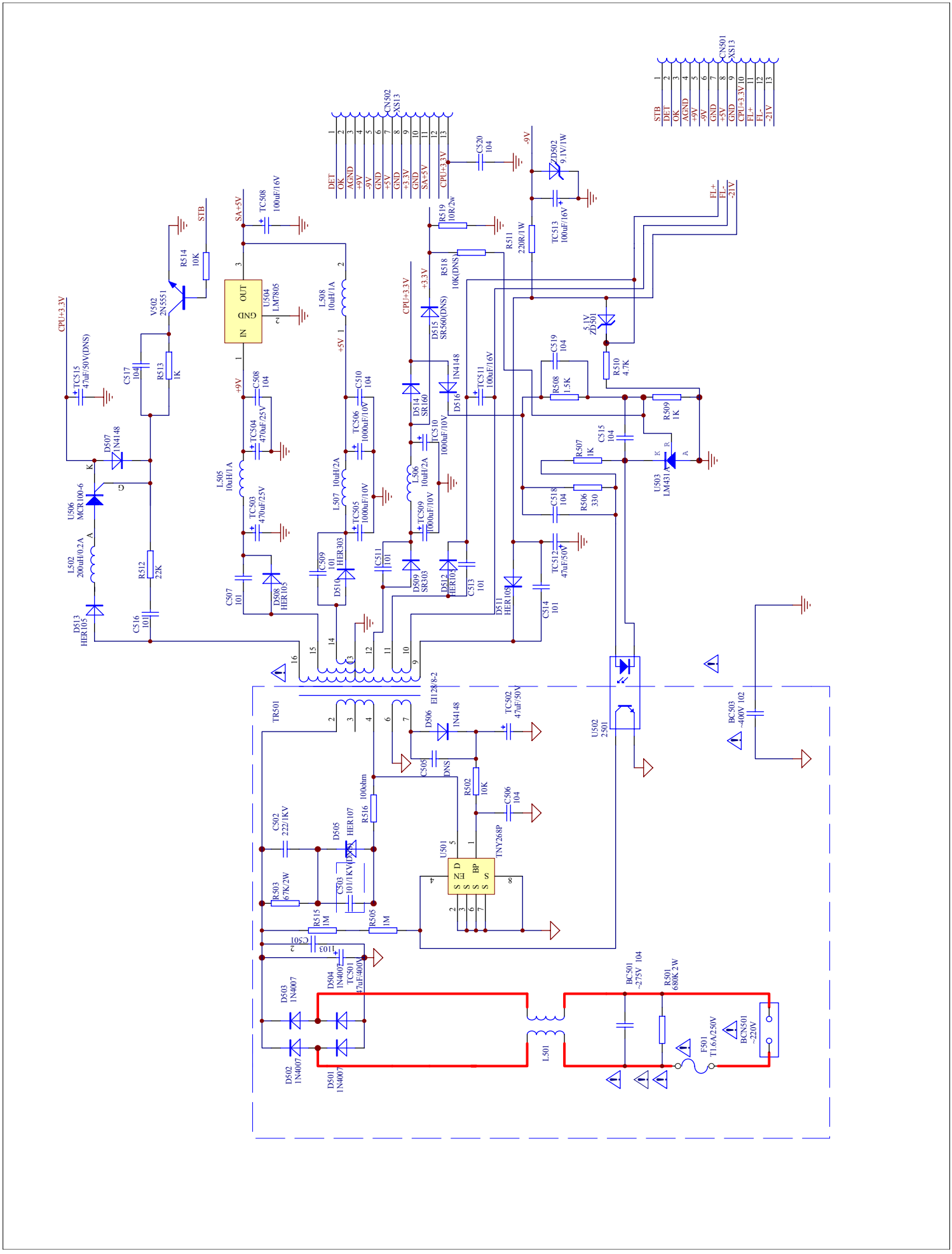
FRONT SCHEMATIC DIAGRAM



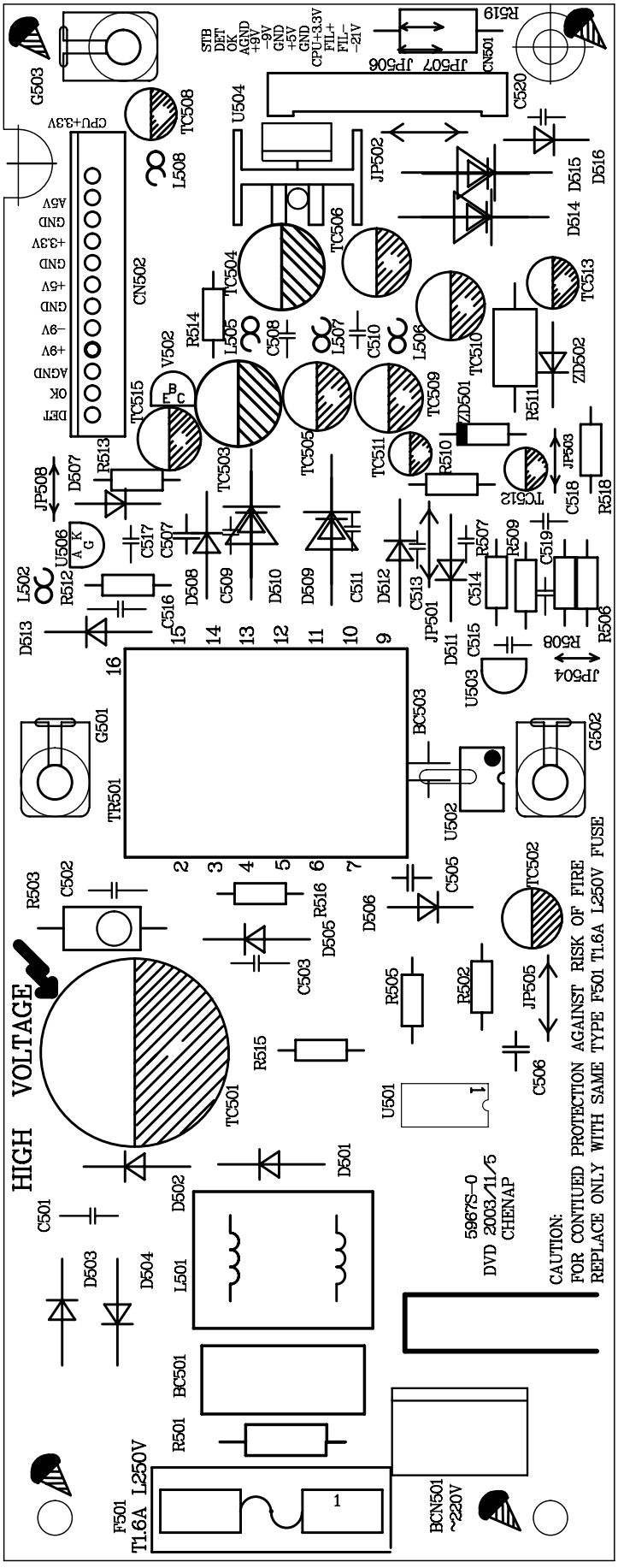
FRONT SCHEMATIC DIAGRAM



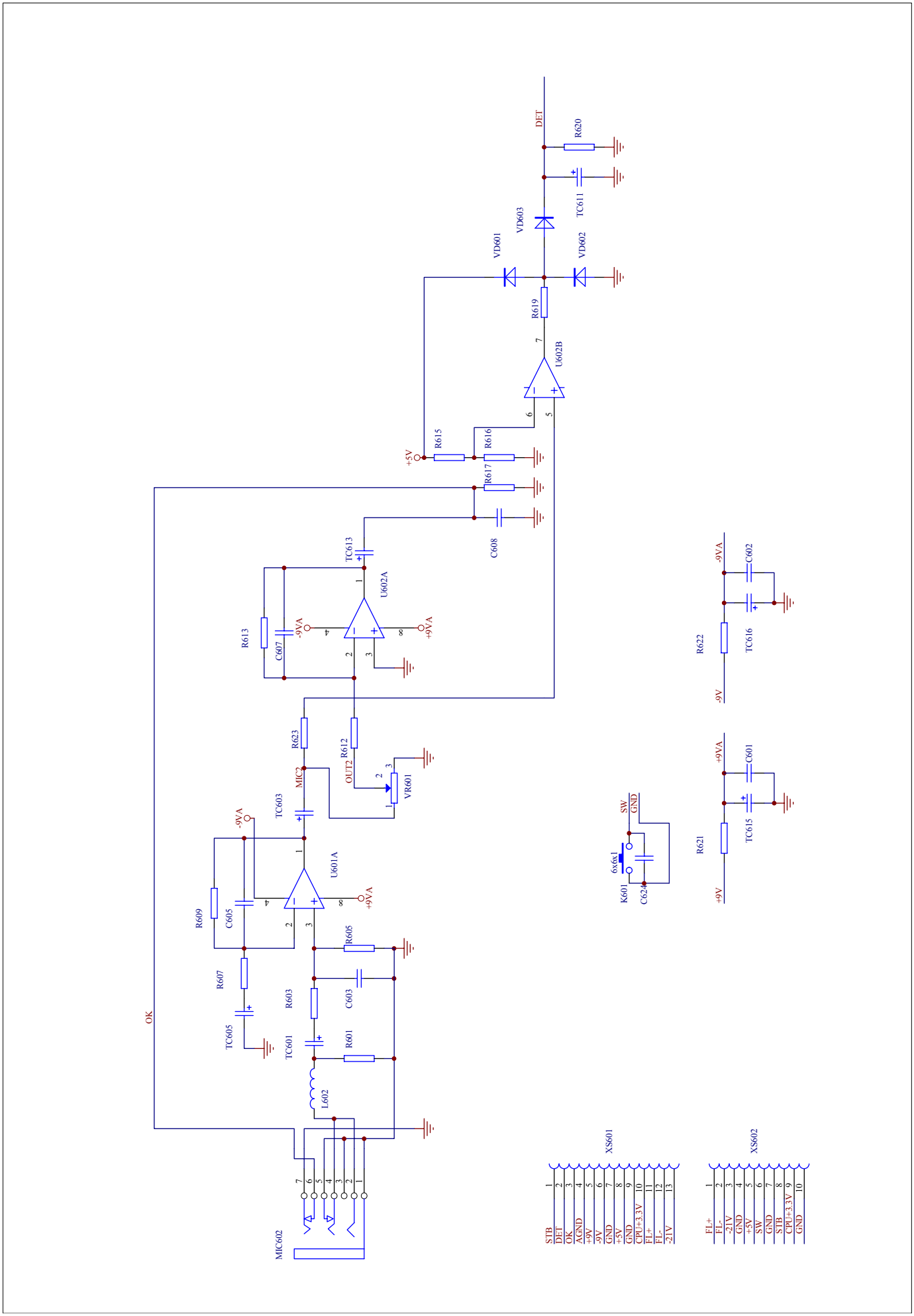
POWER BOARD SCHEMATIC DIAGRAM

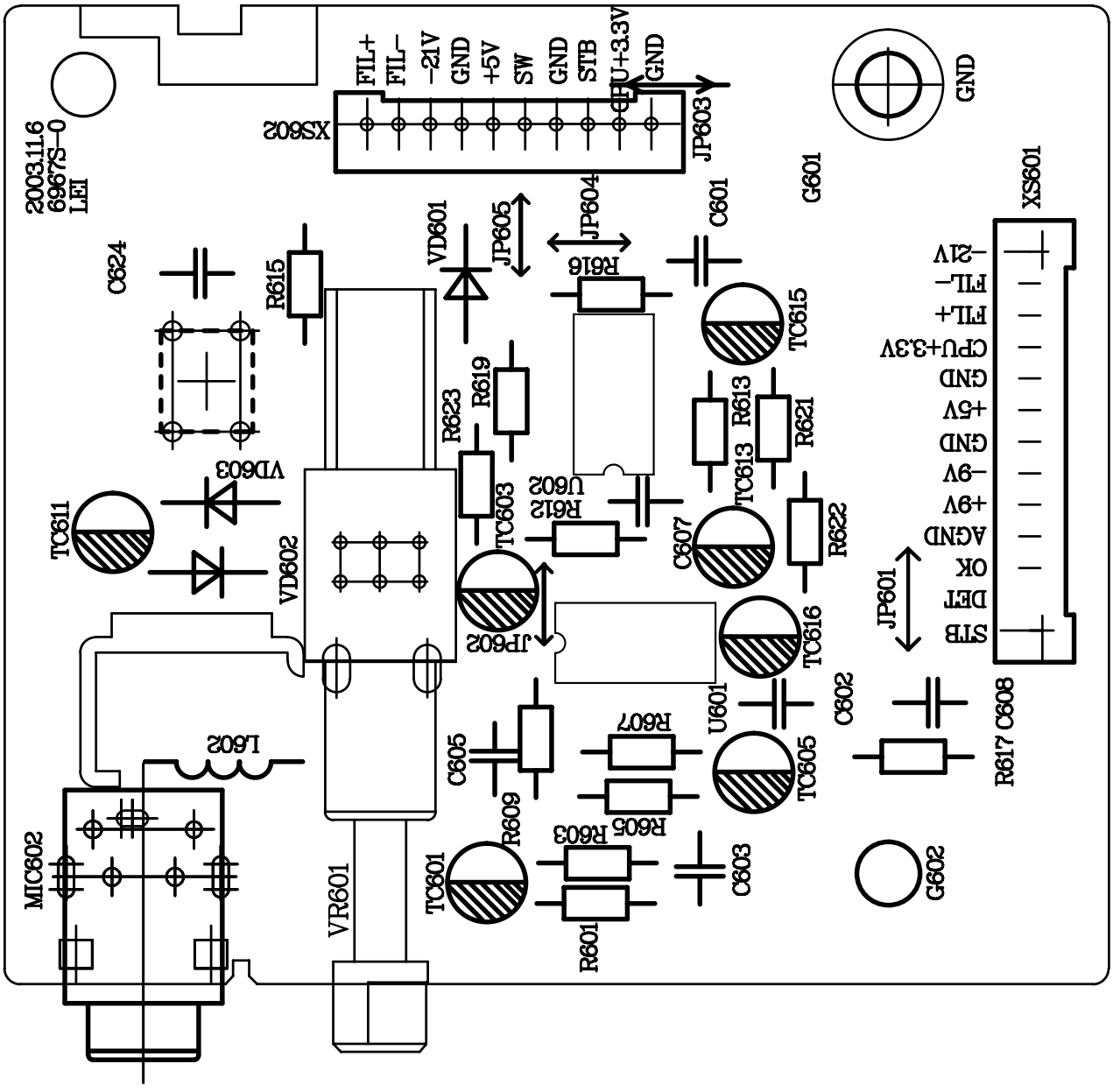


POWER BOARD SCHEMATIC DIAGRAM

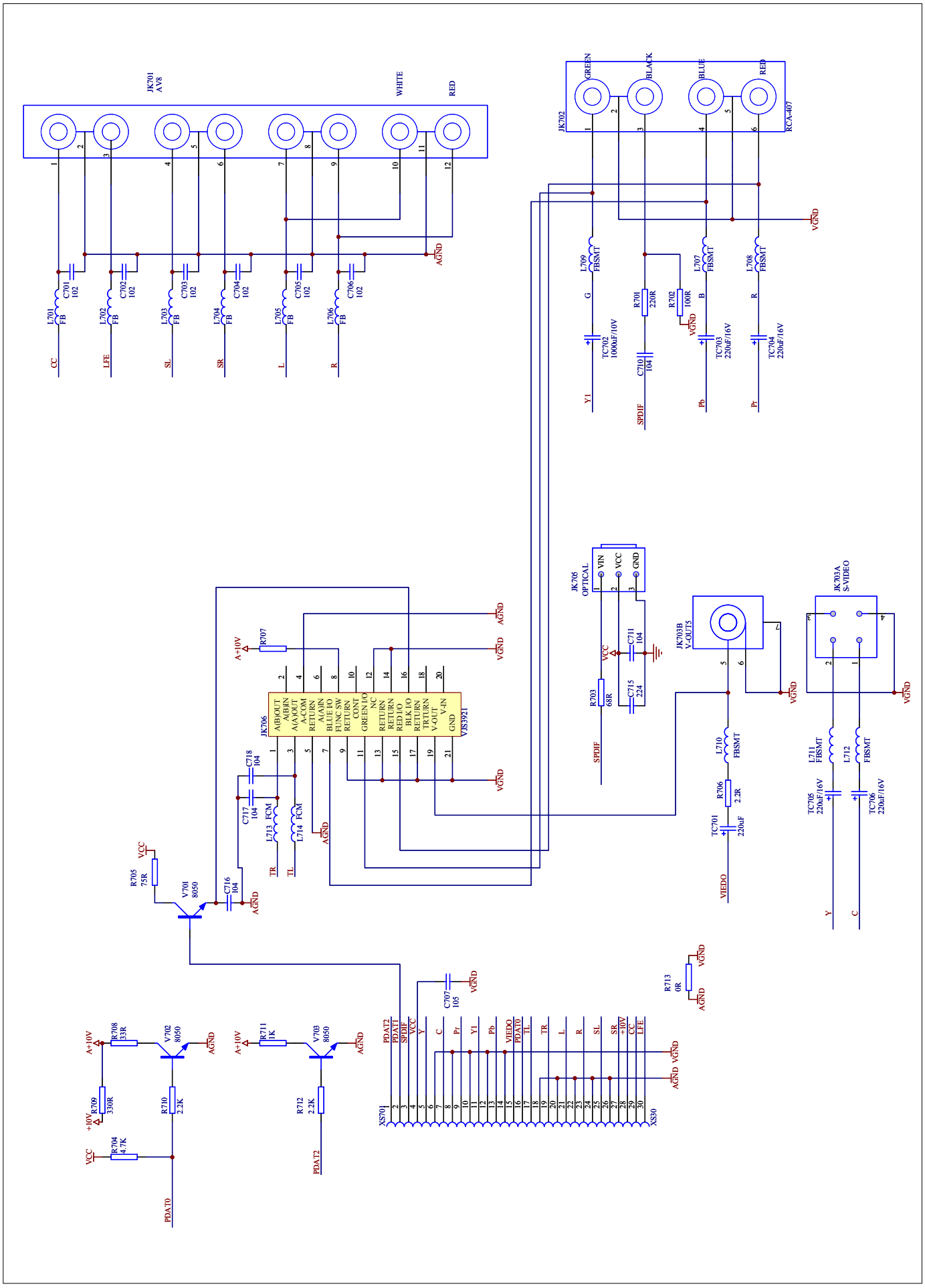


OK SCHEMATIC DIAGRAM

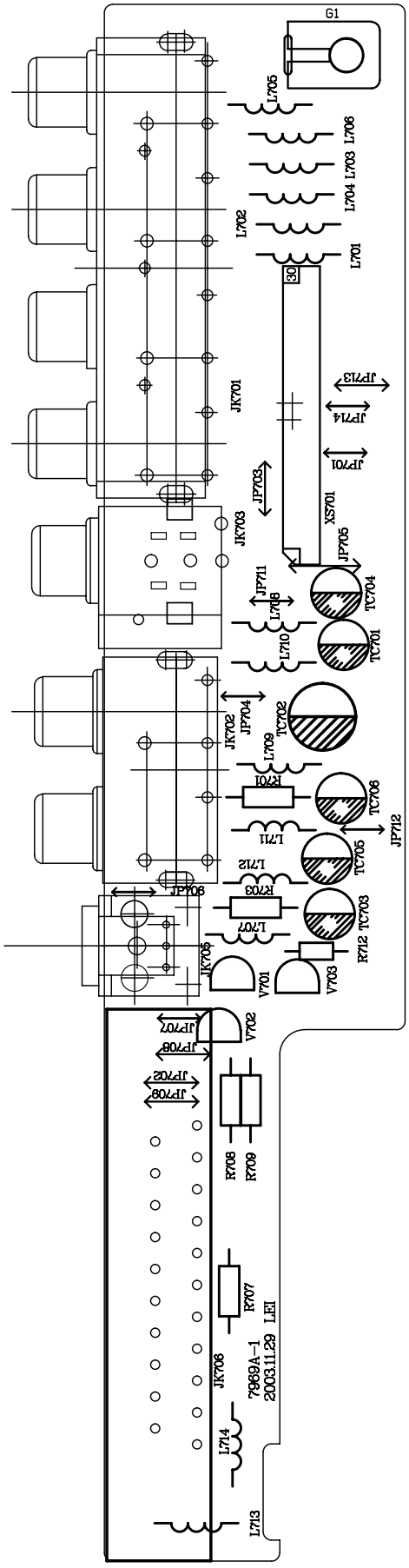



2003.11.6
6967S-0
LEI
XS602
FIL+
FIL-
-21V
GND
+5V
SW
GND
STB
CPU+3.3V
GND
JP603
GND
G601
XS601
-21V
FIL-
FIL+
CPU+3.3V
GND
+5V
GND
-9V
+9V
AGND
OK
DET
STB
JP601
C624
R615
VD601
JP605
JP604
R616
C601
TC615
R623
R619
R613
R621
VD603
TC611
VD602
TC603
R612
U602
TC613
C607
R622
JP602
TC616
U601
C602
C605
R607
TC605
R617
C608
L602
R609
R605
MIC602
TC601
R603
C603
G602
VR601
R601

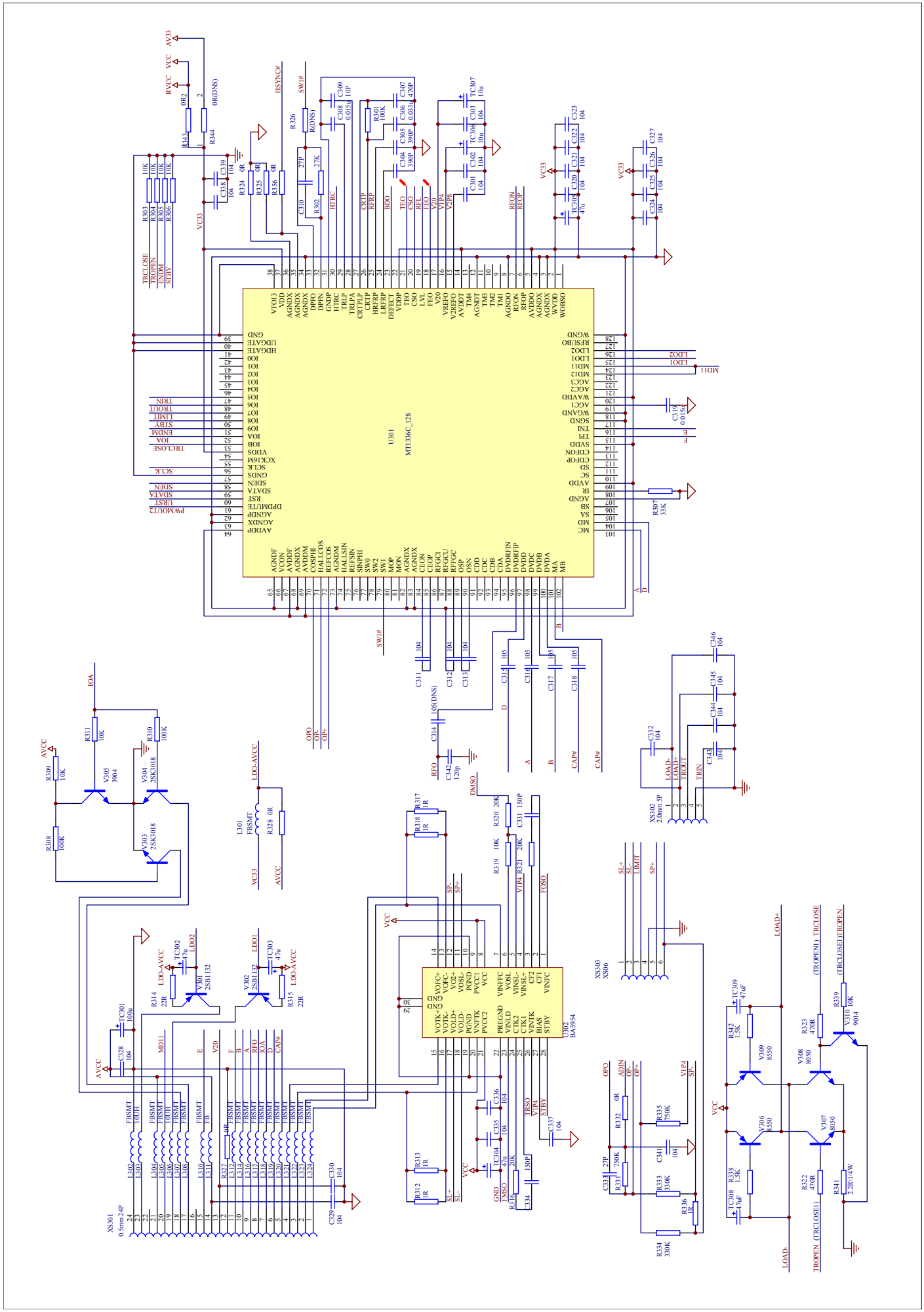
OUTPUT BOARD SCHEMATIC DIAGRAM



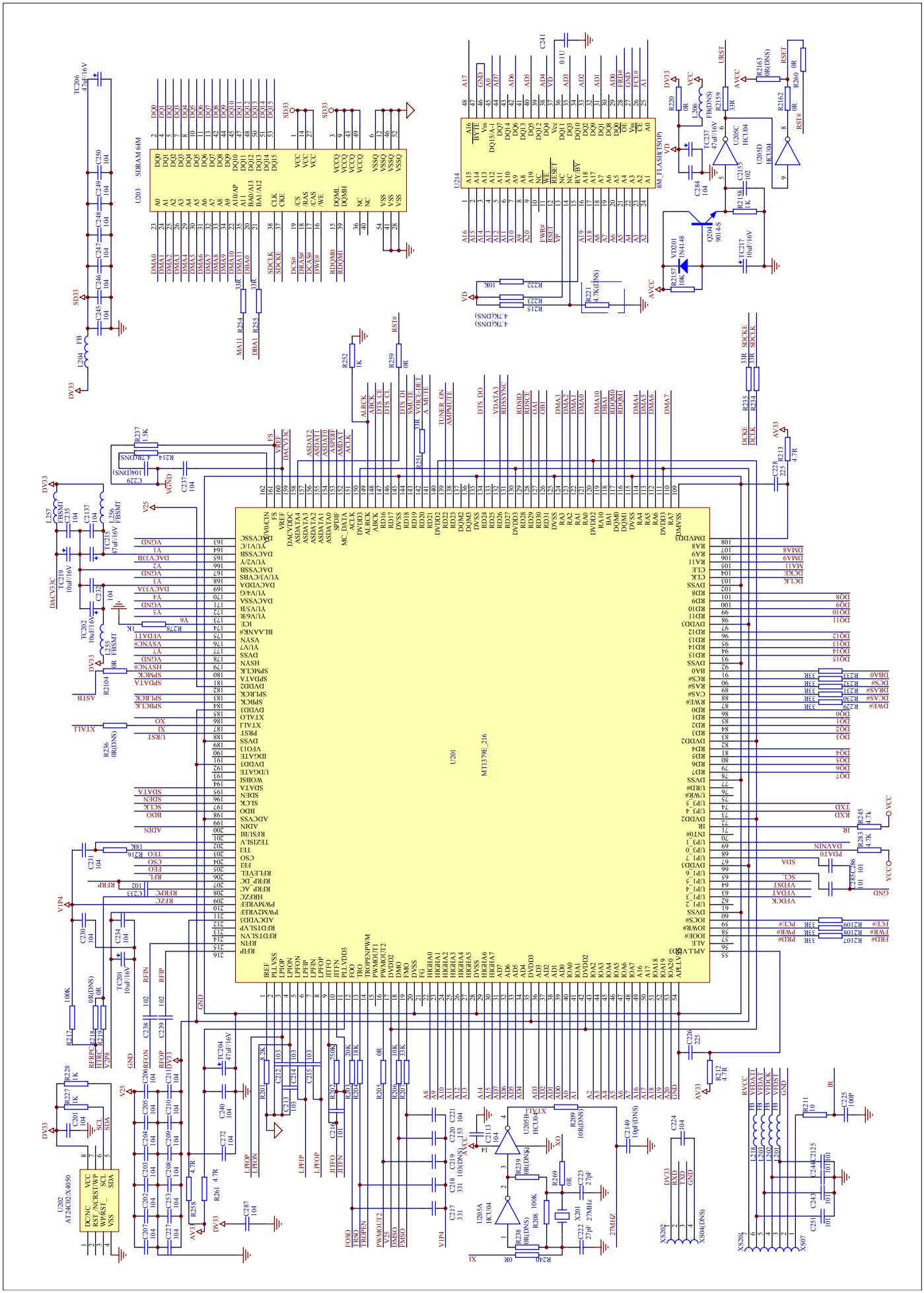
OUTPUT BOARD SCHEMATIC DIAGRAM



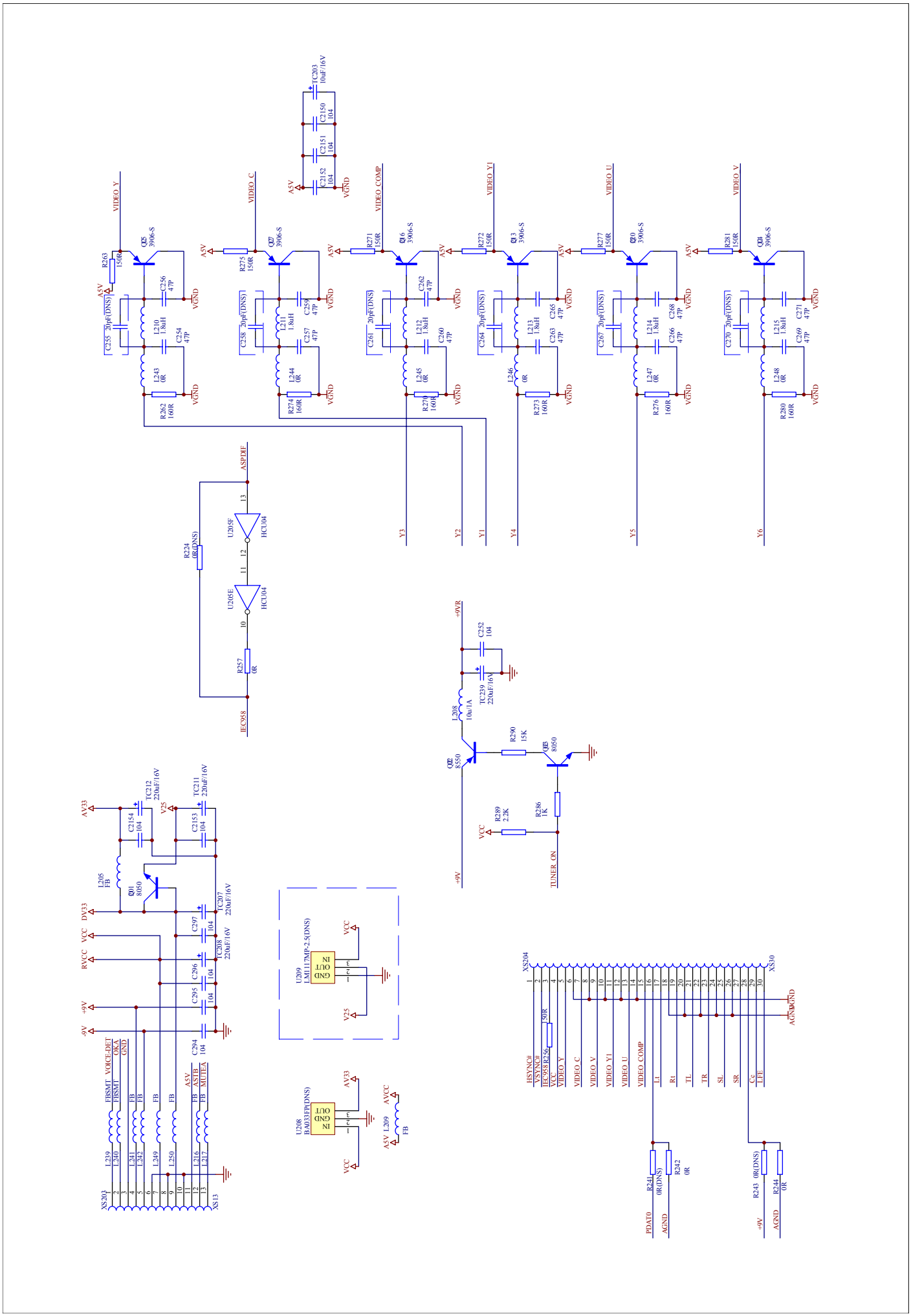
MIAN SCHEMATIC DIAGRAM



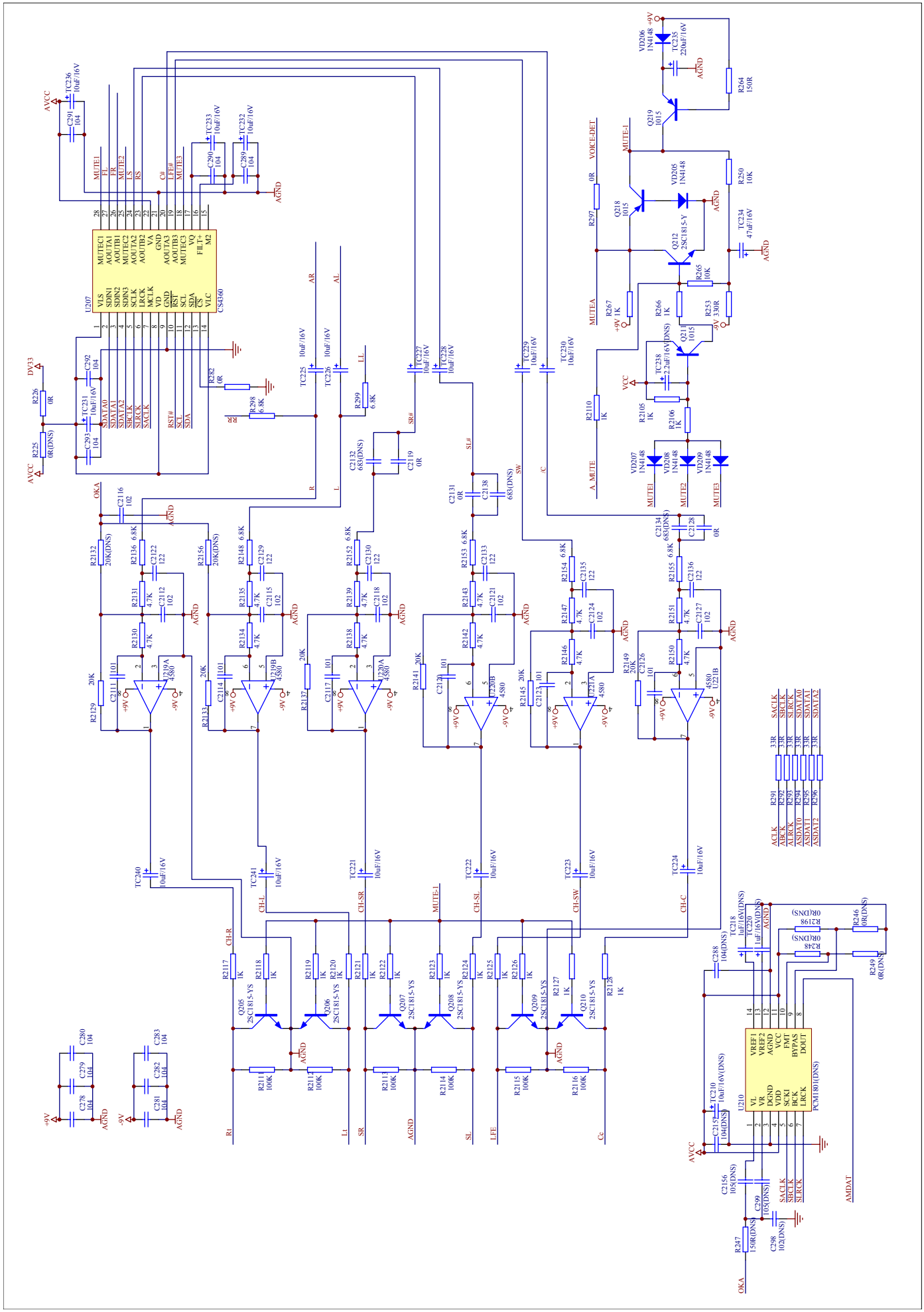
MIAN SCHEMATIC DIAGRAM



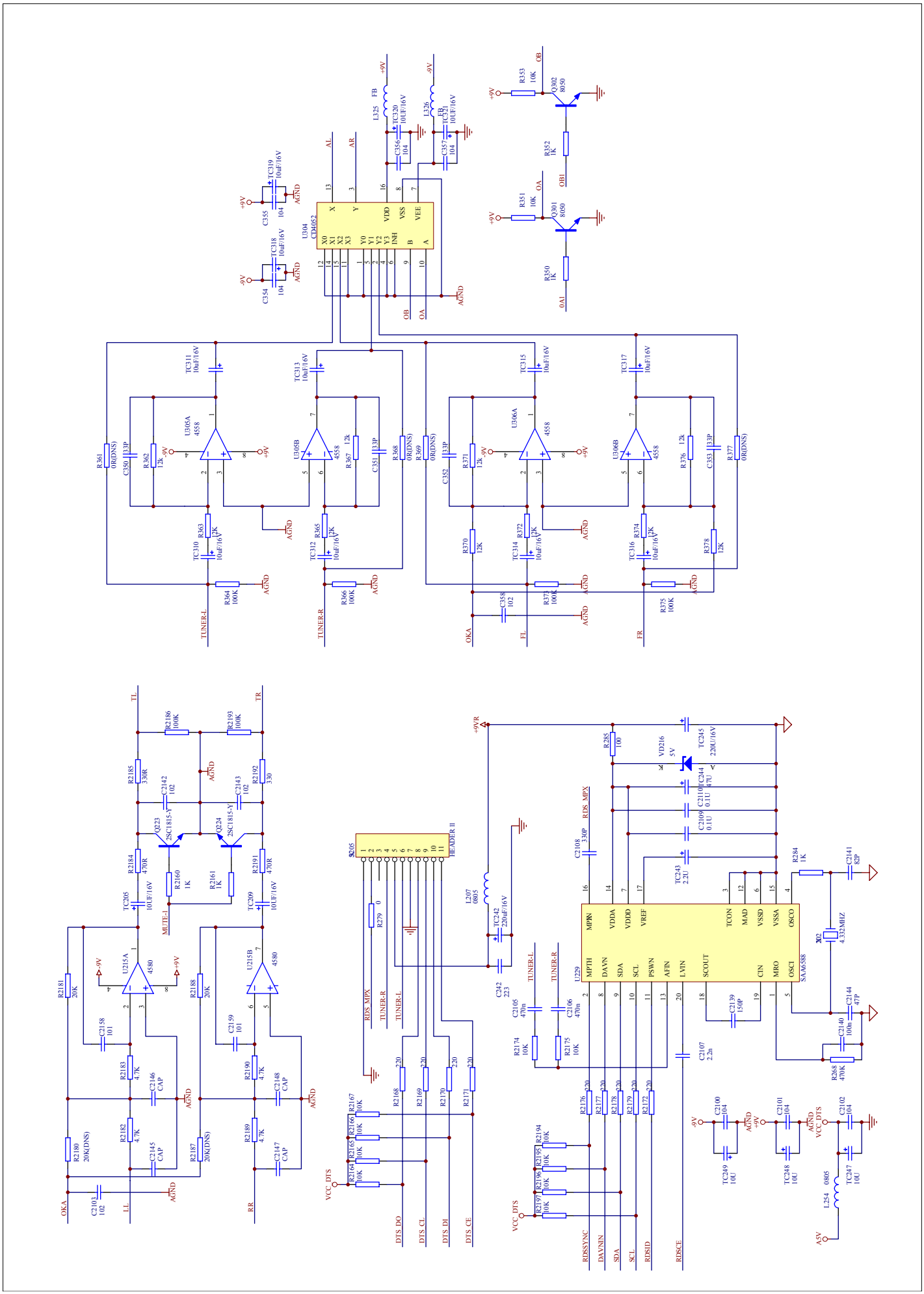
MIAN SCHEMATIC DIAGRAM



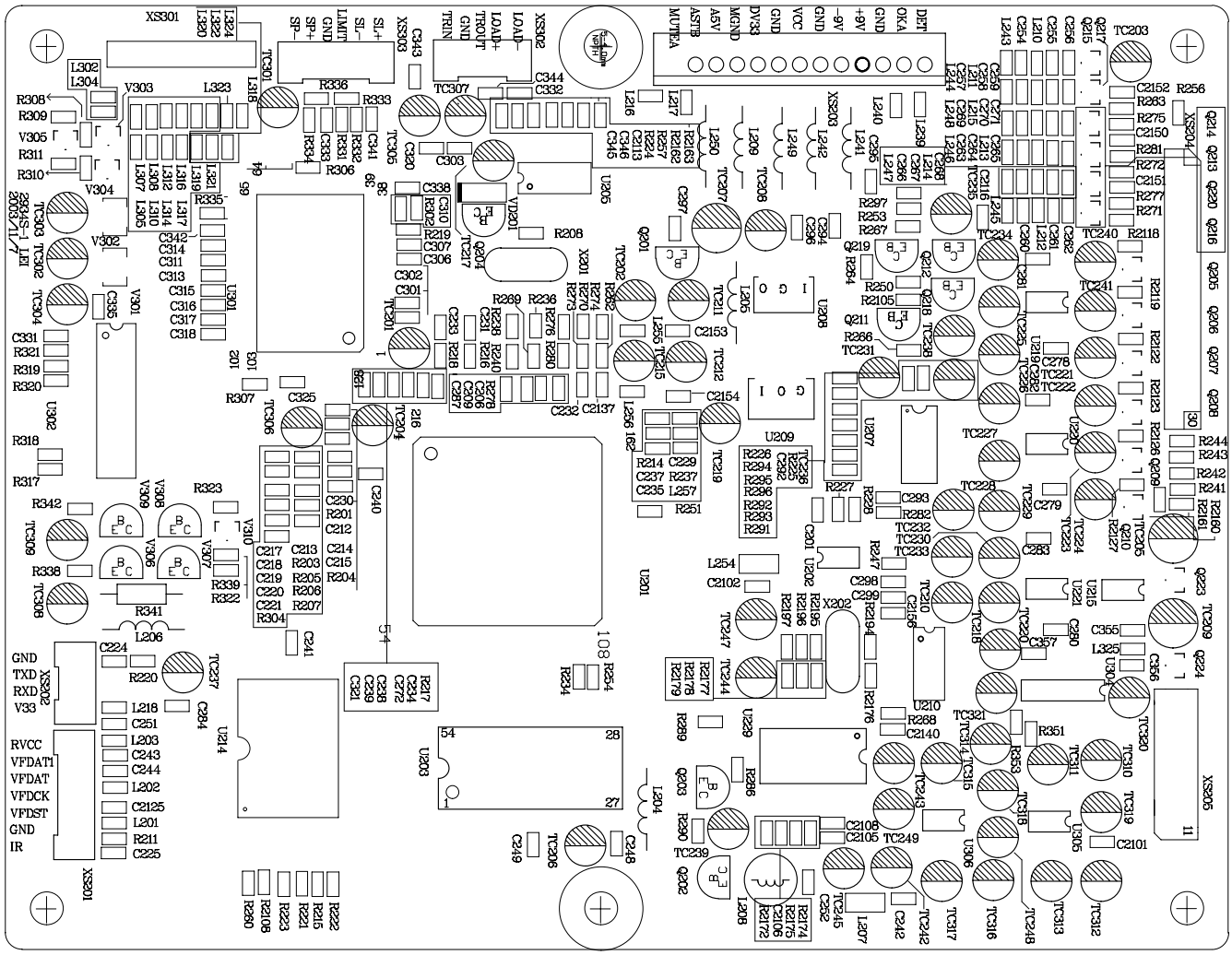
MIAN SCHEMATIC DIAGRAM



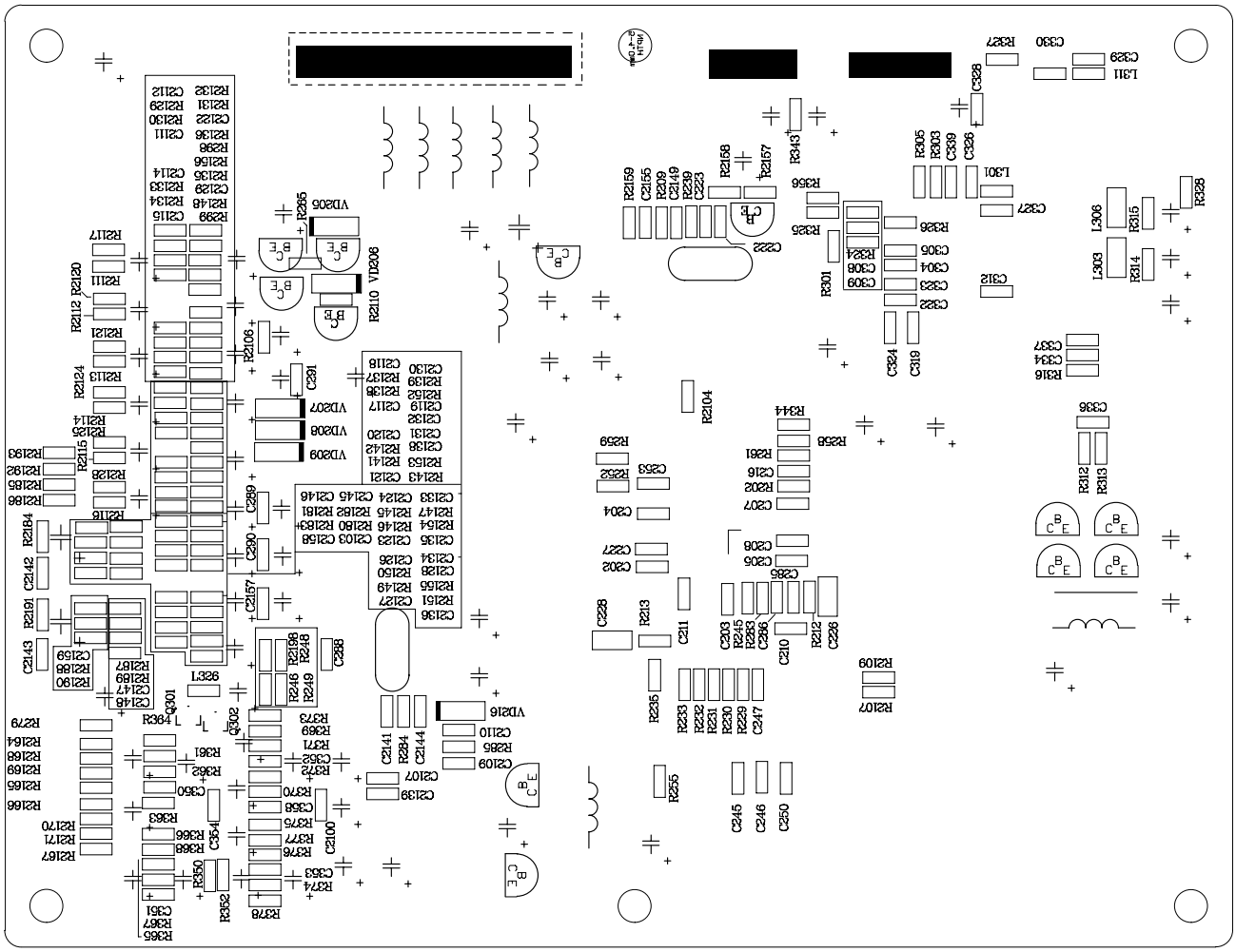
MIAN SCHEMATIC DIAGRAM



MIAN SCHEMATIC DIAGRAM



MIAN SCHEMATIC DIAGRAM



10. SPARE PARTS LIST

bbk9903S MATERIAL LIST

1、DECODING BOARD

NO		MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1		SMD RESISTOR	1/16W 0Ω ±5%	29	C2119,C2128,C2131,L243~L248,R205,R219,R220,R226,R240,R241,R243,R257,R259,R269,R282,R332,R327,R2162,R344,L301,R246,R249,R2185,R2192
2		CARBON FILM RESISTOR	1/4W2.2Ω±5%	1	R341
3		SMD RESISTOR	1/16W1Ω±5%	5	R312,R313,R317,R318,R336
4		SMD RESISTOR	1/16W 4.7Ω ±5%	4	R212,R213,R258,R261
5		SMD RESISTOR	1/16W 15Ω ±5%	2	R314,R315
6		SMD RESISTOR	1/16W 33Ω ±5%	19	R2107~R2109,R2159,R229~R235,R254,R255,R291~R296
7		SMD RESISTOR	1/16W 470Ω ±5%	2	R322,R323
8		SMD RESISTOR	1/16W 150Ω ±5%	15	R256,R262~R264,R270~R277,R280,R281,R247
9		SMD RESISTOR	1/16W 220Ω ±5%	4	R2168~R2171
10		SMD RESISTOR	1/16W 330Ω ±5%	1	R253
11		SMD RESISTOR	1/16W 1K ±5%	31	R227,R228,R252,R266,R267,R2104,R2105, R2106,R2110,R2117~R2128,R2158,R2160, R2161,R290,R286,R2184,R2191,R350,R352,L217
12		SMD RESISTOR	1/16W 1.5K ±5%	2	R338,R342
13		SMD RESISTOR	1/16W 4.7K ±5%	19	R2130,R2131,R2134,R2135,R2138, R2139,R2142,R2143,R2146,R2147,R2150, R2151,R2182,R2183,R2189,R2190,R222,R223,R289
14		SMD RESISTOR	1/16W 6.8K ±5%	8	R2136,R2148,R2152~R2155，R298，R299
15		SMD RESISTOR	1/16W 8.2K ±5%	1	R201
16		SMD RESISTOR	1/16W 10K ±5%	19	R206,R250,R265,R303~R306,R309,R311,R319,R339,R2157,R2164~R2167,R351,R353,R211
17		SMD RESISTOR	1/16W 12K ±5%	4	R371,R372,R374,R376
18		SMD RESISTOR	1/16W 15K ±5%	6	R207,R363,R365，R362,R367，R307
19		SMD RESISTOR	1/16W 20K ±5%	4	R203,R316,R320,R321
20		SMD RESISTOR	1/16W 18K ±5%	2	R204,R216
21		SMD RESISTOR	1/16W24K±5%	8	R2129,R2133,R2137,R2141,R2145,R2149,R2181,R2188
22		SMD RESISTOR	1/16W 2K ±5%	1	R237
23		PRECISION SMD RESISTOR	1/16W 330K ±1%	2	R333,R334
24		PRECISION SMD RESISTOR	1/16W 750K ±1%	3	R202,R331,R335
25		SMD RESISTOR	1/16W 100K ±5%	16	R208,R2111~R2116,R217,R308,R310,R373,R375,R2186,R2193,R364,R366
26		CD	CD11 16V10U±20%5×11 2	41	TC201,TC202,TC203,TC217,TC219, TC221~TC233,TC236,TC240,TC241,TC306, TC307,TC247,TC248,TC249,TC318,TC319, TC205,TC209,TC310,TC312,TC314,TC316, TC311,TC313,TC315,TC317,TC320,TC321, TC210
27		CD	CD11 16V220U±20%6×12 2.5	9	TC207,TC208,TC211,TC212,TC235,TC301, TC242,TC245,TC239
28		CD	CD11 16V47U±20%5×11 2	11	TC204,TC206,TC215,TC234,TC237, TC302~TC305,TC308,TC309
29		CD	CD11 16V1U±20%5×11 2	2	TC218,TC220

30		SMD CAPACITOR	50V 27P ±5% NPO 0603	3	C222,C223,C333
31		SMD CAPACITOR	50V 33P ±5% NPO 0603	4	C350~C353
32		SMD CAPACITOR	50V 47P ±5% NPO 0603	15	C254,C256,C257,C259,C260,C262,C263,C265,C266,C268,C269,C271,C243,C244,C2125
33		SMD CAPACITOR	50V 101 ±5% NPO 0603	13	C216,C225,C285,C286,C342,C2111,C2114,C2117,C2120,C2123,C2126,C2158,C2159
34		SMD CAPACITOR	50V 331 ±5% NPO 0603	2	C217,C218
35		SMD CAPACITOR	50V 151 ±5% NPO 0603	2	C331,C334
36		SMD CAPACITOR	50V 391 ±10% 0603	1	C304
37		SMD CAPACITOR	50V 104 +80%-20% 0603	91	C201~C211,C221,C224,C227,C230~C232,C234,C235,C237,C240,C241,C245~C250,C252,C253,C272,C278~C283,C284,C287,C289~C297,C301~C303,C312~C313,C320~C330,C332,C335~C339,C341,C343~C346,C2113,C2137,C2150~C2154,C2100~C2102,C354,C355,C356,C357,C2157,C288
	37.1	SMD CAPACITOR	25V 104 +80%-20% 0603	91	C201~C211,C221,C224,C227,C230~C232,C234,C235,C237,C240,C241,C245~C250,C252,C253,C272,C278~C283,C284,C287,C289~C297,C301~C303,C312~C313,C320~C330,C332,C335~C339,C341,C343~C346,C2113,C2137,C2150~C2154,C2100~C2102,C354,C355,C356,C357,C2157,C288
38		SMD CAPACITOR	16V 105 +80%-20% 0603	6	C315~C318,C2156,C299
39		SMD CAPACITOR	10V 225 +80%-20% 0805	2	C226,C228
40		SMD CAPACITOR	50V 102 ±10% 0603	15	C233,C238,C239,C2103,C2112,C2115,C2116,C2118,C2121,C2124,C2127,C2146,C2148,C2155,C298
41		SMD CAPACITOR	50V 122 ±10% 0603	8	C2122,C2129,C2130,C2133,C2135,C2136, C2145,C2147
42		SMD CAPACITOR	50V 103 ±10% 0603	4	C212~C215
43		SMD CAPACITOR	50V 153 ±10% 0603	3	C220,C308,C319
44		SMD CAPACITOR	16V 333 ±10% 0603	2	C306,C242
45		SMD CAPACITOR	50V 471 ±5% NPO 0603	1	C311
46		SMD CAPACITOR	50V 82P ±5% NPO 0603	1	C305
47		SMD INDUCTOR	10UH ±10% 2012	3	L254,L303,L306
48		CHOKE COIL	立式 10UH 1A 5mm	1	L208
49		SMD INDUCTOR	1.8UH ±10% 1608	6	L210~L215
50		MAGNETIC BEADS INDUCTOR	RH354708	7	L204,L205,L209,L241,L242,L249,L250
51		SMD MAGNETIC BEADS	FCM1608K-221T05	28	L201~L203,L239,L240,L302,L304,L305,L307,L308,L310,L311,L312,L314,L316~L324, L255~L257,L325,L326
52		SMD MAGNETIC BEADS	FCM2012V-221T07	1	L207
53		SMD DIODE	1N4148	6	VD201,VD205~VD209
	53.1	SMD DIODE	LS4148	6	VD201,VD205~VD209
	53.2	SMD DIODE	LL4148	6	VD201,VD205~VD209
54		SMD TRIODE	8050D	2	Q301,Q302
55		TRIODE	C8050	4	V307,V308,Q201,Q203
56		TRIODE	8550C	3	V306,V309,Q202
57		TRIODE	9014C	1	Q204
58		TRIODE	C1815Y	1	Q212
59		SMD TRIODE	C1815	8	Q205~Q210,Q223,Q224
60		TRIODE	2SA1015	3	Q211,Q218,Q219
61		SMD TRIODE	3906	6	Q213~Q217,Q220
62		SMD TRIODE	3904	1	V305
63		SMD TRIODE	9014C	1	V310
64		SMD TRIODE	2SK3018	2	V303,V304

65		SMD TRIODE	2SB1132	2	V301,V302
66		IC	NJM4558M SOP	6	U219,U220,U221，U215，U305，U306
	66.1	IC	4580 SOP	6	U219,U220,U221，U215，U305，U306
	66.2	IC	4558 SOP	6	U219,U220,U221，U215，U305，U306
67		IC	MM74HCU04M SOP	1	U205
	67.1	IC	HCU04 SOP	1	U205
68		IC	HY57V641620HGT-7 TSOP	1	U203
69		IC	TL 74HC4052D SOP	1	U304
	69.1	IC	36C7T 3MCD4052BM SOP	1	U304
70		IC	CS4360 SSOP	1	U207
71		IC	24C02N SOP	1	U202
72		IC	MT1336E-C QFP	1	U301
73		IC	MT1379EE-C QFP	1	U201
74		IC	BA5954FP HSOP	1	U302
75		IC	PCM1801U SOP	1	U210
76		CRYSTAL OSCILLATOR	27.00MHz 49-S	1	X201
78		CABLE SOCKET	15P 1.0mm STRAIGHT CONTACT DUAL FLAT PLUG	1	XS204
79		CABLE SOCKET	6/5P 1.25mm CURVING HORIZONTAL DUAL FLAT PLUG	1	XS205
80		SOCKET	5P 2.0mm	2	XS201,XS302
81		SOCKET	6P 2.0mm	1	XS303
82		SOCKET	13P 2.5mm	1	XS203
83		CABLE SOCKET	24 0.5mm SMD WITH CLASP	1	XS301
84		PCB	2934S-1	1	

2. POWER BOARD

NO		MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1		CARBON FILM RESISTOR	1/4W100Ω±5% SHAPED 10	1	R516
2		CARBON FILM RESISTOR	1/4W150Ω±5% SHAPED 10	1	R506
3		CARBON FILM RESISTOR	1/4W1K±5% SHAPED 10	2	R507,R513
4		METAL FILM RESISTOR	1/4W12K±1% SHAPED 10	1	R509
5		METAL FILM RESISTOR	1/4W4.7K±1%	1	R508
6		CARBON FILM RESISTOR	1/4W10K±5% SHAPED 10	2	R502,R514
7		CARBON FILM RESISTOR	1/4W4.7K±5% SHAPED 10	1	R510
8		CARBON FILM RESISTOR	1/4W22K±5% SHAPED 10	1	R512
9		METAL OXIDE FILM RESISTOR	1W 220Ω±5％ SHAPED R 15×8	1	R511
10		METAL OXIDE FILM RESISTOR	2W68K±5% SHAPED FLAT 15×7	1	R503
11		HIGH VOLTAGE RESISTOR	1/2W680K±5%	1	R501
12		CARBON FILM RESISTOR	1/4W1MΩ±5%	2	R505,R515
13		PORCELAIN CAPACITOR	50V 100P ±10% 5mm	5	C507,C509,C511,C513,C514
14		PORCELAIN CAPACITOR	1000V 222±20% NPO7.5mm	1	C502
15		CERAMIC CAPACITOR	1000V 103±20% NPO10mm	1	C501
16		PORCELAIN CAPACITOR	50V 104 ±20% 5mm	8	C506,C508,C510,C517,C515,C518,C519,C520
17		PORCELAIN CAPACITOR	1000V 101 +80%-20% 7.5mm	1	C516
	17.1	PORCELAIN CAPACITOR	1000V 101 ±10% 7.5mm	1	C516
18		CERAMIC CAPACITOR	CT81 400V 221±20% 10mm	1	BC503
	18.1	CERAMIC CAPACITOR	CT81 400V221±10% 10mm	1	BC503
19		TERYLENE CAPACITOR	275V 104 ±20% 15mm	1	BC501
	19.1	TERYLENE CAPACITOR	275V 104 ±10% 15mm	1	BC501
20		CD	GZ16V100U±20%6×12 2.5	3	TC508,TC511,TC513
	20.1	CD	CD11 16V100U±20%6×12 2.5	3	TC508,TC511,TC513
	20.2	CD	CD110 16V100U±20%6×12 2.5	3	TC508,TC511,TC513
	20.3	CD	CD11C 16V100U+20%-15%6×7 2.5	3	TC508,TC511,TC513
	20.4	CD	CD11C 16V100U±20%6×7 2.5	3	TC508,TC511,TC513
21		CD	CD11 25V470U+20%-10%10×16 5	2	TC503,TC504
	21.1	CD	CD11 25V470U±20%10×16 5	2	TC503,TC504
22		CD	CD11 50V47U±20%6×12 2.5	3	TC502,TC512,TC515

23		CD	CD11 10V1000U±20%8×16 3.5	4	TC505,TC506,TC509,TC510
	23.1	CD	CD11 10V1000U±20%8×14 3.5	4	TC505,TC506,TC509,TC510
	23.2	CD	GS 10V1000U±20%8×16 3.5	4	TC505,TC506,TC509,TC510
	23.3	CD	GS 10V1000U±20%8×14 3.5	4	TC505,TC506,TC509,TC510
24		CD	LP3 400V47U±20%22×28 10	1	TC501
	24.1	CD	LS 400V47U±20%22×25 10	1	TC501
25		CHOKE COIL	VERTICAL 10UH 1A 5mm	2	L502,L505
26		CHOKE COIL	VERTICAL 10UH 2A 5mm	2	L506,L507
27		SWITCHING POWER TRANSFORMER	BCK-28-0287	1	T501
28		DIODE	HER105	4	D508,D511,D512,D513
29		DIODE	HER306	2	D509,D510
31		DIODE	HER107	1	D505
32		VOLTAGE REGULATOR DIODE	5.1V 1/2W	1	ZD501
33		VOLTAGE REGULATOR DIODE	9.1V 1W	1	ZD502
34		DIODE	1N4148	2	D506,D507
35		DIODE	1N4007	4	D501~D504
36		TRIODE	2N5551	1	V502
37		IC	TNY268P DIP	1	U501
38		IC	KA431AZ TO-92	1	U503
	38.1	IC	431L TO-92	1	U503
	38.2	IC	TL431C TO-226AA(LP)	1	U503
	38.3	IC	HA17431VP TO-92	1	U503
39		POWER GRID FILTER	UT-20 40mH ±20% 10×13	1	L501
40		PHOTOELECTRIC COUPLER	HS817	1	U502
41		CONTROLLABLE SILICON	MCR100-6	1	U506
	41.1	CONTROLLABLE SILICON	NCR169D TO-92	1	U506
42		METAL OXIDE FILM RESISTOR	2W10Ω±5% SHAPED FLAT 15×7	1	R519
43		SOCKET	13P 2.5mm	1	CN502
44		SOCKET	2P 8.0mm 2#	1	BCN501
45		CONNECTION CORDS	Φ0.6 SHAPED 5mm	3	JP504,JP506,JP507
46		CONNECTION CORDS	Φ0.6 SHAPED 10mm	4	JP501~JP502,JP505,D516
47		CONNECTION CORDS	Φ0.6 SHAPED 7.5mm	2	JP508,JP503
48		HEAT RADIATOR BOARD	11×15×25 WHITE AB905	1	FIXED HEAT RADIATION BOARD
49		TAPPING SCREW	BT 3×8 BLACK	1	U504 FOR HEAT RADIATION
50		CONNECTION CORDS	Φ0.6 SHAPED 12.5mm	2	D515,D514
51		FUSE	T1.6AL 250V	1	F501
52		FUSE HOLDER	BLX-2	1	FOR F501
53		GROUND CHIP OF POWER BOARD	AB903	1	G503
54		IC	LM7805 GOLE SEALED TO-220	1	U504
55		PCB	5967S-0	1	
56		SOCKET	13P 2.0mm	1	CN501

3. MAIN FRONT PANEL

NO		MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1		SOFT SPONGE SPACER	15×7×13.5 DOUBLE-FACED, HARD	2	CONNECT VFD WITH FRONT PANEL PCB
2		SOFT SPONGE SPACER	8×8×14.5 DOUBLE-FACED, HARD	1	CONNECT IR SENSOR WITH FRONT PANEL PCB
3		VFD	VFD16-0801	1	VFD401
	3.1	VFD	HNV-08SS56	1	VFD401
4		DIODE	1N4148	1	D401
5		IC	PT6311 QFP	1	U401
6		LIGHT TOUCH RESTORE SWITCH	KFC-A06-2WB L3.8	3	K401～K403
7		FLAT CABLE	5P100 2.0 2 SOCKET WITL L NEEDLE REVERSE	1	XS402

8		RECEIVER	HS0038B3V	1	U403
9		CARBON FILM RESISTOR	1/6W2.2Ω±5% SHAPED 7.5	1	R418
10		CARBON FILM RESISTOR	1/6W100Ω±5% SHAPED 7.5	1	R415
11		CARBON FILM RESISTOR	1/6W10K±5% SHAPED 7.5	4	R406,R409,R410,R417
12		SMD RESISTOR	1/16W 4.7K ±5%	1	R435
13		SMD RESISTOR	1/16W 10K ±5%	3	R407,R408,R416
14		CARBON FILM RESISTOR	1/6W33K±5% SHAPED 7.5	5	R402~R404,R411~R412
15		SMD RESISTOR	1/16W 33K ±5%	3	R401,R413~R414
16		SMD RESISTOR	1/16W 51K ±5%	1	R405
17		SMD RESISTOR	1/16W 470Ω ±5%	1	R433
18		RADIATION DIODE	Φ3 RED	1	LED401
19		CD	CD11C 50V47U±20% 8×9 3.5	1	TC414
20		CD	CD11 16V22U±20%5×11 2	1	TC416
21		SMD CAPACITOR	50V 104 +80%-20% 0603	2	C401,C422
22		PORCELAIN CAPACITOR	50V 104 +80%-20% 2.5mm	1	C405
23		SMD RESISTOR	1/16W 0Ω ±5%	1	R430
24		CD	CD11C 16V100U±20%6×7 2.5	2	TC407,TC402
25		SMD CAPACITOR	50V 101 ±5% 0805	3	C403,C404,C406
26		PCB	4967A-1	1	
27		FLAT CABLE	10P250 2.0 2 SOCKET WITH L NEEDLE, THE SAME DIRECTION	1	XS401

4. OK BOARD

NO		MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1		CARBON FILM RESISTOR	1/6W10Ω±5% SHAPED 7.5	2	R621,R622
2		CARBON FILM RESISTOR	1/6W1K±5% SHAPED 7.5	1	R607
3		CARBON FILM RESISTOR	1/6W10K±5% SHAPED 7.5	3	R605,R609,R623
4		CARBON FILM RESISTOR	1/6W4.7K±5% SHAPED 7.5	1	R612
5		CARBON FILM RESISTOR	1/6W330Ω±5% SHAPED 7.5	1	R616
6		CARBON FILM RESISTOR	1/6W100K±5% SHAPED 7.5	2	R615,R617
7		CARBON FILM RESISTOR	1/6W5.1K±5% SHAPED 7.5	1	R613
8		CARBON FILM RESISTOR	1/6W22K±5% SHAPED 7.5	1	R601
9		CARBON FILM RESISTOR	1/6W100Ω±5% SHAPED 7.5	1	R619
10		CARBON FILM RESISTOR	1/16W 10K ±5%	1	R620
11		CARBON FILM RESISTOR	1/6W560Ω±5% SHAPED 7.5	1	R603
12		CD	CD11 16V4.7U±20%5×11 2	3	TC601,TC603,TC613
13		CD	CD11 16V22U±20%5×11 2	1	TC605
14		CD	CD11 10V47U±20%5×7 2	3	TC611,TC615,TC616
	14.1	CD	CD11C 16V47U±20%5×7 2	3	TC611,TC615,TC616
15		PORCELAIN CAPACITOR	50V 47P ±5% NPO 5mm	1	C605
	15.1	PORCELAIN CAPACITOR	50V 47P ±5% 5mm	1	C605
	15.2	PORCELAIN CAPACITOR	50V 47P ±10% 5mm	1	C605
16		PORCELAIN CAPACITOR	50V 102 +80%-20% 2.5mm	1	C608
17		PORCELAIN CAPACITOR	50V 103 ±10% 5mm	1	C603
18		PORCELAIN CAPACITOR	50V 104 +80%-20% 2.5mm	3	C601,C602,C624
19		MAGNETIC BEADS INDUCTOR	RH354708	1	L602
20		DIODE	1N4148	3	VD601~VD603
21		IC	NJM4558D DIP	2	U601,U602
22		SOCKET	10芯 2.0mm	1	XS602
23		MICROPHONE SOCKET	ST-403-070-100	1	MIC602
24		ROTATED POTENTIOMETER	WH09NTX-1C-A10K-F30 WITH NUT	1	VR601
25		CONNECTION BOARDS	Φ0.6 SHAPED 7.5mm	2	JP601,JP603
26		CONNECTION BOARDS	Φ0.6 SHAPED 5mm	3	JP602,JP604,JP605
27		MIC METAL PLANK	DV967GREY	1	
28		LIGHT TOUCH RESTORE SWITCH	HORIZONTAL 6×6×1	1	K601
29		WIRE	20# 70mm BLACK WITH WELDING PIECE	1	GND1
30		PCB	6967S-0	1	

31		SOFT FLAT CABLE	13P50 2.0 2 SOCKET WITH L NEEDLE REVERSE	1	XS601

5. OUTPUT BOARD

NO		MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY	LOCATION
1		SMD RESISTOR	1/16W 100Ω ±5%	1	R702
2		CARBON FILM RESISTOR	1/4W68Ω±5%	1	R703
3		SMD RESISTOR	1/16W 2.2Ω ±5%	1	R706
4		CARBON FILM RESISTOR	1/4W220Ω±5%	1	R701
5		SMD CAPACITOR	50V 102 ±10% 0603	8	C701~C706,C717,C718
6		SMD CAPACITOR	25V 104 +80%-20% 0805	3	C710,C711,C716
	6.1	SMD CAPACITOR	50V 104 +80%-20% 0805	3	C710,C711,C716
8		SMD CAPACITOR	50V 224 +80-20% 0805	1	C715
	8.1	SMD CAPACITOR	25V 224 +80%-20% 0805	1	C715
	8.2	SMD CAPACITOR	16V 224 +80%-20% 0805	1	C715
9		CD	CD11 16V220U±20%6×12 2.5	5	TC701,TC703~TC706
10		CD	GS 10V1000U±20%8×14 3.5	1	TC702
	10.1	CD	CD11 10V1000U±20%8×14 3.5	1	TC702
	10.2	CD	GS 10V1000U±20%8×16 3.5	1	TC702
	10.3	CD	CD11 10V1000U±20%8×16 3.5	1	TC702
11		MAGNETIC BEADS INDUCTOR	RH354708	14	L701~L714
12		ELECTRO-OPTIC TRANSFORMER	TX179ATW	1	JK705
	12.1	ELECTRO-OPTIC TRANSFORMER	TX179AT	1	JK705
13		TERMINAL SOCKET	AV4-8.4-6G-3	1	JK702
14		TERMINAL SOCKET	DASW-8	1	JK703
15		TERMINAL SOCKET	AV8-8.4-6G-3	1	JK701
16		CABLE SOCKET	15P 1.0mm STRAIGHT CONTACT DUAL FLAT PLUG	1	XS701
17		CONNECTION CORDS	Φ0.6 SHAPED 5mm	7	JP701,JP704,JP706,JP707,JP711,JP712, JP714
18		CONNECTION CORDS	Φ0.6 SHAPED 7.5mm	5	JP702,JP703,JP708,JP709,JP713
19		CONNECTION CORDS	Φ0.6 SHAPED 10mm	2	JP705,R707
20		SCART SOCKET	SCART-01	1	JK706
21		TRIODE	S8050D	3	V701~V703
22		PCB	7969A-0	1	
23		SMD RESISTOR	1/16W 4.7K ±5%	1	R704
24		CARBON FILM RESISTOR	1/4W330Ω±5%	1	R709
25		CARBON FILM RESISTOR	1/4W33Ω±5%	1	R708
26		SMD RESISTOR	1/16W 2.2K ±5%	1	R710
27		CARBON FILM RESISTOR	1/6W2.2K±5%	1	R712
28		SMD RESISTOR	1/16W 1K ±5%	1	R711
29		SMD RESISTOR	1/16W 75Ω ±5%	1	R705
30		SMD CAPACITOR	16V 105 +80%-20% 0603	1	C707

AM/FM Tuner Specification

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			TFCF1U800A
END CUST	CUST	CUST MODEL NO.	ALPS MODEL NO.

					APPD	CHKD	DSGD	
								TITLE PRODUCT **TFCF1U** SPECIFICATION
					DOCUMENT NO.			
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				0/11

AM/FM Tuner Specification

1.Application product P/N TFCF1U TYPE FM/AM TUNER

1-1.Manufacturing location Japan and People Republic of China and Malaysia

2.Specification Customer Specification USA / CND Version

3.Test conditions

Usual standard test with next condition

Measurement shall be started to minutes after power applied

The apply voltege must be regulated +9 v ± 2%

Condition Temperature :5。ｵ35。

Humidity :45。ｵ85 % Rh

If there is an objection to test result, they set up with next test condition

Condition Temperature :20±2。

Humidity :60。ｵ70 % Rh

Unit: Scale / Tolerance

	Components	Materials Finish/ Specifications				Components	Materials Finish/ Specifications		
1			6						
2			7						
3			8						
4			9						
5			1		0				

					DSGD.			
					CHKD.	TITLE PRODUCT		
						TFCF1U SPECIFICATION		
					APPD			
						(1/11)		
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

4.General Specifications

4-1.FM Tuner General Specifications

Frequency Range	87.5MHz。ォ108.0MHz
STEP Frequency	50KHz/100KHz
Intermediate Frequency	10.7MHz(Upper Heterodyne)
Operating Temperature	ィC20。ォ」ォ70。
ANT Input Impedance	75 Unbalanced

4-2. PLL General Specifications

Cutout port function		B01	B02					
		FM/AM	。ェ					
Seral date	0	AM	。ェ					
	1	FM	。ェ					

Crystal Frequency :75KHz

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(2/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

4-3.AM Tuner General Specifications

Frequency Range	530KHz｡ｵ1710KHz
STEP Frequency	10KHz or 9KHz
Intermediate Frequency	450KHzｺﾕ(Upper Heterodyne)
Operating Temperature	ｲC20｡ｵﾚｵ70｡
ANT Input Impedance	Use Dummy antenna which specified If there hanppened,should use loop antenna

5.Machanical specifications

Dimensions	See Assembly drawing
Core torque	3｡ｵ30mN·m
Variable Resistor Torque	3｡ｵ30mN·m
Antenna Connector	FMﾚﾕSticker S DIN 45325/F AMﾚﾕSMK LPR0210-XX09 or ﾏ犒ｱﾆｷ

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(3/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

6-1.Terminal load connections」ユ

Specified jig should be used for measurement

Jig circuit follows 10-2

During FM measurement,use specified by IHF T-200(200Hz。ォ15KHz B.P.F)

Filter for audio output of filer *Less than 200Hz 」ユ18dB/act.out

*220Hz and 15KHz」ユ-3dB MIN

19KHz」ユ-30dB MAX

6-2.Standard connection diagram

FM section」ユ

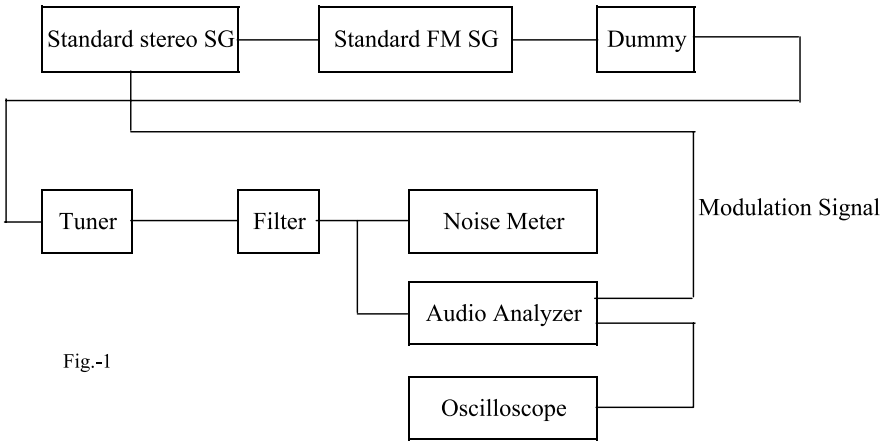


Fig.-1

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(4/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

6-3.Test Modulation

FM」ｺMONO 1KHz 75.0KHz dev

STEREO 1KHz L」ｵR 67.5KHz dev

PILOT 7.5KHz dev

Antenna Input 75ﾗｸ Opened SSG-Dunmy los

RF Input Level 60dBu

AM」ｺ400hz 30% mod

Use Dunmy antenna which specified by ALPS.

RF Input level」ｺ94dBu(ANT Input)

7.DC Specification

ITEM	TEST Condition	SPEO ｹ貂			UNIT
		MIN	TYP	MAX	ｵ･ﾎｻ
Supply Voltage 」ｵ9v	Off Station	8.5	9	9.5	V
Supply Currant 」ｵ9v	Off Station	。I	65	90	mA

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(5/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

8.FM Tuner Electrical Specification (Measurement Points Unless Otherwise Stated are 87.5,98,100MHz.
Concerning MONORAL test shall be at L out terminal)

ITEM	TEST Condition			SPEC ヶ貂			UNITヶ貂
				MIN	TYP	MAX	
50dB S/N Sensitivity			87.5MHz	。I	17	25	dBu
			98.0MHz	—	15	25	
			106.0MHz	。I	17	25	
IHF Sensitivity	Distortion 3%		87.5MHz	。I	14	20	dBu
			98.0MHz	。I	12	20	
			106.0MHz	。I	14	20	
Max S/N Ratio		MONO	98.0MHz	65	72	。I	dB
		STEREO	98.0MHz	60	67	。I	
Distortion		MONO	98.0MHz	。I	0.2	1.5	%
		STEREO	98.0MHz	。I	0.3	2	
Distortion with strong signal	120dBu	MONO	98.0MHz	。I	0.2	2	%
		STEREO	98.0MHz	。I	0.3	2.5	
Audio Output Level	L and R out	MONO	98.0MHz	0	3	6	dBs
		STEREO	98.0MHz	-1	2	5	
Stereo Separation			98.0MHz	25	40	—	dB
Stereo Work Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	18	27	dBu
Tuned Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	18	27	dBu
Auto Stop Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	20	33	dBu

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(6/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

ITEM	TEST Condition		SPEC ｹ貂			UNITｹ貂
			MIN	TYP	MAX	
Image Rejection	MONO	98.0MHz	17	23	—	dB
Carrier Leak		98.0MHz	28	33	—	dB
Emphasis	-12.29 IHF Filter Off	98.0MHz	-3	0	3	dB
Pilot Margin		98.0MHz	4	10	—	dB
Adjacent Channel Selectivity	±400KHz	98.0MHz	20	30	—	dB
AM Rejection		98.0MHz	40	60	—	dB
I.F. Rejection		98.0MHz	60	90	—	dB
Spurious Response Patio		98.0MHz	40	50	—	dB
Spurious Radiation	Meat FOC Requirements Note1.		3	10	—	dB
Antenna Leakage	Meat FOC Requirements Note1.		3	8	—	dB

Note1.Spurlous Radiation and Antenna Leakage ｣ｺUse Radio Set Provided by CUSTMOR

					DSGD.			
					CHKD.	TITLE		PRODUCT
					APPD	**TFCF1U**		SPECIFICATION
								(7/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

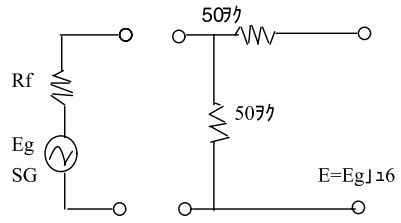
9.AM Tuner Electrcical Specification (Test shall be at L out Terminal)

ITEM	TEST Condition			SPEC ㄅ貂			UNITㄅ貂
				MIN	TYP	MAX	
S/N 20dB Sensitivity			620KHz	—	54	61	dBu
			1050KHz	—	48	57	
			1490KHz	—	48	56	
Max S/N			1050KHz	43	54	—	dB
Distortion			1050KHz	—	1.3	2.5	%
Distortion with Strong Signal	104dBu RF Input Level		1050KHz	—	1.3	2.5	%
Audio Output Level	L.R OUT		1050KHz	-11	-7	—	dBs
One Signal Selectivity	±10KHz		1050KHz	18	27	—	dB
Image Rejection			1050KHz	30	36	—	dB
I.F. Rejection			1050KHz	45	55	—	dB
AGC Form			1050KHz	44	50	—	dB
Audio Frequency Response	O Point 400Hz	100Hz	1050KHz	-10	-5.5	—	dB
	Refㄱ400Hz	4KHz	1050KHz	-22	-16	—	
Auto stop level			1050KHz	—	50	66	dBu
Tuned Level			1050KHz	—	52	61	dBu

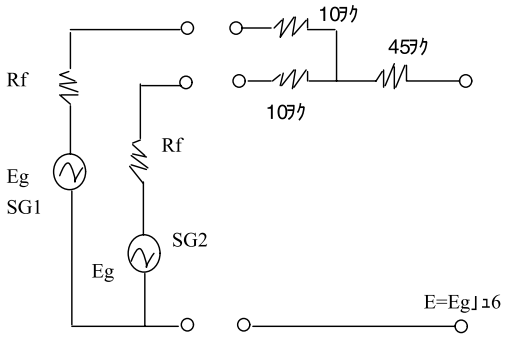
					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(8/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

10-1.ANT PAD

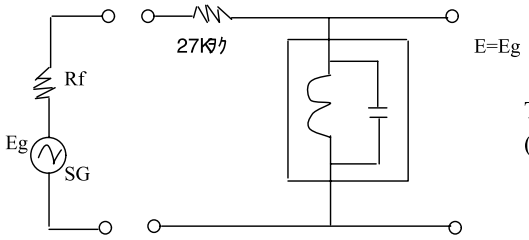
(1).FM1 SIGNAL



(2).FM2 SIGNAL



(3).AM1 SIGNAL



Trans mand TOKO
(LィP15.2uH , C=30PF)

ANT Input Signal Voltage is Open Voltage ON SSG

NOTE」ユUse Test jig which specified

Rf = 50ヲク

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(9/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

11.Printed-Wiring Board Material

ITEM	Contants		
Material Suppliar	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD
Trade Name	MCL − 437F	MCL − 437F	MCL − 437F
UL Grade	94V − 0	94V − 0	94V − 0
Edging Supplier	NIPPON ELEC Co.,LTD	NIPPON ELEC Co.,LTD	PNE PCB LTD.
UL Type Designation	NE 49S△	NE M PF2△	PNE − 1B
UL File NO.	E41166 (S)	E41166 (S)	E67640

Material Suppliar	SUZHOU Matsushita Electric Work Co.,LTD	Suzhou Matsushita Electric Work Co.,LTD
Trade Name	R8700	R8700
UL Grade	94V − 0	94V − 0
Etching Supplier	Yamanashi Matsushita Elactic Work Co.,LTD	Suzhou Matsushita Electric Works(PWB) Co.,LTD
UL Type Designation	NTP−N870A−T YMEW−N870A−T	SMEW−N870A−T
UL File NO.	E107496 (S)	E164387 (S)

Dimension of Print-Wiring Board	56 × 49

					DSGD.			
					CHKD.	TITLE		PRODUCT
						TFCF1U		SPECIFICATION
					APPD			
								(11/E)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

Description of DI control Data

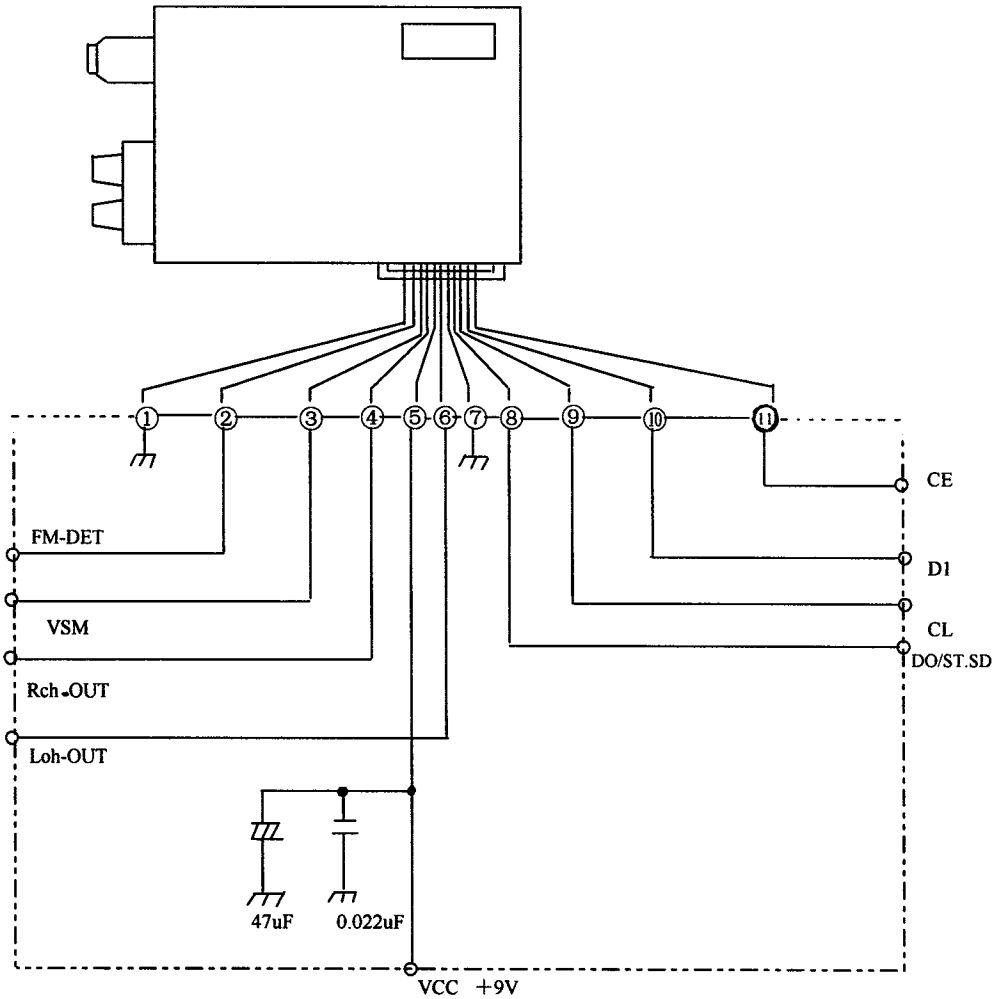
<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS,SNS</td><td>
• Data to set the dividing number of programmable divider
Binary value with P15 assued to be MSB. LSB varies according to DVS and SNS.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number(N)</th><th>actual dividing number</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* P0 to P3 invalid when LSB:P4
• To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN,AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
</td><td></td></tr>
</table>

10-2. TEST JIG

NOTE: Use Test jig which specified



					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(10/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

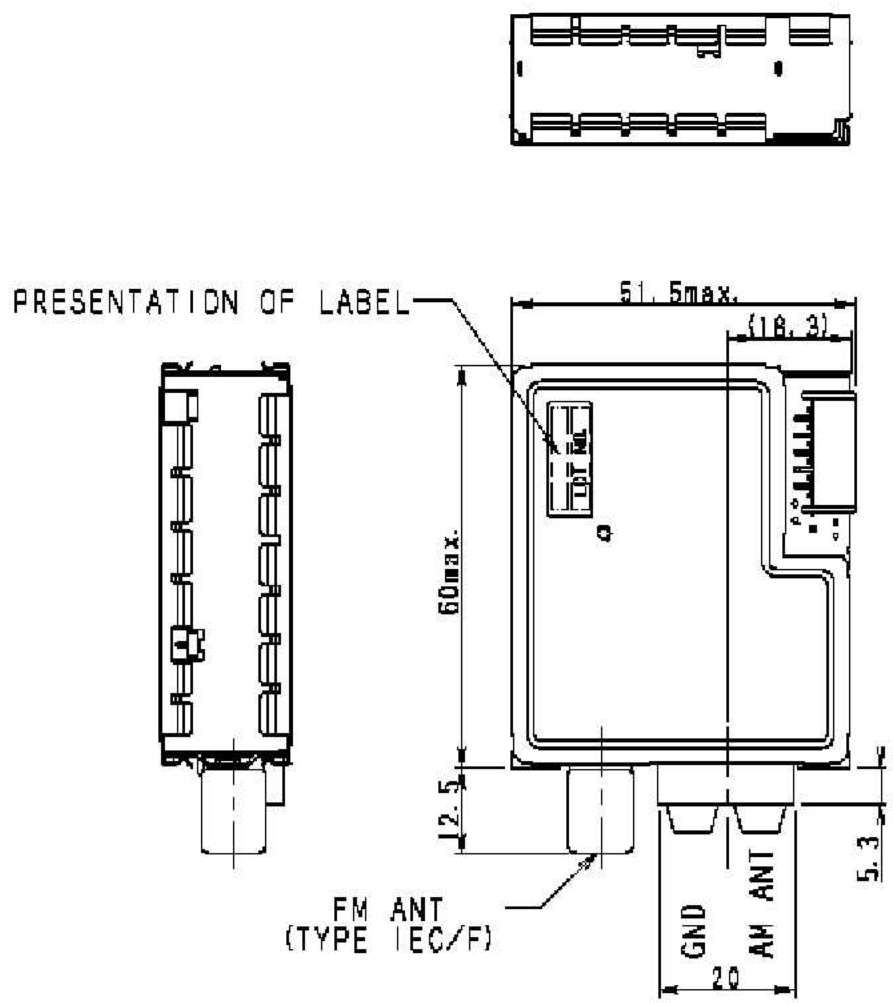
11.Printed-Wiring Board Material

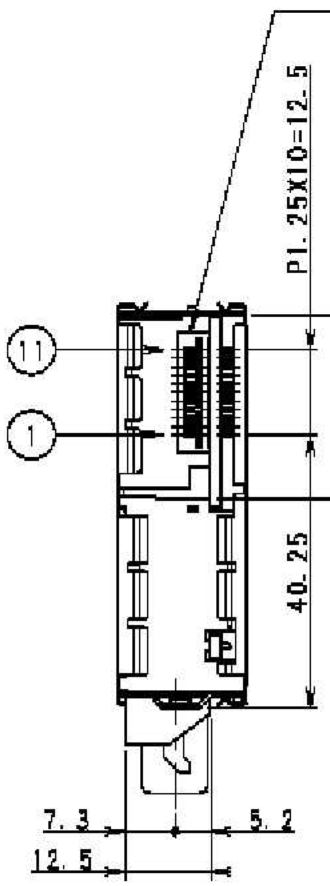
ITEM	Contants		
Material Suppliar	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD
Trade Name	MCL ｣ｪ 437F	MCL ｣ｪ 437F	MCL ｣ｪ 437F
UL Grade	94V ｣ｪ 0	94V ｣ｪ 0	94V ｣ｪ 0
Edging Supplier	NIPPON ELEC Co.,LTD	NIPPON ELEC Co.,LTD	PNE PCB LTD.
UL Type Designation	NE 49S。	NE M PF2。	PNE ｣ｪ 1B
UL File NO.	E41166 (S)	E41166 (S)	E67640

Material Suppliar	SUZHOU Matsushita Electric Work Co.,LTD	Suzhou Matsushita Electric Work Co.,LTD
Trade Name	R8700	R8700
UL Grade	94V ｣ｪ 0	94V ｣ｪ 0
Etching Supplier	Yamanashi Matsushita Elactic Work Co.,LTD	Suzhou Matsushita Electric Works(PWB) Co.,LTD
UL Type Designation	NTP｣ｪN870A｣ｪT YMEW｣ｪN870A｣ｪT	SMEW｣ｪN870A｣ｪT
UL File NO.	E107496 (S)	E164387 (S)

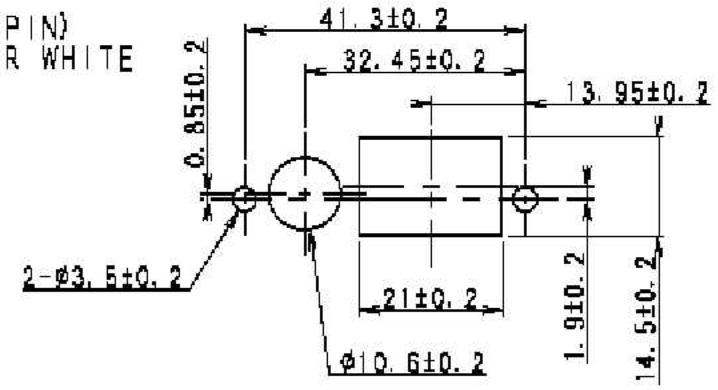
Dimension of Print-Wiring Board	56 × 49

					DSGD.			
					CHKD.	TITLE PRODUCT **TFCF1U** SPECIFICATION		
					APPD	(11/E)		
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				



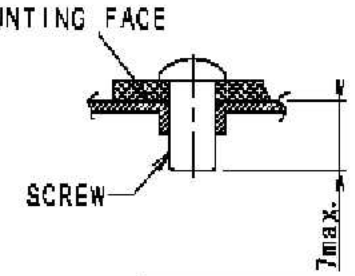


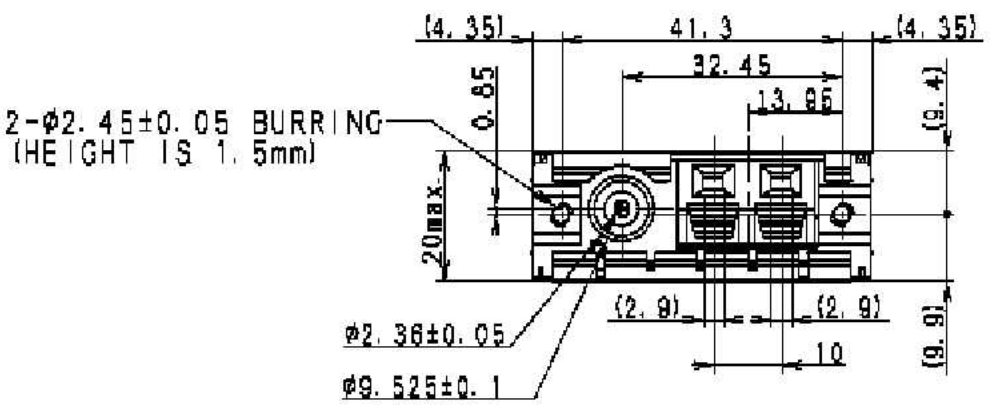
RECOMMENDED MOUNTING HOLE(REFERENCE ONLY)



No.	NAME
①	GND
②	FM DET
③	VSM
④	Rch OUT
⑤	Vcc
⑥	Lch OUT
⑦	GND
⑧	DO
⑨	CL
⑩	DI
⑪	CE

NOTE 1. TOLERANCES ARE ±0.5mm.
UNLESS OTHERWISE SPECIFIED.
2. ALPS CAN ALTER COVER HOLE DESIGN
WITHOUT NOTICE IF NO ELECTRICAL DEGRADATION.
3. SCREW LENGTH FROM MOUNTING FACE IS 8mm MAX.





						TFCF1U
				PRESENTATION OF LABEL	CUST PARTS NO.	ALPS MODEL NO.

PART NO.	NAME	MATERIAL	SPEC.	FINISH

ZONE	SYNB.	DATE OR NO.	APPD.	CHKD.	DSGD.
C-5	B1	Sep. 9.'02	M. K	Y. S	J. K
D-1	A1	K020108	H. O	Y. S	J. K

DSGD. CHKD. APPD.

SCALE 1 : 1

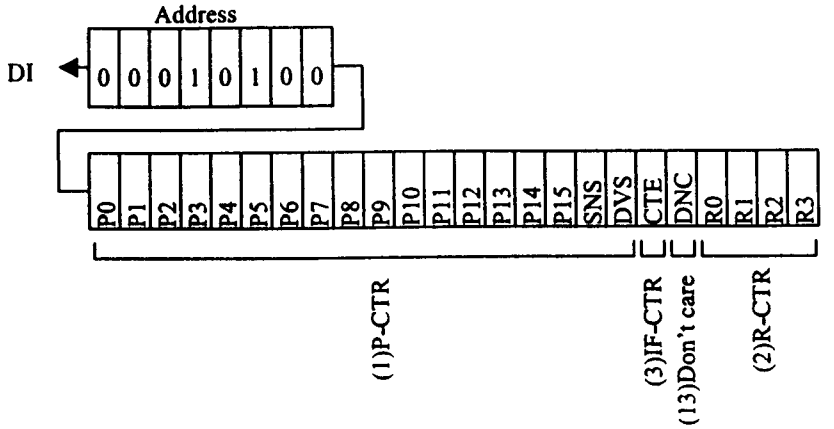
UNIT mm

TITLE TFCF1 ASSEMBLY DRAWING

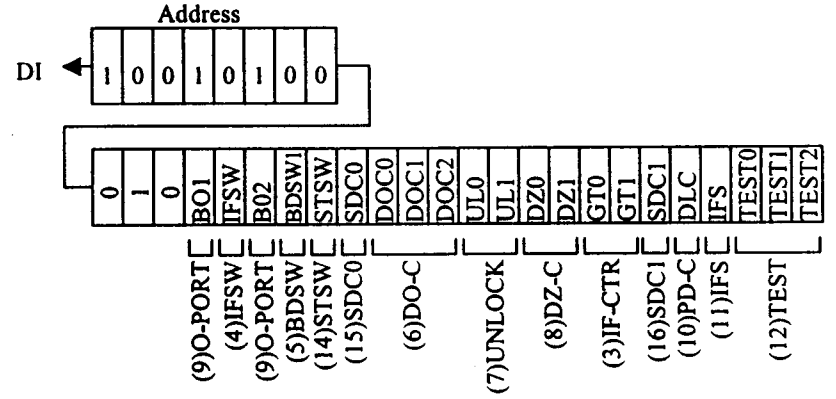
KEY NO. U111A6 (A3・■■■■)

Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



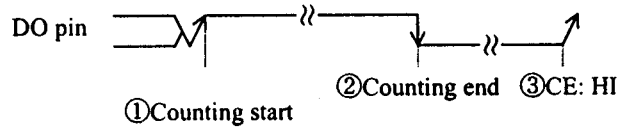
Description of DI control Data

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS,SNS</td><td>
• Data to set the dividing number of programmable divider
Binary value with P15 assued to be MSB. LSB varies according to DVS and SNS.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number(N)</th><th>actual dividing number</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* P0 to P3 invalid when LSB:P4
• To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN,AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
</td><td></td></tr>
</table>

<table>
<tr><td>(3)</td><td>CTE
GT0,GT1</td><td>
<table>
<tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>16</td><td>3 to 4</td></tr>
<tr><td>1</td><td>1</td><td>32</td><td>3 to 4</td></tr>
</table>
</td><td>IFS</td></tr>
<tr><td>(4)</td><td>MUTE control data
IFSW</td><td>• Data to determine the output of output port IFSW, controlling the MUTE function.
"Data"=0: at receiving
1: MUTE</td><td></td></tr>
<tr><td>(5)</td><td>FM/AM BAND selection control data
BDSW</td><td>• Data to determine the output of output port BDSW, controlling selection of BAND.
"Data"=0: AM
1: FM</td><td></td></tr>
<tr><td>(6)</td><td>DO pin control data

DOC0
DOC1
DOC2</td><td>• Data to control DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC(See the item with asterisk below)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Low when SDON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Low when stereo</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
• The open condition is selected at power ON/reset.
* IF counter counting end check
 

① With end-UC set and IF counter starting (CTE=0→1), DO pin opens automatically.
② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made.
③ DO pin opens when serial data is entered/output (CE pin: Hi)
Note: DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE: Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).</td><td>UL0,UL1
CTE</td></tr>
</table>

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(7)</td><td>Unlock detection data

UL0,UL1</td><td>• Phase error (ϕE) detection width selection data to judge if PLL is locked.
Phase error exceeding the detection width is judged that PLL is locked
(*:don't care)
<table><tr><th>UL1</th><th>UL0</th><th>ΦE Detection width</th><th>Detection output</th></tr><tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Direct output of ϕE</td></tr><tr><td>1</td><td>*</td><td>±6.67μ</td><td>ϕE extended by 1 to 2 ms</td></tr></table>* DO pin is LOW. Serial data output: UL = 0.</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>(8)</td><td>Phase comparator control data

DZ0,DZ1</td><td>• Data to control the dead zone of phase comparator
<table><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></table>Dead zone width: DZA<DZB<DZC<DZD</td><td></td></tr>
<tr><td>(9)</td><td>Output port data

$\overline{BO1}$,$\overline{BO2}$</td><td>• Data to determine the output of output ports $\overline{BO1}$ and $\overline{BO2}$
"Data"=0: OPEN
1: Low</td><td></td></tr>
<tr><td>(10)</td><td>Charge pump control data

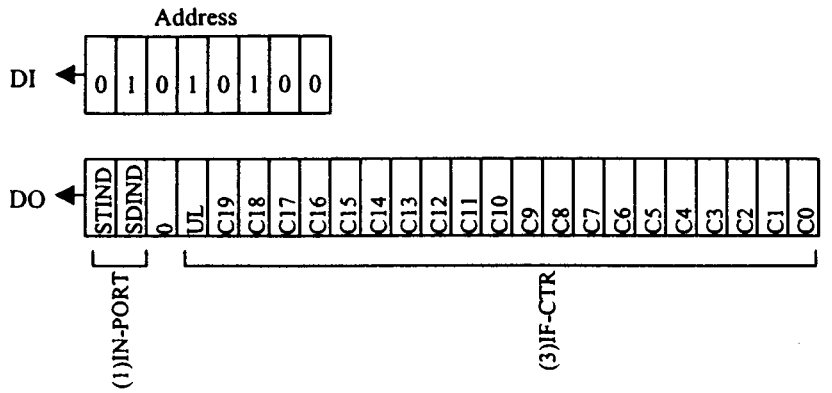
DLC</td><td>• Data to enforce control of charge pump output
<table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Forced to LOW</td></tr></table>In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0 V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to Vcc. (Dead lock clear circuit)</td><td></td></tr>
<tr><td>(11)</td><td>IFS</td><td>• Normally, set Data = 1. Setting Data = 0 causes the input sensitivity worsening mode and the sensitivity decreases by about 10 to 30mVrms.</td><td></td></tr>
<tr><td>(12)</td><td>LSI test data
TEST0 to 2</td><td>• LSI test data
TEST0
TEST1 } All to be set to "0"
TEST2
All set to zero at power ON/reset</td><td></td></tr>
<tr><td>(13)</td><td>DNC</td><td>• Set data = 0.</td><td></td></tr>
<tr><td>(14)</td><td>Forced monaural control data

STSW</td><td>• Data to determine the output of output port STSW, controlling the forced stereo functions.
"Data"=0: MONO
1: STEREO</td><td></td></tr>
<tr><td>(15)
(16)</td><td>SD sensitivity control data

SDC0
SDC1</td><td>• Data to determine the output of output ports SDC0 and SDC1, controlling the SD sensitivity
"Data"=SDC0: 0, SDC1: 0 → SD sensitivity = 42dBuV (Typ)
SDC0: 0, SDC1: 1 → SD sensitivity = 45dBuV (Typ)
SDC0: 1, SDC1: 0 → SD sensitivity = 51dBuV (Typ)
SDC0: 1, SDC1: 1 → SD sensitivity = 56dBuV (Typ)</td><td></td></tr>
</table>

DO control data (serial data output) composition

(1) OUT mode

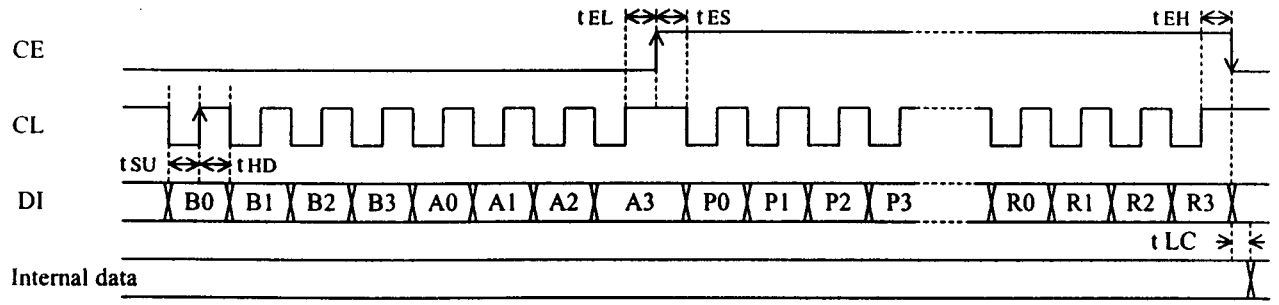


Description of the DO output data

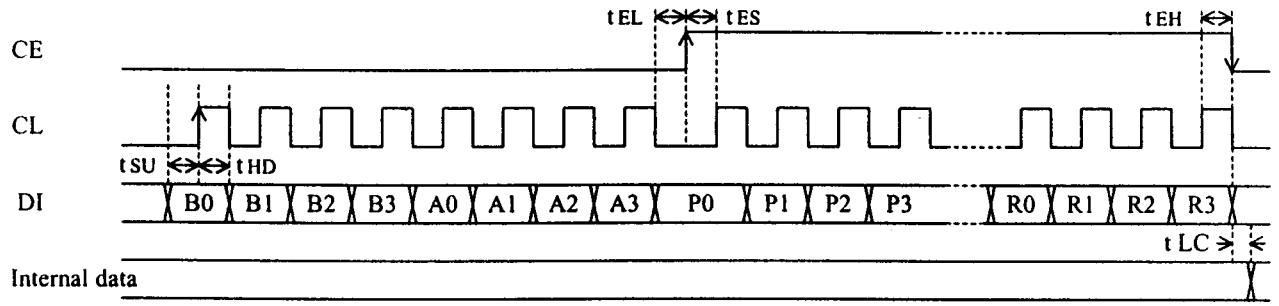
No.	Control block data	Description	Related data
(1)	Stereo and SD indicators control data STIND, SDIND	• Data latching stereo and SD indicator conditions. Latching made in the data output (OUT) mode. STIND ← Stereo indicator condition 0: ST ON, 1: ST OFF SDIND ← SD indicator condition 0: SD ON, 1: SD OFF	
(2)	PLL unlock data UL	• Data latching the content of unlock detection circuit UL ← 0: At unlock 1: At lock or detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	• Data latching the content of IF counter (20-bit binary counter) C19 ← MSB of binary counter C0 ← LSB of binary counter	CTE GT0 GT1

Serial data input (IN1/IN2) t SU, tHD, tEL, tES, tEH ≧ 0.75 μs t LC < 0.75 μs

① CL: Normally HI

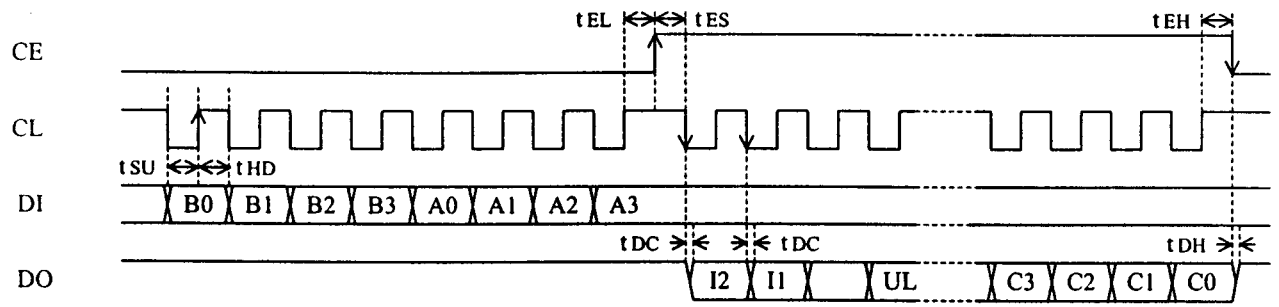


② CL: Normally LOW

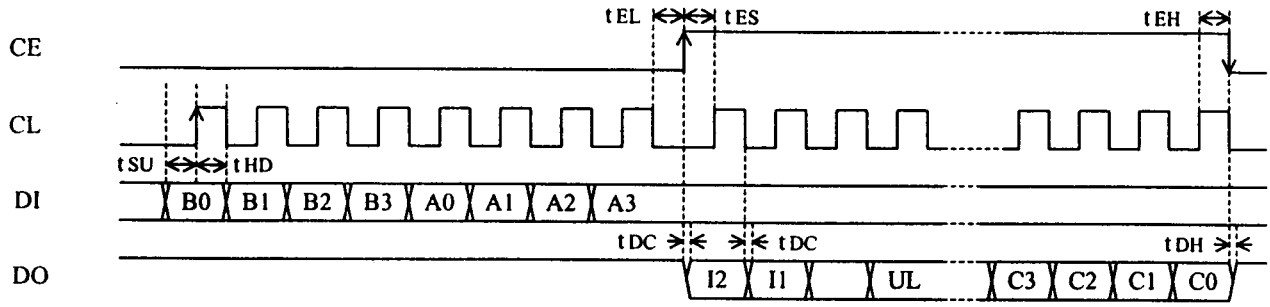


Serial data output (OUT)tSU, tHD, tEL, tES, tEH ≧ 0.75 μs tDC, tDH < 0.35 μs

① CL: Normally Hi

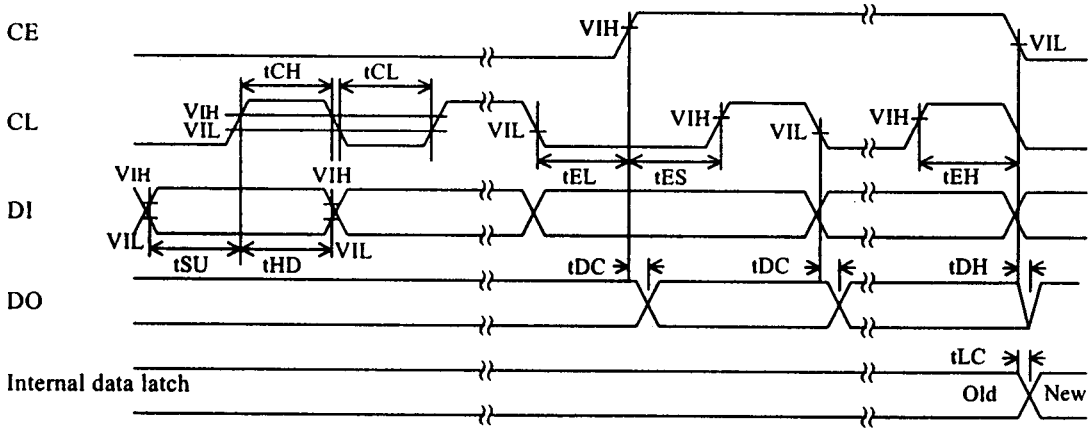


② CL: Normally low

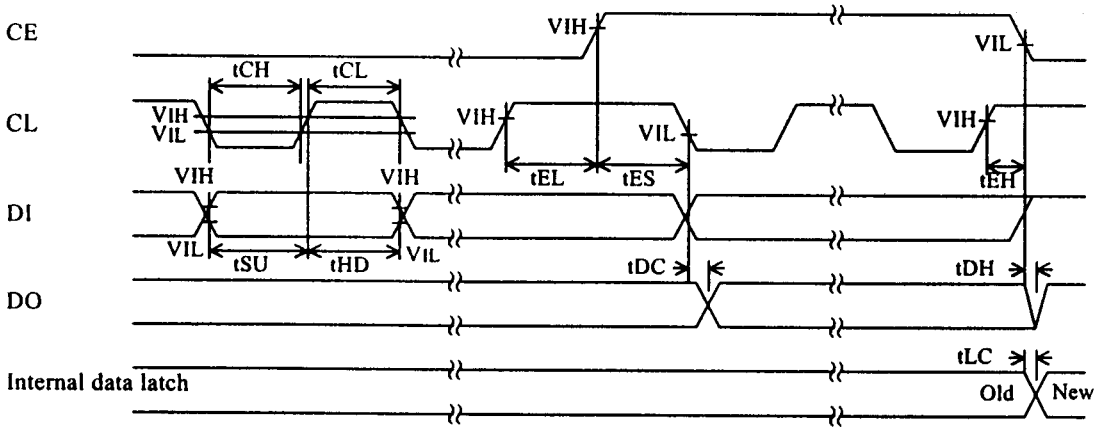


(Note) DO pin is an Nch open drain pin, so that the data varying time (tDC and tDH) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



<< When CL stops at the "L" level >>



<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI,CL		0.75			μs
Data hold time	tHD	DI,CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE,CL		0.75			μs
CE setup time	tES	CE,CL		0.75			μs
CE hold time	tEH	CE,CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO,CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO,CE					

最新カスタムIC搭載により容積30%減（当社従来品比）の小形化を実現。
30 % less volume than our traditional models thanks to state-of-the-art customized IC.

■特長
- 独自開発のICを搭載し、当社従来品容積比約30%減の小形化（60ml）を達成。
- ANTコネクタ部を直出構造とし、内部をフルシールド化することにより、優れたノイズ除去能力を発揮。

■用途
- マイクロコンポーネントステレオ、MDラジカセ、DVD、オーディオレシーバなど多機能化、小形化傾向の進む、各種オーディオ機器、ミニコンポーネントステレオ、各種多機能オーディオ機器。

■Features
- Uniquely developed IC has achieved a small volume of 60 ml, 30 % less than our traditional models.
- Fully shielded structure with ANT connector effectively filters out noise.

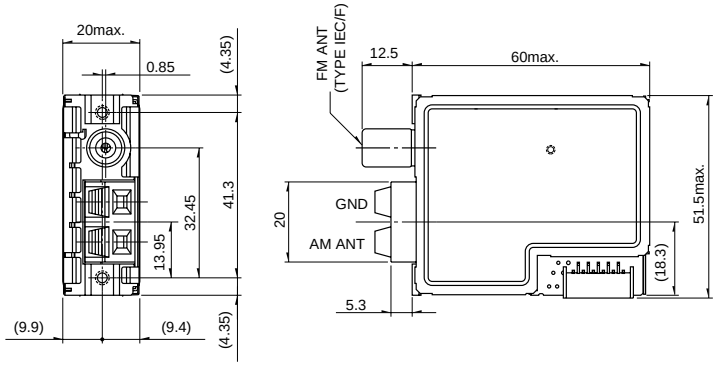
■Applications
- Offers a wide range applications to audio equipment, especially multi-functional, compact audio equipment, such as mini- and micro-component stereo equipment, MD radio cassette recorders, DVDs and audio receivers.

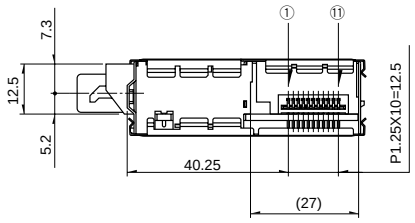
■主な仕様　Typical Specifications

Items		Specifications
Receiving frequency range	AM (kHz)	530 to 1710
	FM (MHz)	87.5 to 108
Input impedance (Ω)	AM	—
	FM	75
Receive sensitivity (dBμ)	AM@SN20dB	51
	FM@SN50dB	15
Stereo separation (dB)	FM	45
Output level (dBs)	AM	−7.5
	FM	2.5
Total harmonic distortion (%)	AM	1.2
	FM	0.25
Power consumption (V/W)		9/500
Volume (ml)		60

■外形図　Dimensions

Unit : mm





Terminal No.	Terminal name
①	GND
②	FM DET
③	VSM
④	Rch OUT
⑤	Vcc
⑥	Lch OUT
⑦	GND
⑧	DO
⑨	CL
⑩	DI
⑪	CE

■回路ブロックダイヤグラム　Circuit Block Diagram