



DVD Player

Service Manual

MODEL: DVD-K2203

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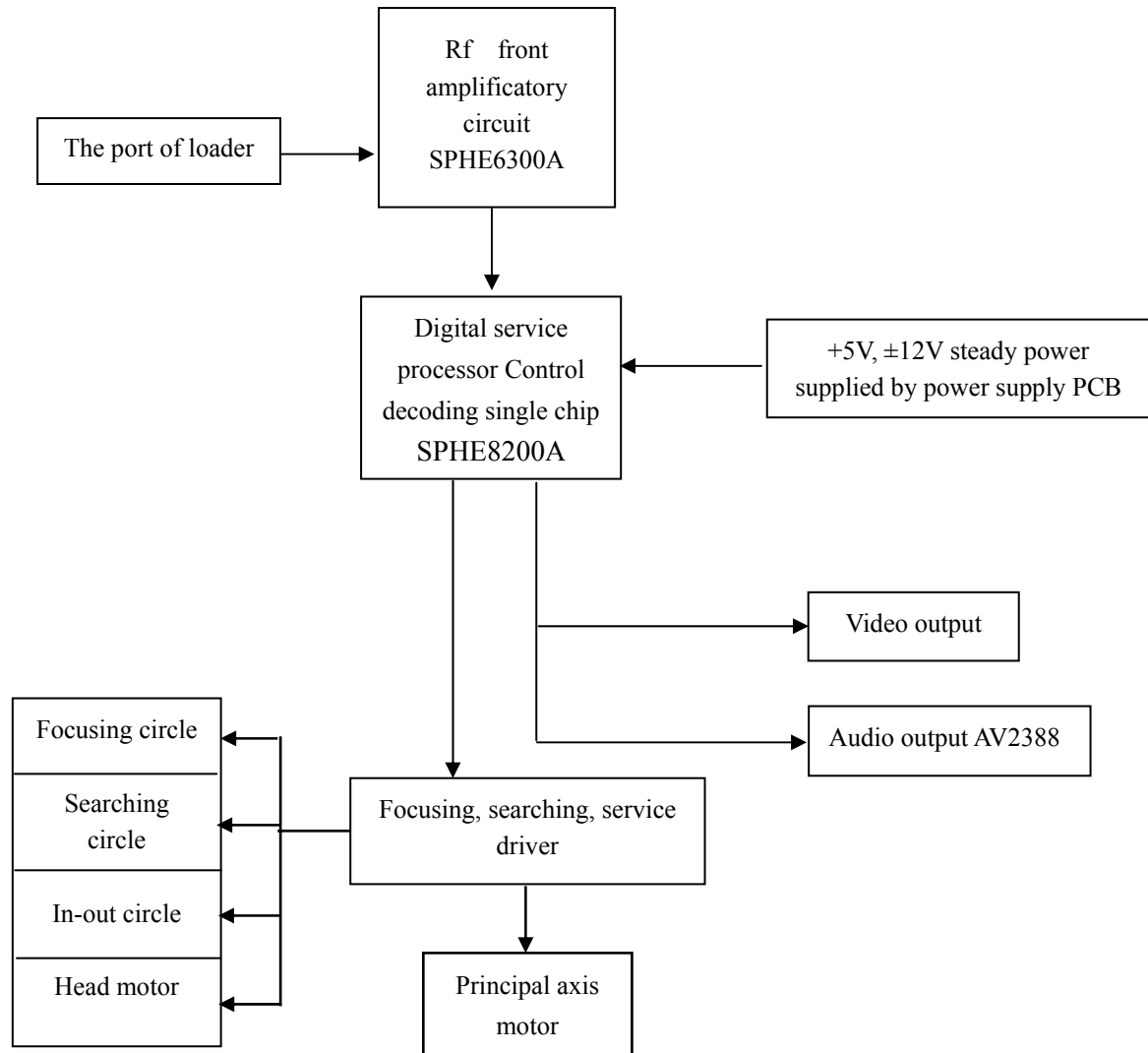
SPECIFICATION

Play mode	NTSC /PAL /AUTO
Disc mode	DVD, VCD, MP3, CD, DVD-R, CD-R, CDR-W
Resolution	≥500 lines
Video S/N ratio	≥56dB
Frequency response	Fs 96KHz; 4Hz-44KHz: +/-1dB
Audio S/N ratio	≥90dB
Dynamic range	≥90dB
Distortion	<0.01%
D/A converter	192KHz /24bit
Video output	1Vp-p(75Ω)
S-Video output	Y: 1Vp-p (75Ω) C: 0.3Vp-p (75Ω)
Audio output	2.0V ± 0.0V / 1.0V
Digital audio output	Coaxial, optical
AC-3	5.1 channel output
Power voltage	~90-250V 50/60Hz
Power consumption	≤25W
Size	409 x 98 x 300mm
Weight	2.5Kg

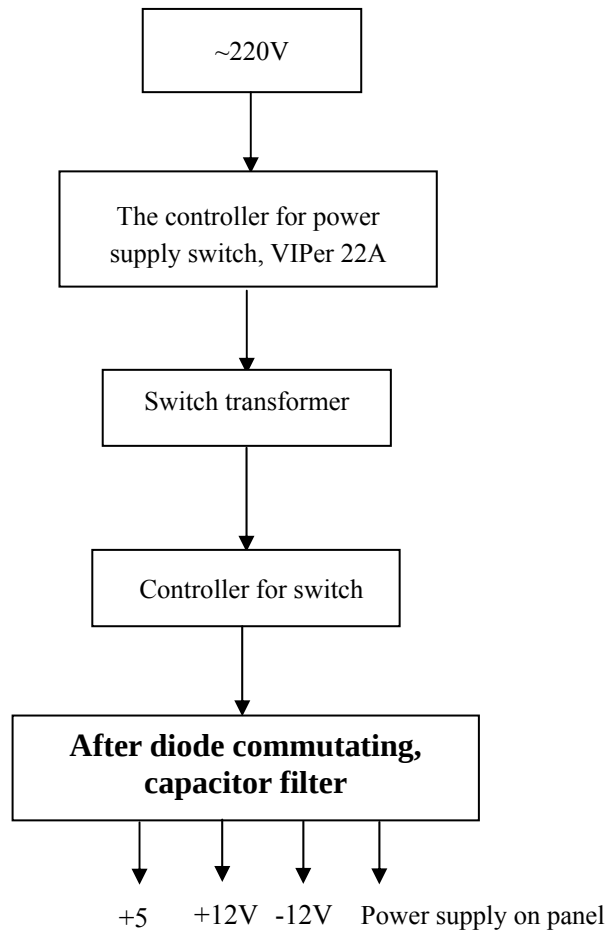
Specifications are subject to change without notice.

DVD CHART

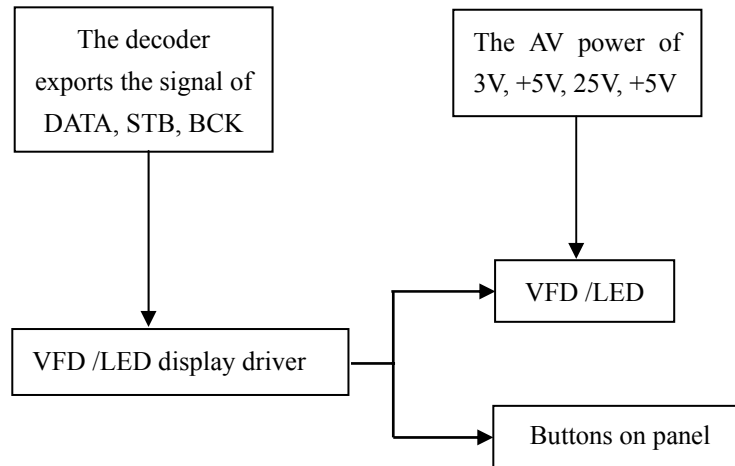
DVD decoder



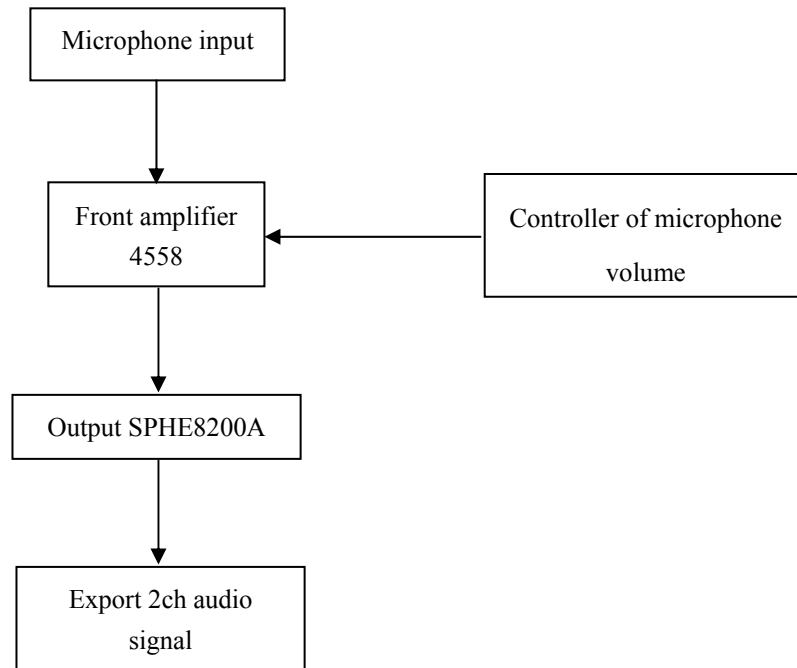
Power Supply of DVD



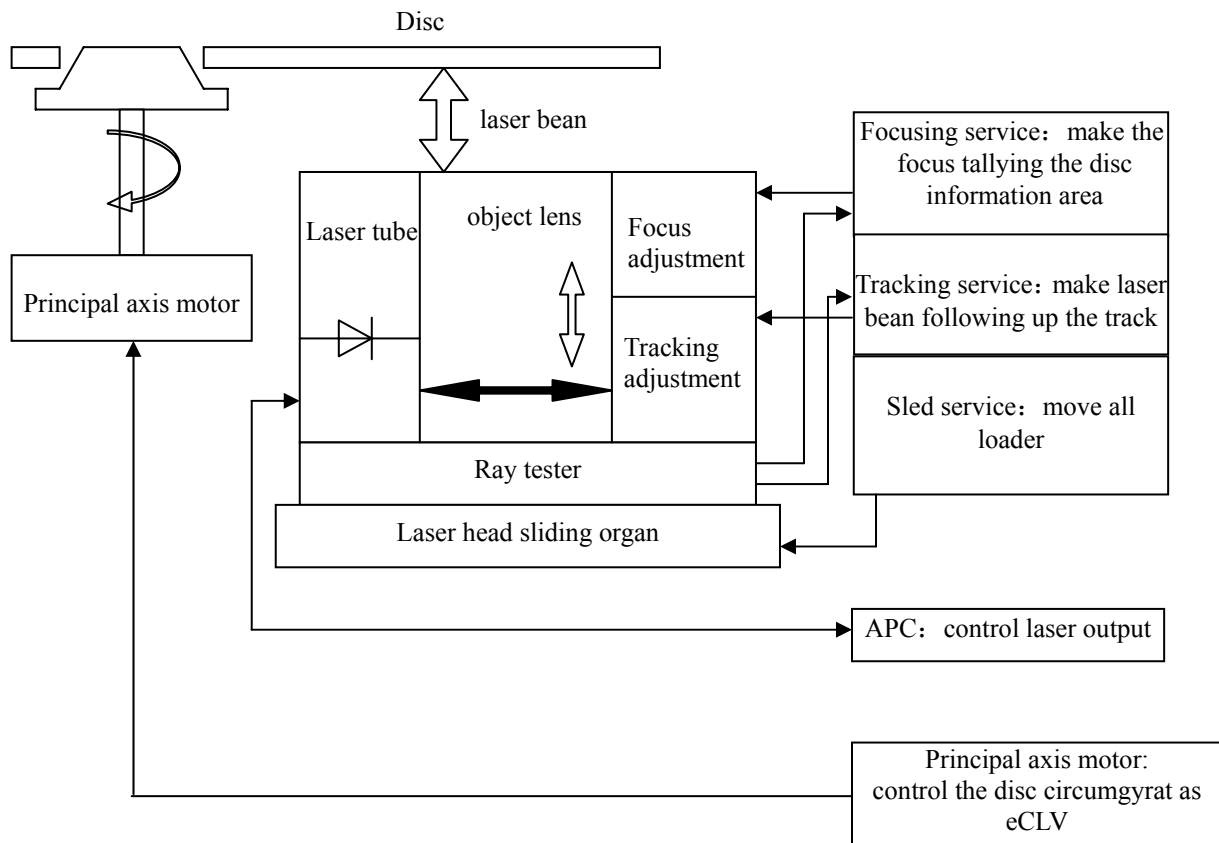
DVD panel



Karaoke of DVD



SERVICE FRAMEWORK



MAIN FUNCTION OF IC

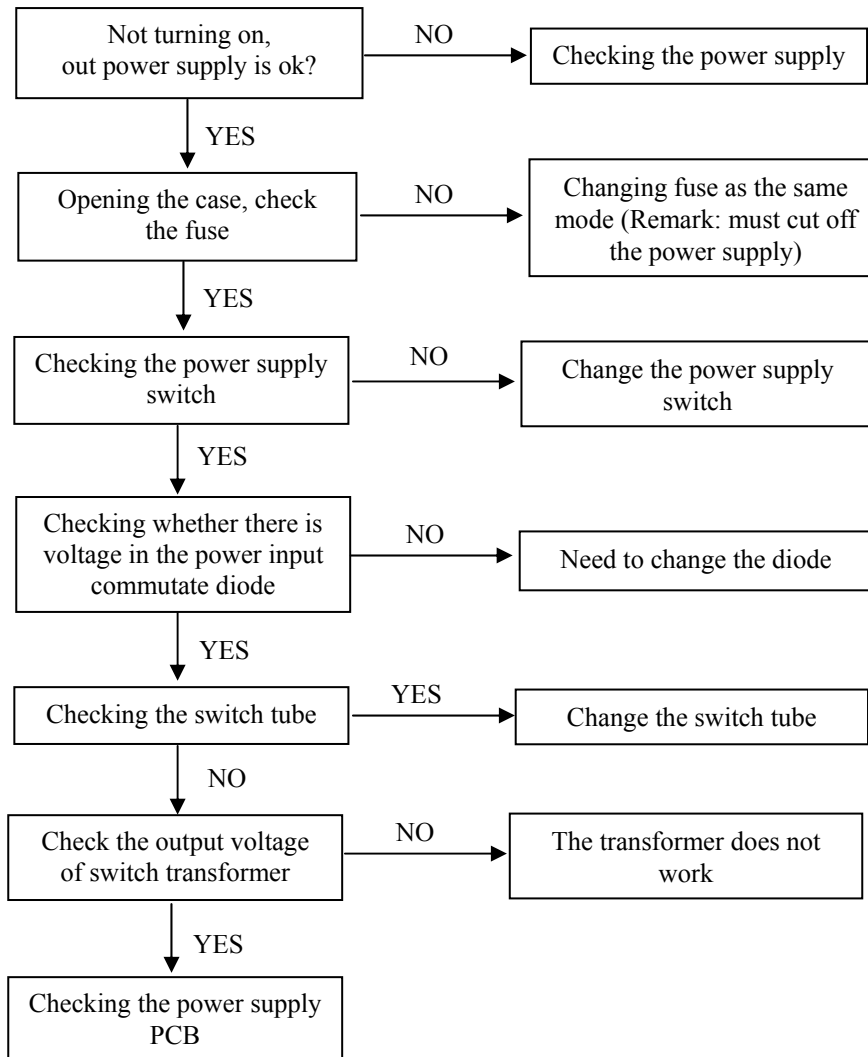
1. The function of SPHE6300A: radio signal front amplifier
2. The function of SPHE8200A: digital signal processor
: central processing: MPEG decoding
3. The function of CD5954: driving IC
4. PCM1606 /CE2752: audio D/A transformer
5. The function of KM16 x 256K: random processor
6. The function of AM29F040B: FLASH

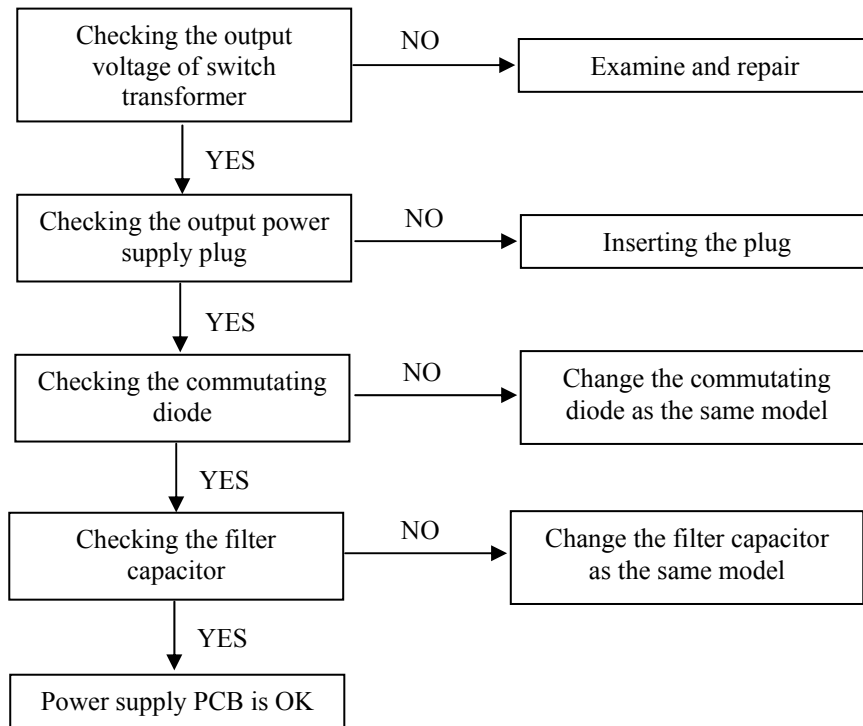
Other IC

7. The function of SEB117: regulator IC
8. The function of 4558: operator amplifier

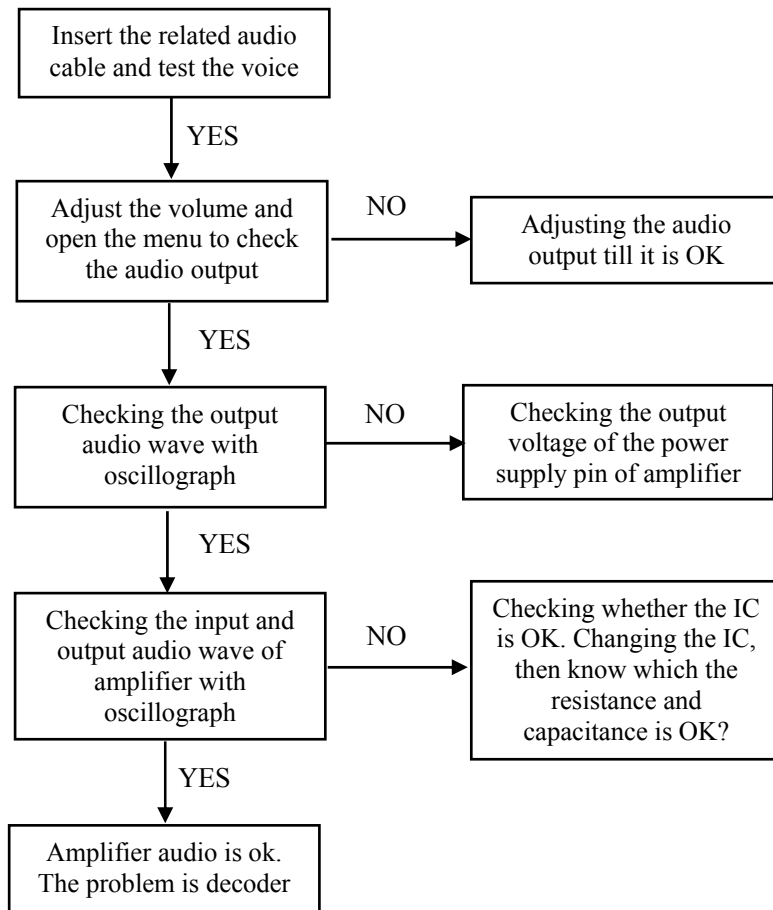
REPAIR PROCEDURE

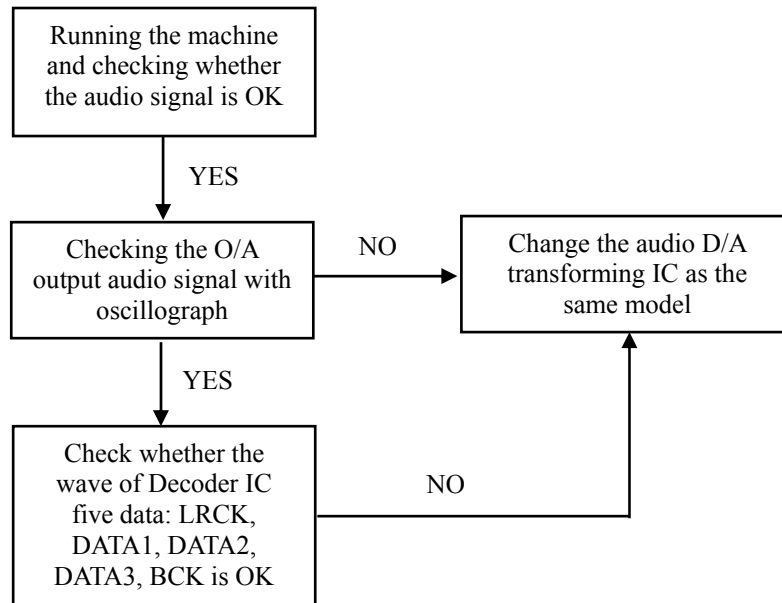
Power supply



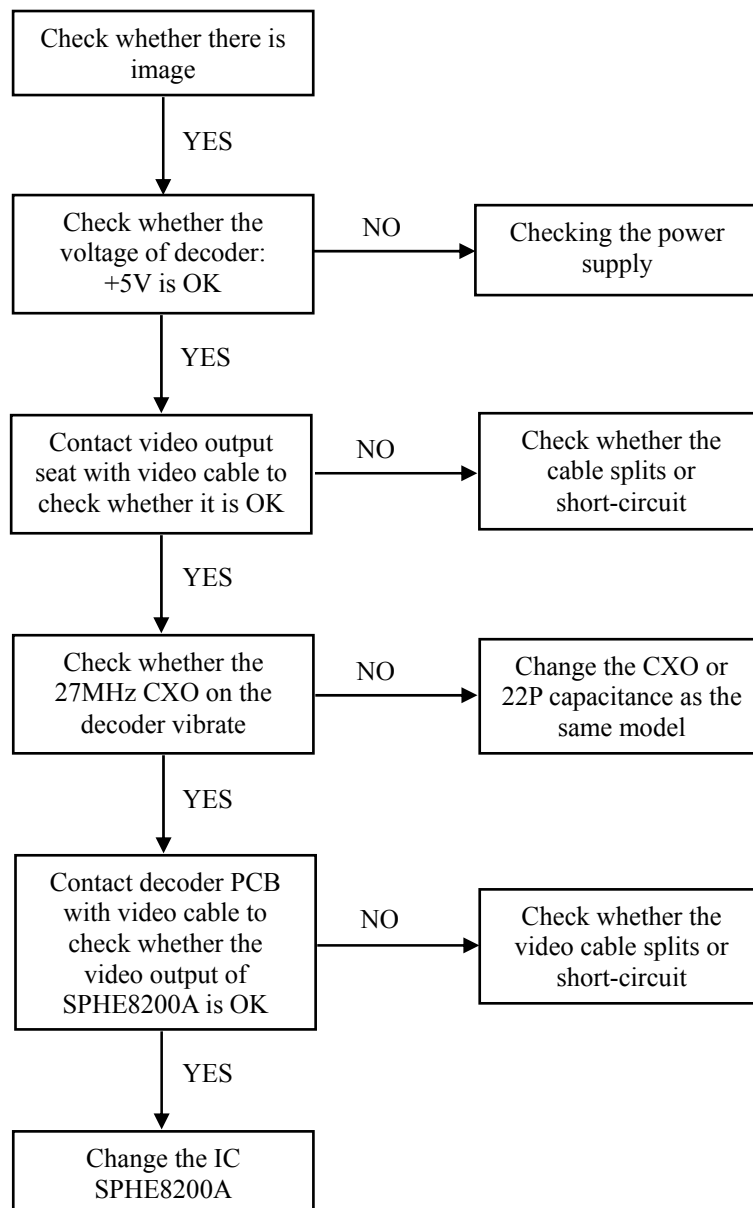


Audio

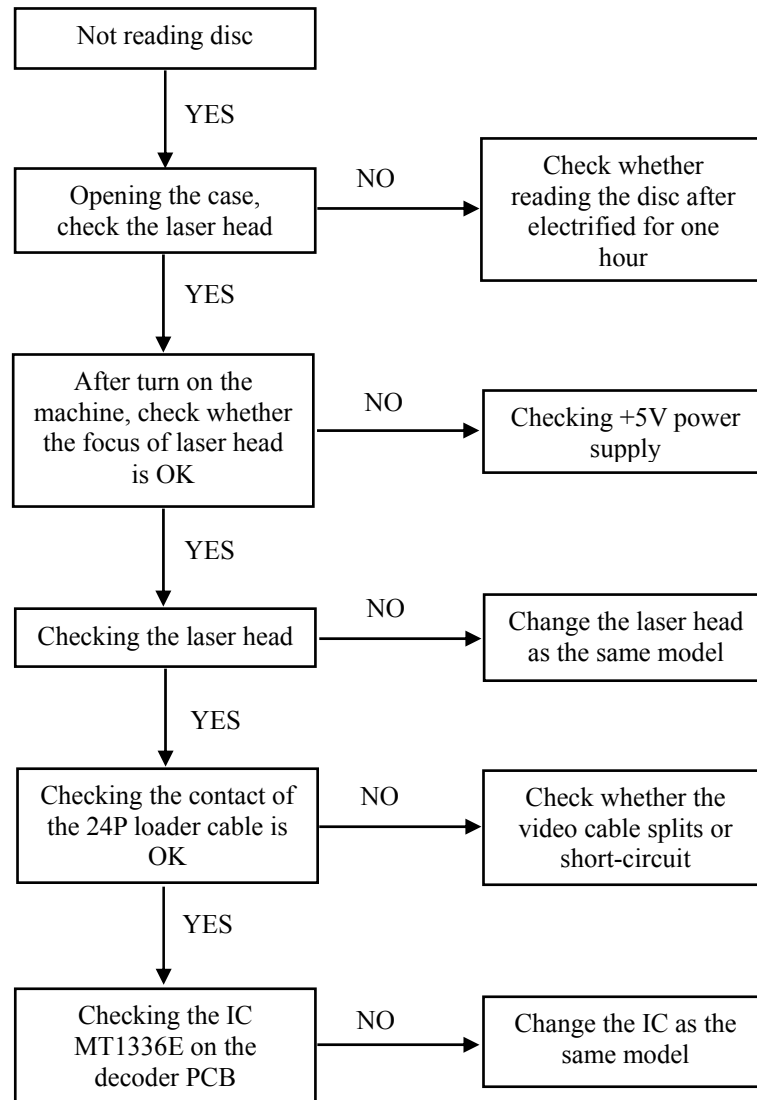




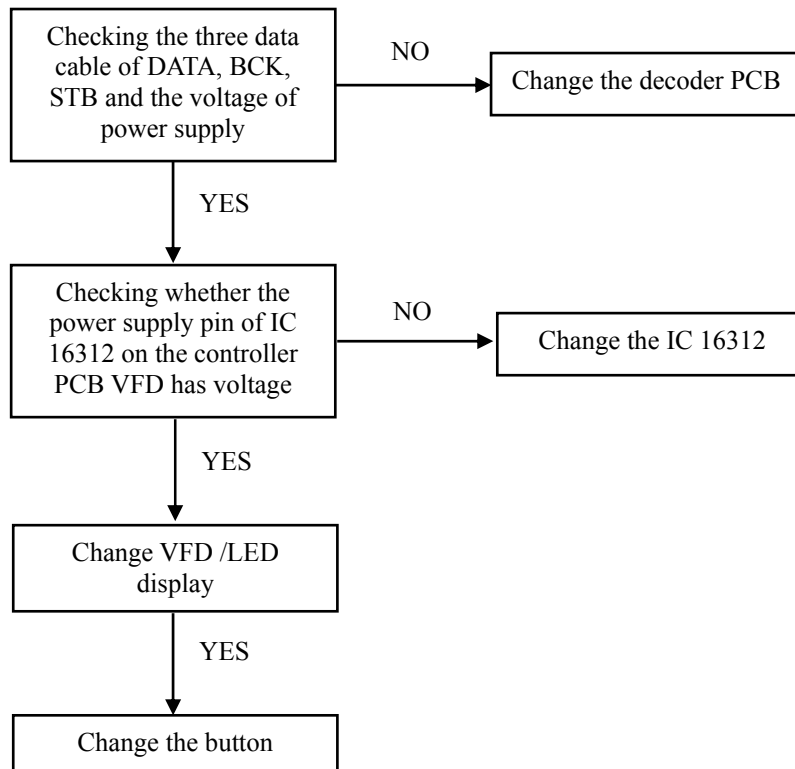
Video



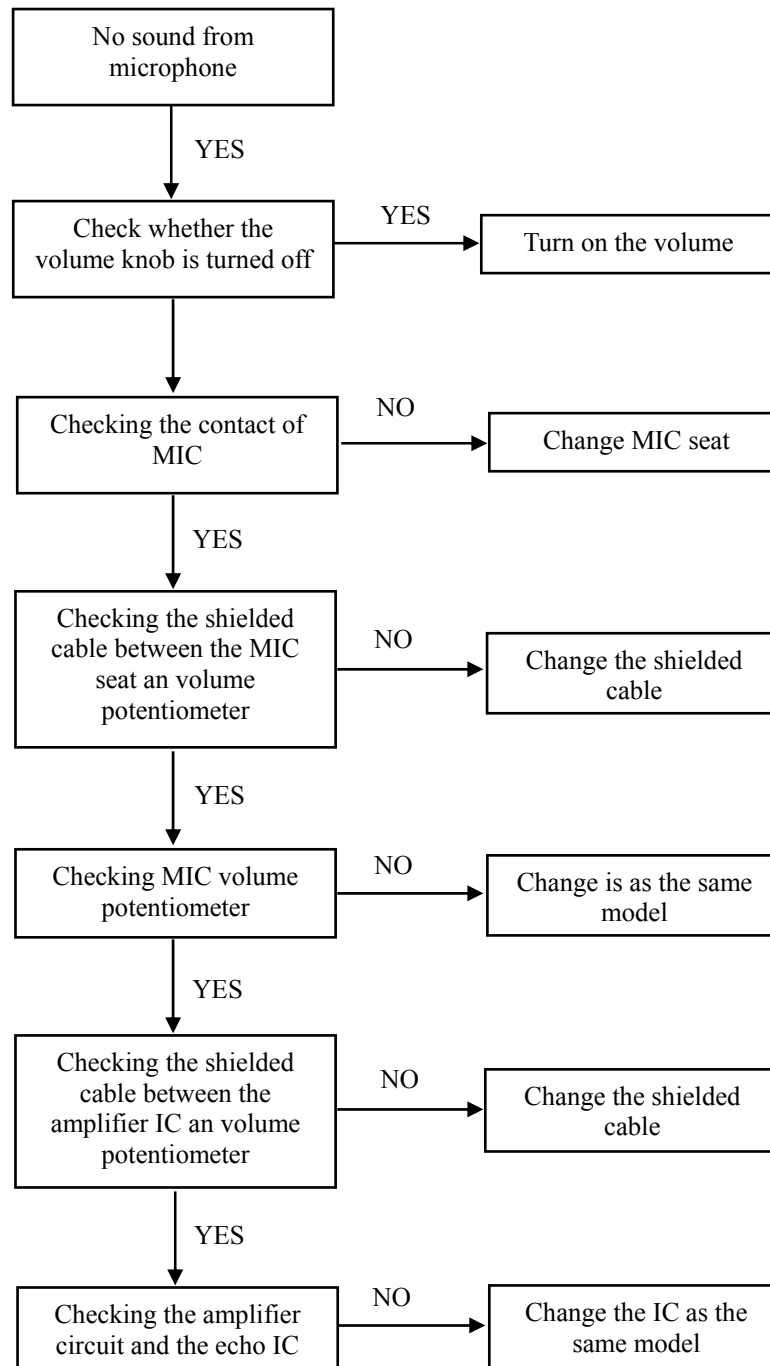
Decoder



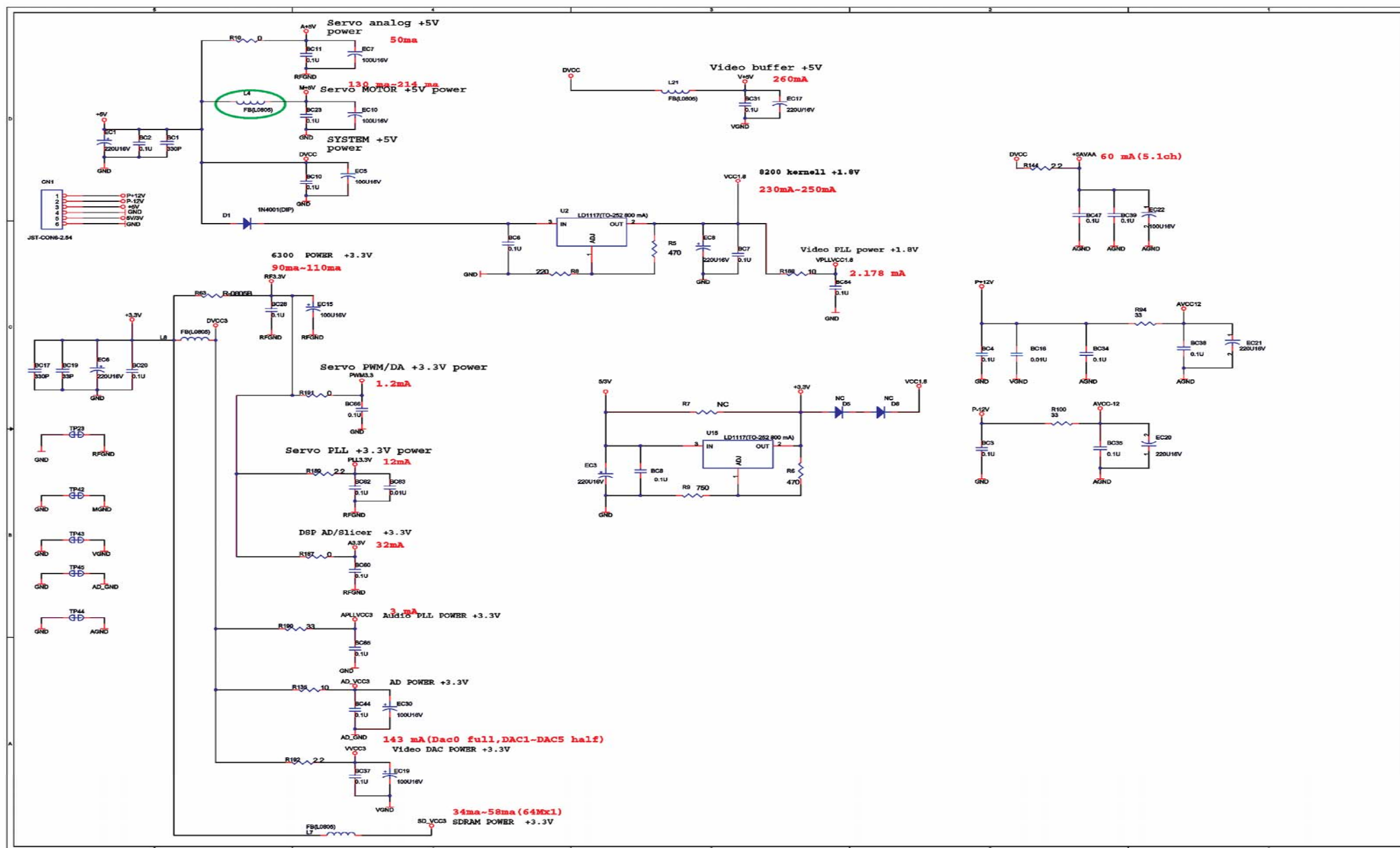
Panel Control



KARAOKE



Power board



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SUNPLUS — SPCA8200A + SPHE6300 + OUTPUT

Background

This DVD design is based on SUNPLUS SPCA8200A single chip DVD mpeg and servo processor. The SPCA8200A is built upon SUNPLUS proven Programmable Multimedia Processor architecture with integrated servo DSP. A complete DVD design using SPHE6300 RF-Amp can support all major popular optical pickup heads. With SPCA8200A unify memory architecture, the whole system memory is reduced to a minimum.

System Clock Requirement

SPCA8200A require a 27MHz clock to operate. This 27MHz can either be generated externally and feed into pin 77 and pin 79 or thru a 27MHz crystal attached to pin 78 and 77. This 27Mhz will be used for all video processing reference. In addition, internal multiplier will generate a much higher operating frequency for the internal RISC+DSP code to operate. Audio clock is generated from SPCA8200A by its internal PLL circuitry.

SDRAM Usage

SPCA8200A support the use of higher density 1Mx16 SDRAM. A sinlge of 1Mx32 SDRAM is sufficient for the whole system to operate.

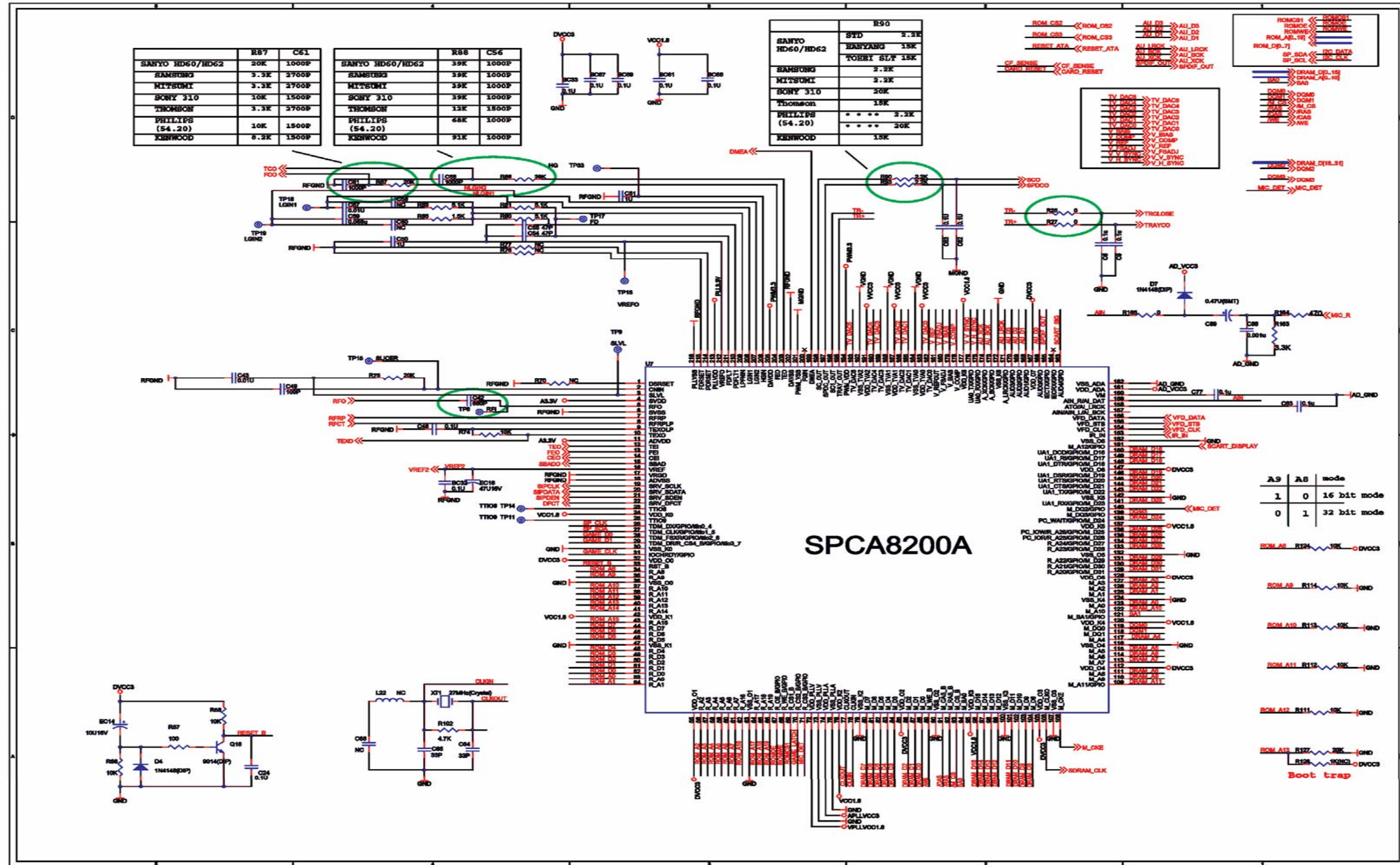
System Configuration

CHIP	FUNCTION
SPCA8200A	Single chip processor that handles all system control, DVD decoding and servo control.
16MBit SDRAM	Data storage and frame buffer
4M/8Mbit EPROM/FLASH	Program storage
24C02 SERIAL EE	System setup configuration storage
WM8726/WM8761	2-Channel AudioDAC
WM8746/WM8766	6-Channel AudioDAC

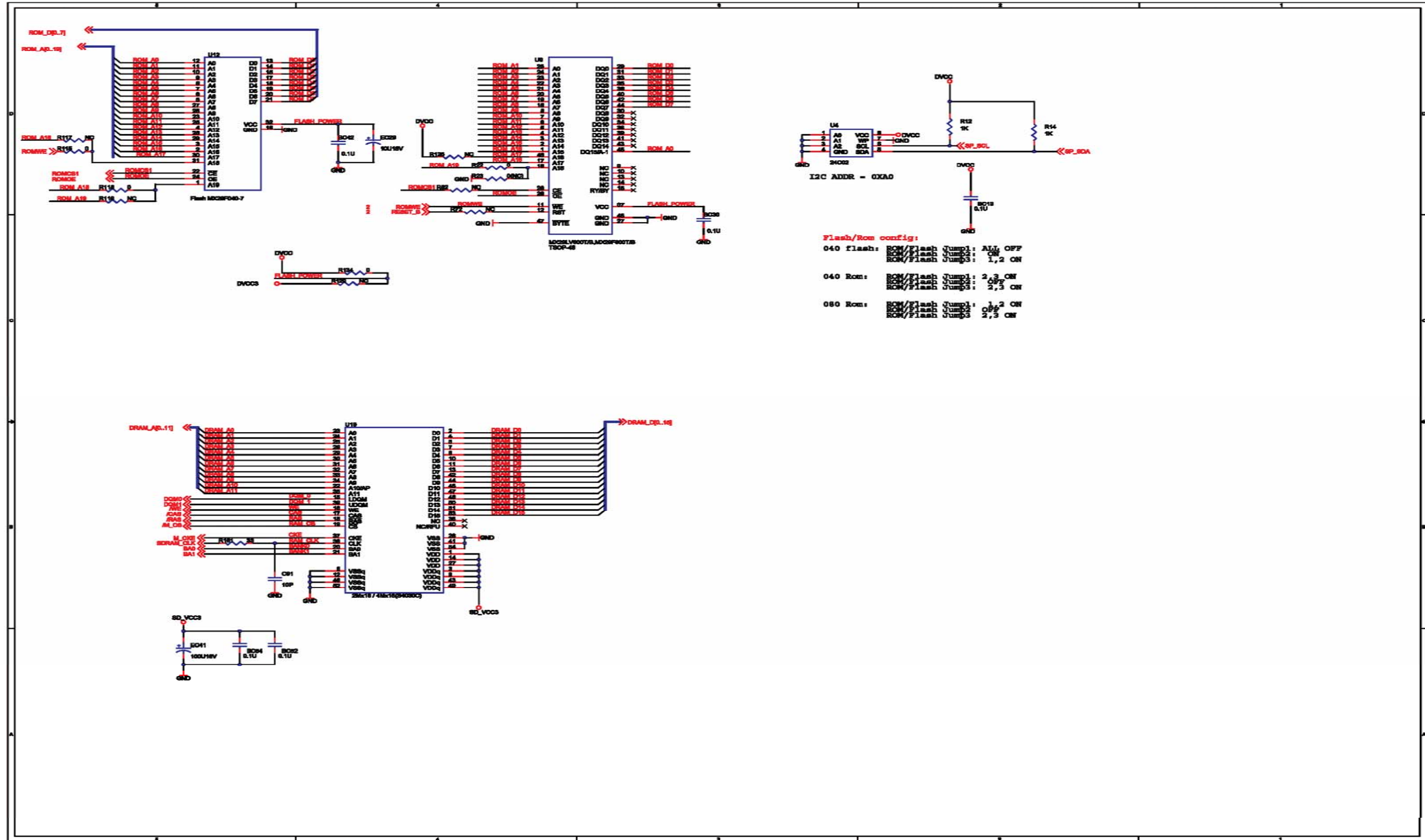
System I/O DEFINE

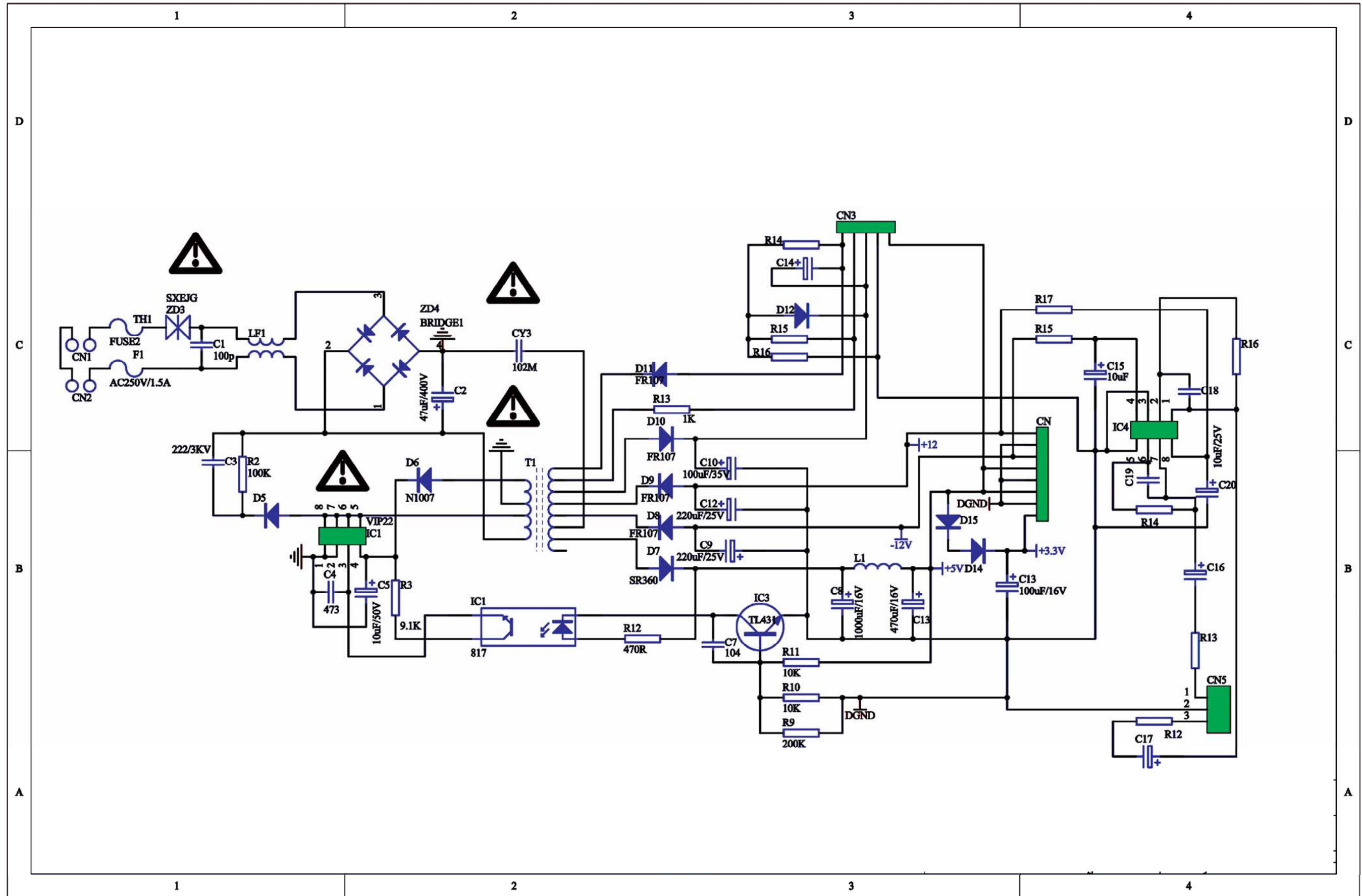
XGPIOx EAUXx AUXx	FUNCTION
TDM_DX/GPIO/ttio0_4	SP_CLK/12C_CLK
TDM_CLK/GPIO/ttio1_5	SP_SDA/12C_DATA
TDM_FSXR/GPIO/ttio2_6	GAME_D0
TDM_DR/R_CS4_B/GPIO/ttio3_7	GAME_D1
IOCHRDY/GPIO	GAME_CLK
RST_B	RESET_B
R_CS2_B/GPIO	GAME_LATCH
R_OE_B/GPIO	ROMOE
R_WE_B/GPIO	ROMWE
M_DQ2/GPIO	MIC_DET
M_BA1/GPIO	RST_AUDIO/MUTE
M_A12/GPIO	SCART_DISPLAY
IR_IN	IR_IN
VFD_CLK	VFD_CLK
VFD_STB	VFD_STB
VFD_DATA	VFD_DATA
AIN/AIN_L/AI_BCK (AIN_R/AI_DAT)	AIN
AUD4/GPIO	SCART_SIG
IECTX/GPIO	SPDIF_OUT
AUD0/GPIO	AU_D0
AUD1/GPIO	AU_D1
AUD2/GPIO	AU_D2
AUD3/GPIO	AU_D3
A_LRCK/GPIO	AU_LRCK
A_BCK/GPIO	AU_BCK
A_XCK/GPIO	AU_XCK
UA0_RX/GPIO	V_H_SYNC
UA0_TX/GPIO	V_V_SYNC

8200 DSP

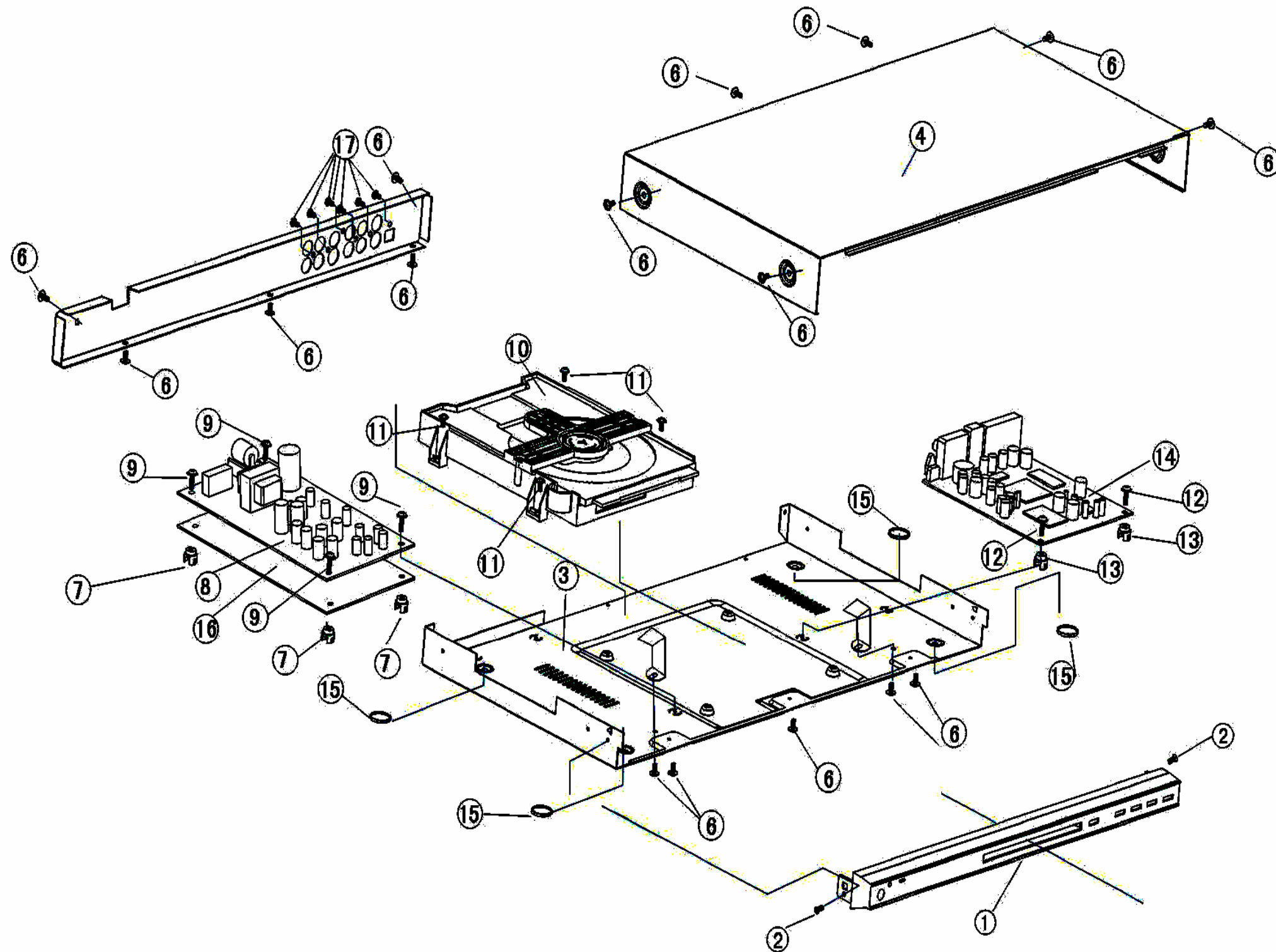


ROM /Flash /Memory





EXPLODED VIEW



PART LIST

No.	Part Name	Qty
1	Front Panel	1
2	Screw 3x10 PWM	2
3	Base Plate	1
4	Top Cover	1
5	Back Panel	1
6	Screw 3 x 6 PWM	18
7	8mm Tube	4
8	Power Board	1
9	Screw 3 x 10 PWM	4
10	Loader	1
11	Screw 3 x 8 PWM	2
12	Screw 3 x 12 PWM	2
13	8mm Tube	2
14	Decoder Board	1
15	Rubber Damper	2
16	JY-L08 Isolation Ring	1
17	PA 3x8	6
The data are subject to change without prior notice		