CIRCUIT DESCRIPTION

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1. Audio Circuit (Circuit diagrams Interface PWB)

1.1 Audio Input

The audio signal input received from the audio input terminal (J301) is applied to the amplifier I311 of 4 (L-CH) and 9 (R-CH) through the low-pass filter consisting of R396, R397, R398, R399, C431,C450 and C041.

In this amplifier, controls of Volume, and mute are conducted. The audio signal controlled at the pin 6 determines the attenuation of output of the amplifiers. Since then, the signal is output to the jack P308.

1.2 Audio Output

The audio signal is output from the plug P002 of the function key board then output to the internal speaker system via earphone jack (JK001),plug P004(R-CH) and plug P003(L-CH).

2. Power Supply (Circuit diagrams MAIN PWB)

2.1 Line Filter

Line filter consists of C801, T801, C803, C804. It eliminates high frequency interference to meet EMI's requirement.

2.2 Rec & Filter

Bridge diode D801 converts AC source into pulsed DC. This pulsed DC is smoothed and filtered by C805.R802 is an NTC (negative thermal coefficient) resistor, used to reduce inrush current to be within safe range.

2.3 Power Transformer

T802 converts energy from power source C805 to secondary side to generate +15V and +5V.

2.4 Output:

When driver Q803 is driven on and off by I801, pin 6 and pin 9 of T802 induce a square wave. This square wave is rectified by D809, D810, then filtered by C817, C822 to generate +15V and +5V respectively.

2.5 Driver : Q803

If the electrical potential of gate is larger than source by about 10 volts, Q803 turns on.

2.6 FB

Negative feedback CKT consists of photo coupler I802 and adjustable regulator I803. It can maintain output voltages +5V and +12V at a stable level.

2.7 PWM :

2.7.1 Start : When power is turned on, Q801 conducts due to bias from C805 and R803. Q801 supplies a 17 volt and a starting current about 0.3mA to pin 7 of I801. I801 starts to oscillate (R810, C813) and outputs a pulse train through pin 6 to drive Q803.

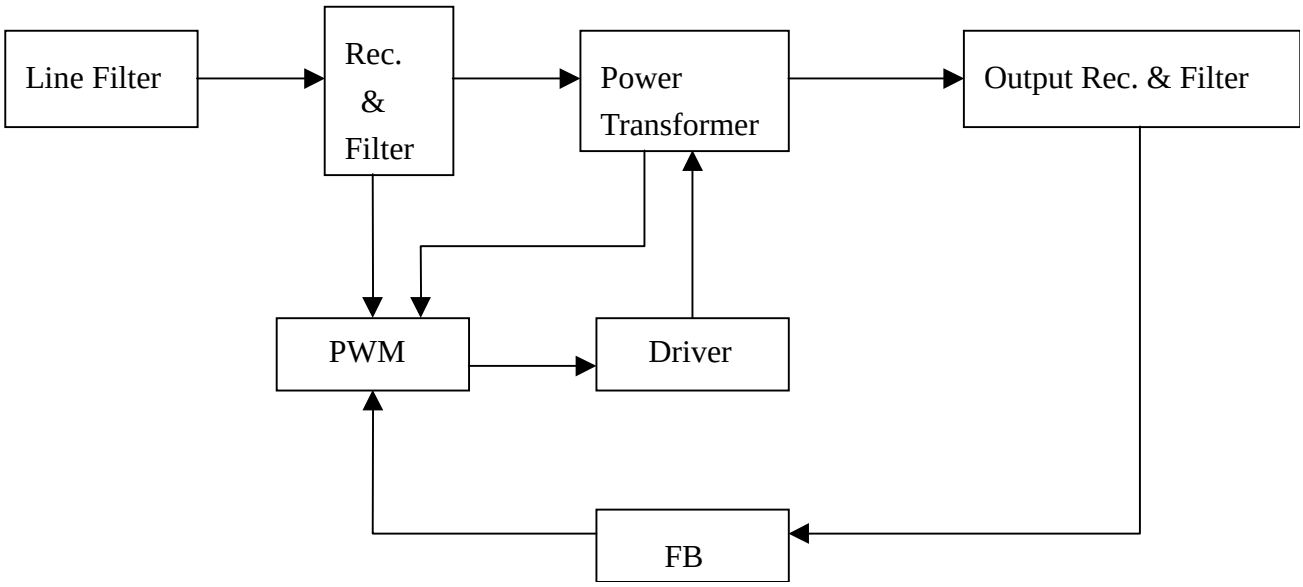
2.7.2 OPP : When Q803 turns on, C805 supplies a linearly increasing triangle current through the primary inductance of T802 to the driver Q803, once the peak value of this current multiplied by R811 exceeds1 volt, pulse train will be shut down immediately to protect Q803, T802 from being burned out.

2.7.3 Regulation : If output voltage +5V goes up, the R terminal of I803 gets more bias, accordingly photo transistor and photo diode flows more current. The voltage of pin 2 goes up too, making the pulse width of pin 6 to become narrower. So the output voltage +5V will be pulled down to a stable value.

2.7.4 OVP : If +5V goes up too much, the induced voltage on pin 4 of T802 becomes large also. Suppose that it is over 18 volts, ZD801 conducts, pin 3 of I801 is pulled up over 1 volt. The pulse train at pin 6 goes down to zero, shutting Q803 off completely.

2.7.5 SCP : If output terminal is short to ground, photo transistor does not conduct, hence Q806 does not conduct either. Then oscillation of I801 is stop, shutting Q803 off completely.

LCD 1560VM Power Board Block Diagram



3. On-screen Circuit (Circuit diagrams Interface PWB)

I303 (gm5110) Embeded function.

On-screen menu screen is established and the resultant data are output from I306 (Circuit diagram Interface PWB, gm5110).

4. Video input Circuit (Circuit diagram Interface PWB)

1. The AC-coupled video signal is used to clamp the black level at 0V for the DSUB input port.
2. A TMDS data and clock signal is used for the DVI-D input connector.

5. Definition Converter LSI Peripheral Circuit (Circuit diagram interface PWB)

I336 gm5110 is the definition converter LSI.

The analog R,G,B signal input entered from the video input circuit is converted into the digital data of video signal through the incorporated A/D converter. Based on this conversion, this device performs interpolation during pixel extension. The source voltage for this device is 3.3V and the system clock frequency is 14.318MHz. The withstand voltage level for the input signal voltage is 3.3V and 5V.

6. System reset, LED Control Circuit (Circuit diagram Interface PWB)

6.1 System reset

System reset is performed by detecting the rising and falling of the 5V source voltage at I307.

6.2 LED control circuit

Green / amber is lit with the control signal of the LED GREEN and LED AMBER signal pin 121, 122 from I303 (Circuit diagram Interface PWB).

7. E^2PROM for PnP (Circuit diagram Interface PWB)

Data transfer between I301, I304, I309 and host.

There are two forms of communications protocal. In both, display capabilities are retrieved by the system software during the boot-up and configuration time.

For the PC platform, this software layer is defined in the VESA BIOS Extension / Display Data Channel, DDC2B/DDC CI, standard.

8. E^2PROM (Circuit diagram Interface PWB)

Data transfer between I306 (24LC16B) and LSI (Circuit diagram Interface PWB page 4/8(I303)) is effected through the IIC bus SCL (pin 52) and SDA (pin 51) of I303. The data to be transferred to each device are stored in I306.

- I303 control data.
- OSD related setting data.
- Other control data for service menu.

9. CPU Circuit (Circuit diagram Interface PWB)

I303 (gm5110) embeded microcontroller with parallel ROM interface (I305).

The source voltage for the device is 3.3V and the system clock frequency is 14.318MHz.

9.1 Detection of POWER Switch Status

The I303 identifies the ON status of the two power supplies. The identification is made when the power supply is turned off. For example, if the power supply is turned off with the POWER switch, the POWER switch must be turned on when activating the power supply again. If the power supply is turned off by pulling out the power cord, then this power supply can be turned on by connecting the power cord, without pressing the POWER switch.

9.2 Display Mode Identification

9.2.1 Functions

(1) Display mode identification

- The display mode of input signal is identified based on Table 1, and according to the frequency and polarity (HPOL, VPOL) of horizontal or vertical sync signal, presence of the horizontal or vertical sync signal, and the discrimination signal (HSYNC_DETECT, VSYNC_DETECT).
- When the mode has been identified through the measurement of horizontal and vertical frequencies, the total number of lines is determined with a formula of “Horizontal frequency / Vertical frequency = Total number of lines. “Final identification can be made by examining the coincidence of the obtained figure with the number of lines for the mode identified from the frequency.
- When the detected frequency if the sync signal has changed, the total number of lines should be counted even through it identified frequency in the same mode. Then, it is necessary to examine whether the preset value for the vertical display position of Item 4-3 has exceeded the total number of lines. If exceeded, a maximum value should be set up, which does not exceed the vertical display position of Item 4-3.

(2) Out of range

This out-of-range mode is assumed when the frequency of the horizontal / vertical signal is as specified below.

- Vertical frequency : Below 56.2Hz or above 75.1Hz
- Horizontal frequency : Below 31.5KHz or above 60KHz

(3) Power save mode.

The power save mode is assumed when the horizontal / vertical signals are as specified below.

- If there is no horizontal sync signal input.
- If there is no vertical sync signal input.
- If the horizontal sync signal outside the measuring range of gm5110.
- If the vertical sync signal outside the measuring range of gm5110.

Table 1

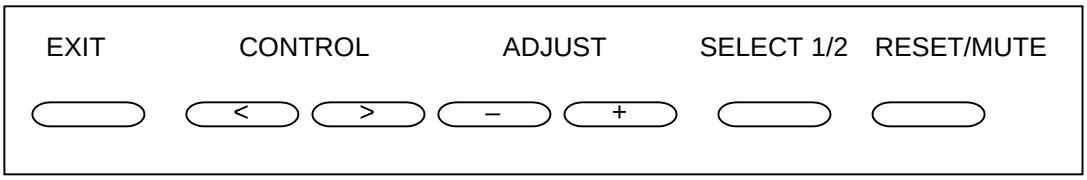
Mode	No	Resolution	H-freq (KHz)	Band Width (MHz)	Polarity	
					H	V
1.	247	VGA 720 x 350 70Hz	31.47	28.322	+	-
2.	102	VGA 720 x 400 70Hz	31.47	28.322	-	+
3.	103	VGA 640 x 480 60Hz	31.47	25.175	-	-
4.	182	MAC 640 x 480 66Hz	35	32.24	-	-
5.	173	VESA 640 x 480 72Hz	37.86	31.5	-	-
6.	109	VESA 640 x 480 75Hz	37.5	31.5	-	-
7.	104	VESA 800 x 600 56Hz	35.16	36	+	+
8.	116	VESA 800 x 600 60Hz	37.88	40	+	+
9.	110	VESA 800 x 600 75Hz	46.88	49.5	+	+
10.	117	VESA 800 x 600 72Hz	48.08	50	+	+
11.	108	MAC 832 x 624 75Hz	49.72	57.283	-	-
12.	118	VESA 1024 x 768 60Hz	48.36	65	-	-
13.	217	SUN 1024 x 768 65Hz	52.45	70.49	-	-
14.	157	VESA 1024 x 768 70Hz	56.48	75	-	-
15.	141	VESA 1024 x 768 75Hz	60.02	78.75	+	+

Attention:

1. When resolution beyond 1024 x 768 is inputted, resolution is lowered with Down scaling to 1024 x 768, and indicated, and OSD should indicate OUT of Range.

9.3 User Control

General Key Description



Exit : Turn off OSM menu, Exit sub menu.

Control : Move the green cursor and select control items.

Adjust : Change the value of each function / Enter to submenu / Proceed auto adjust / Proceed reset

Select 1/2 : Move the NEXT tag / Input signal select.

Reset/Mute : Reset the select item (Open reset warning before reset) / Mute the speaker / headphone sound (short cut: when no OSM menu is shown)

9.3.1 Related Ports of I303

Port	Pin No.	I/O	Signal name	Function	Remarks
GPIO8	39	I/O	RESET/ Mute	RESET switch input MUTE switch input	The set value is returned to the initial value
GPIO10	49	I/O	EXIT	EXIT switch input	Withdraw from OSD
GPIO6	46	I/O	DOWN	– switch input	(–)key
GPIO3	43	I/O	UP	+ switch input	(+)key
GPIO9	48	I/O	LEFT	< switch input	(<)key
GPIO7	47	I/O	RIGHT	> switch input	(>)key
GPIO2	42	I/O	SELECT 1/2	SELECT 1/2 switch input	

9.3.2 Functions

Control is effected for the push-switches to be used when the user changes the parameters, in order to modify the respective setting values. Whether the switch has been pressed is identified with the switch input level that is turned “L”.

Each switch input port is pulled up at outside of I303.

Each parameter is stored in the EEPROM, the contents of which are updated as required.

9.4 Control of Definition Converter gm5110 (I303)

9.4.1 Ports related to control

Pin No.	I/O	Signal name	Function
51	I/O	SDA	Gm5110 serial data
52	I/O	SCL	Gm5110 serial clock
207	I/O	HDATA2	Gm5110 address input
208	I/O	HDATA1	Gm5110 address input

9.4.2 Functions

Major function of I303 are as follows:

(1) Expansion of the display screen.

(2) Timing control for various signal types.

(3) Power-supply sequence (LCD panel).

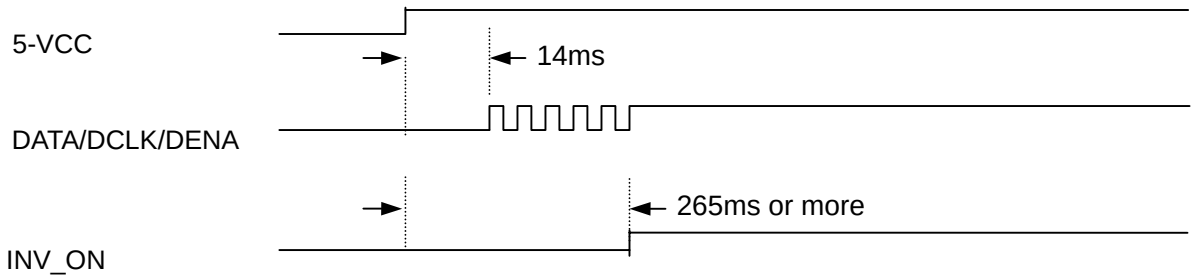
9.5 I^2C Bus Control

9.5.1 Related Ports of I303

Pin No.	I/O	Signal name	Function
52	I/O	IICCLK	IIC bus clock
51	I/O	IICDATA	IIC bus data

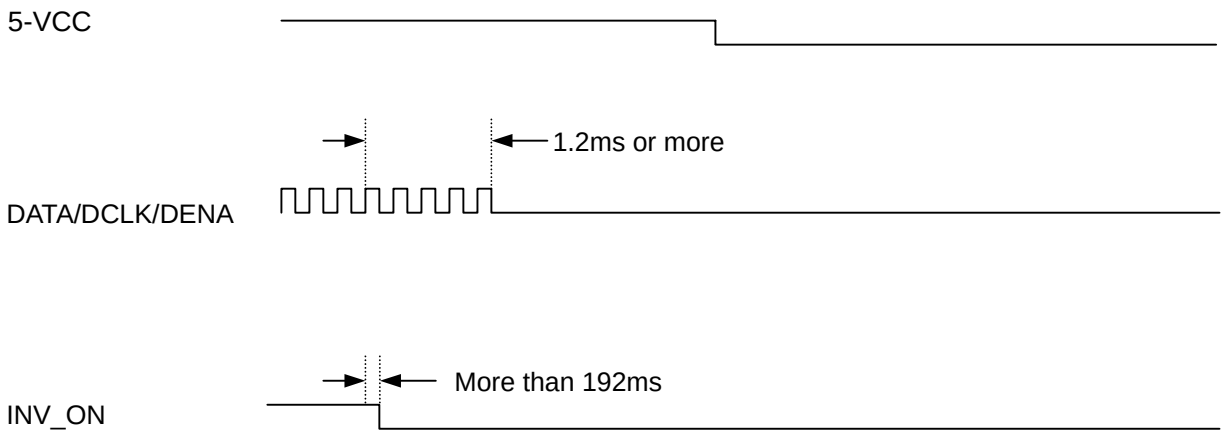
9.6 Power ON Sequence

When the POWER switch is pressed, the POWER OFF signal is turned “H”. When this “H” potential is detected, the I303 begins to establish the respective power supplies according to the sequence shown below.



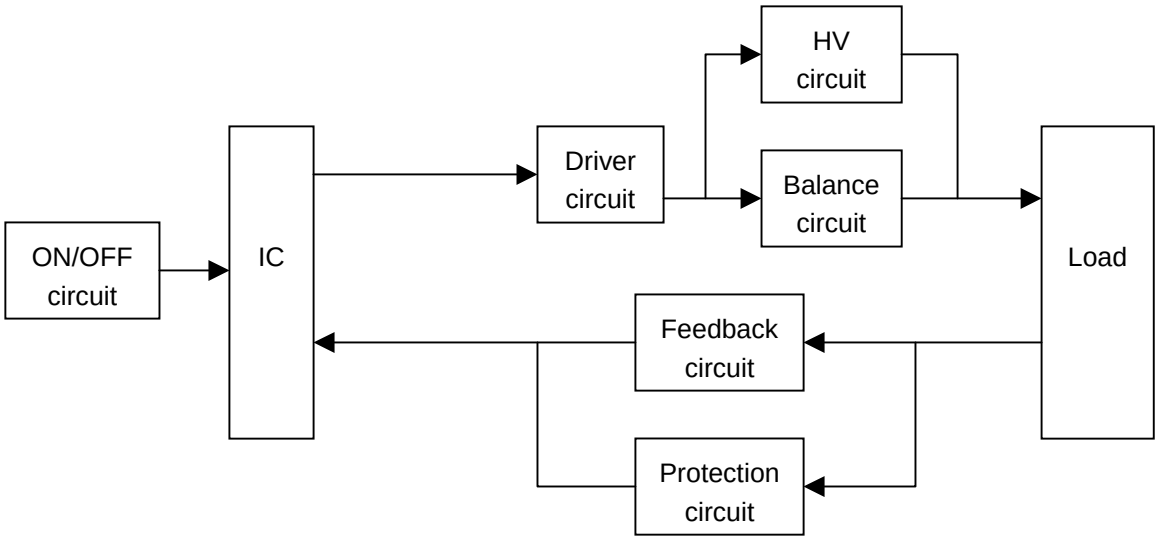
9.7 Power OFF Sequence

When the POWER switch is pressed while the power supply is ON, the POWER ON signal is turned “H”. When shown below. His “H” potential is detected, the I303 begins to turn off the respective power supplies according to the sequence.



10. Inverter

10.1 Circuit Diagram



10.2 Inverter Basic Function

This is DC-AC Inverter which is developed for driving 4 Cold Cathode Fluorescent Lamp (CCFL) in LCD panel.

10.3 Circuit Explain

10.3.1 ON/OFF Circuit:

This is an input signal to turn on or off the AC output voltage of the Inverter.

ON state : On/Off pin ≥2.5V

OFF state : On/Off pin ≥2.0V

10.3.2 IC (Oz960)

It will get the input signal from customer system and control the lamps current and brightness.

The other function include burst mode control, and soft start, over voltage protect.

10.3.3 Driver Circuit

The driver circuit used full bridge frame. The circuit include two N-MOS and two P-MOS.

Adjusting the overlap conduction between Q50, Q51, Q52, Q53.

The CCFL current regulation is achieved. At specific CCFL current, the input power is maintaned constant.

10.3.4 H/V and Balance Circuit

The H/V circuit connect to the lamps and supply the power to drive the lamps. The balance circuit is use L,C,R resonant to control the output current. It can get the same output current even the load is different.

10.3.5 Feedback Current

The sens voltage of the feedback is set at 1.25V voltage. And the IC compare the sens voltage with output current ,and release the control signal to PWM.

10.3.6 Protection circuit

The protection circuit is sence the output current and abnormal signal to protect the inverter.

(1) For output current

The protect circuit will be monitor the lamps current. If the lamps current is correct, it will be allow the inverter to operating continually. In other ward if the lamps current is abnormal it will be shutdown the inverter.

(2) For other abnormal signal in the inverter

If something wrong at power stage, the protect circuit will be shutdown the inverter.