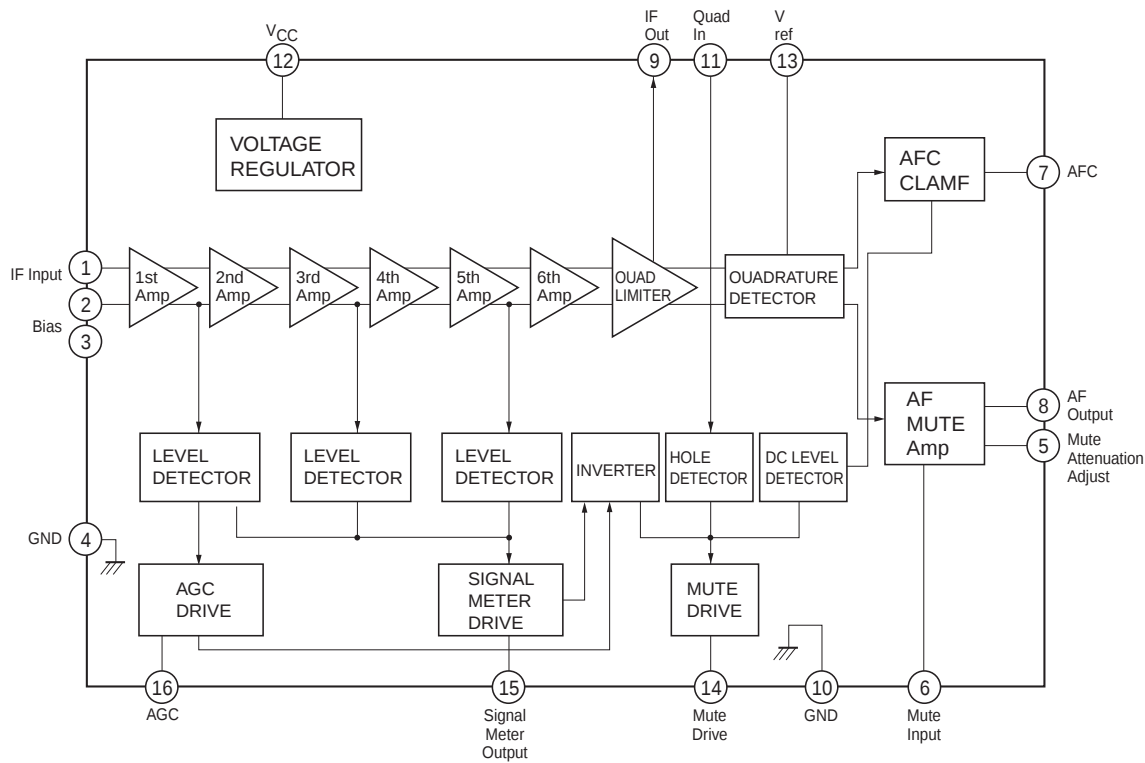
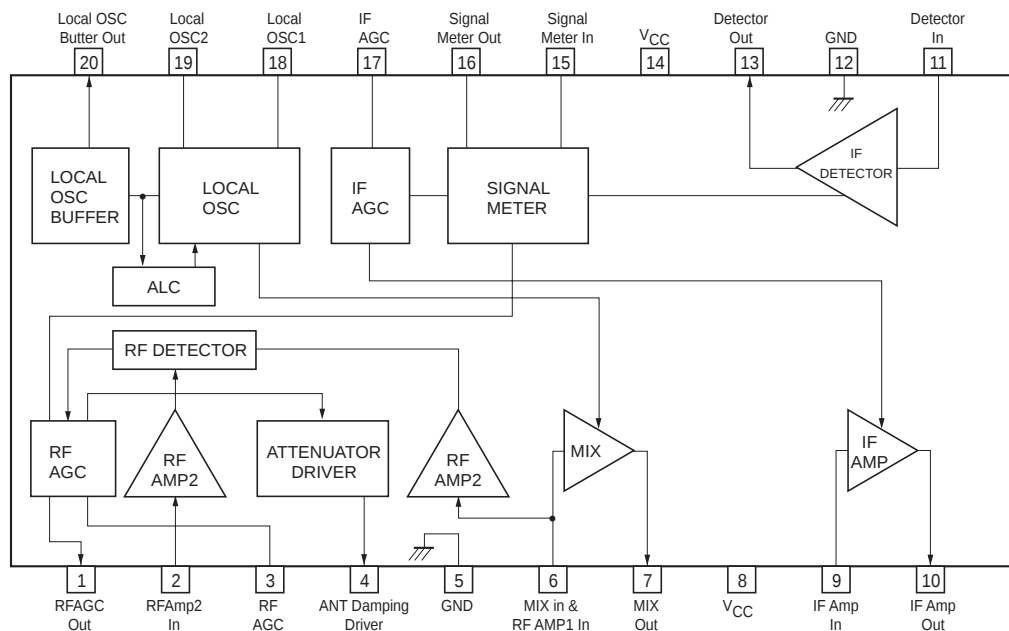


5. INTERNAL BLOCK DIAGRAM of Ics

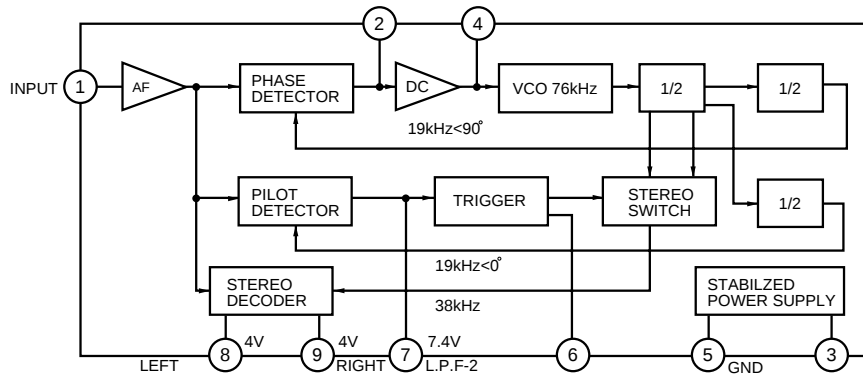
■ IC101 DBL 1018



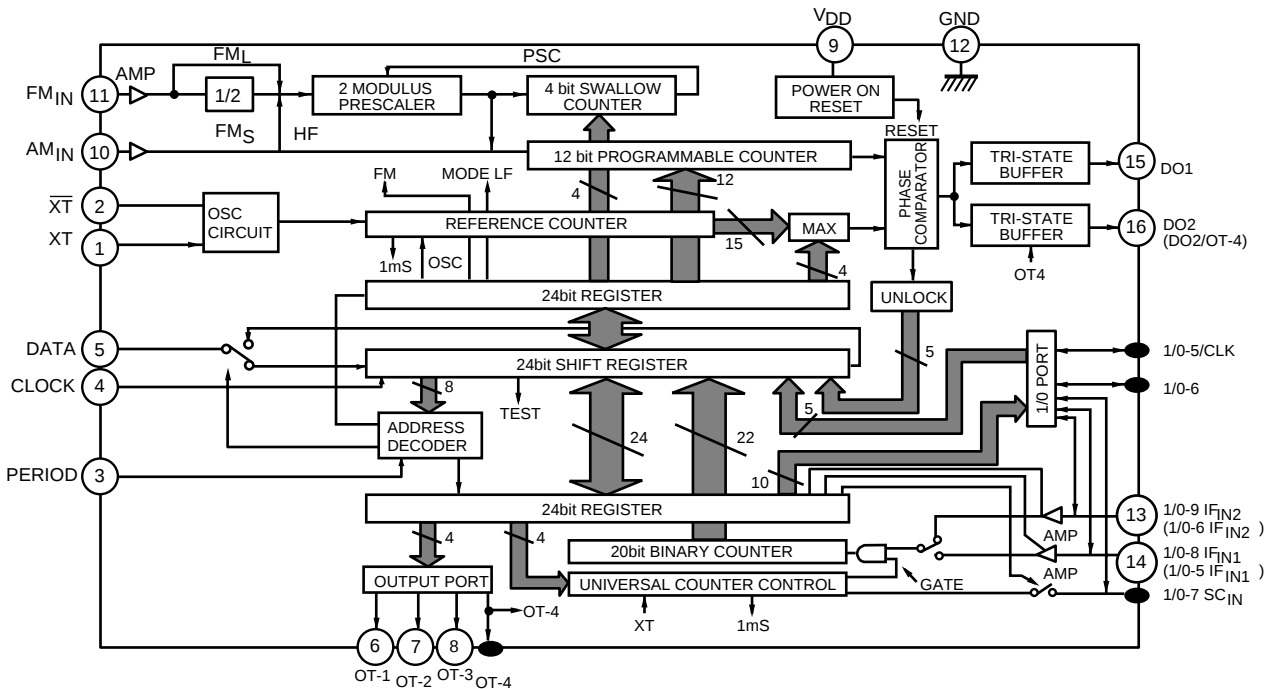
■ IC201 DBL 1019



■ IC301 KIA6043S



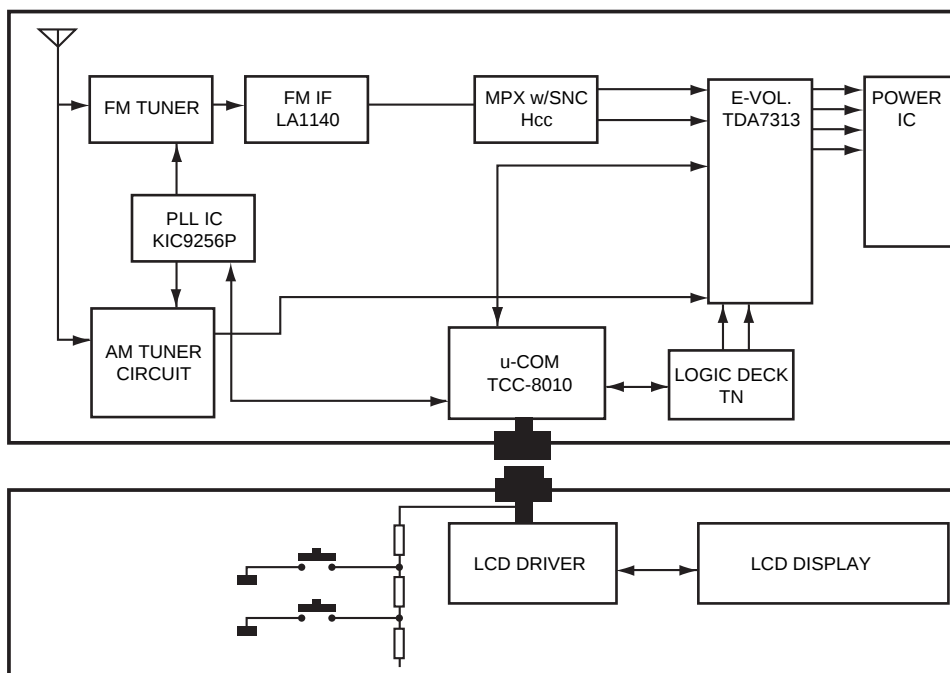
■ IC401 KIC9256P



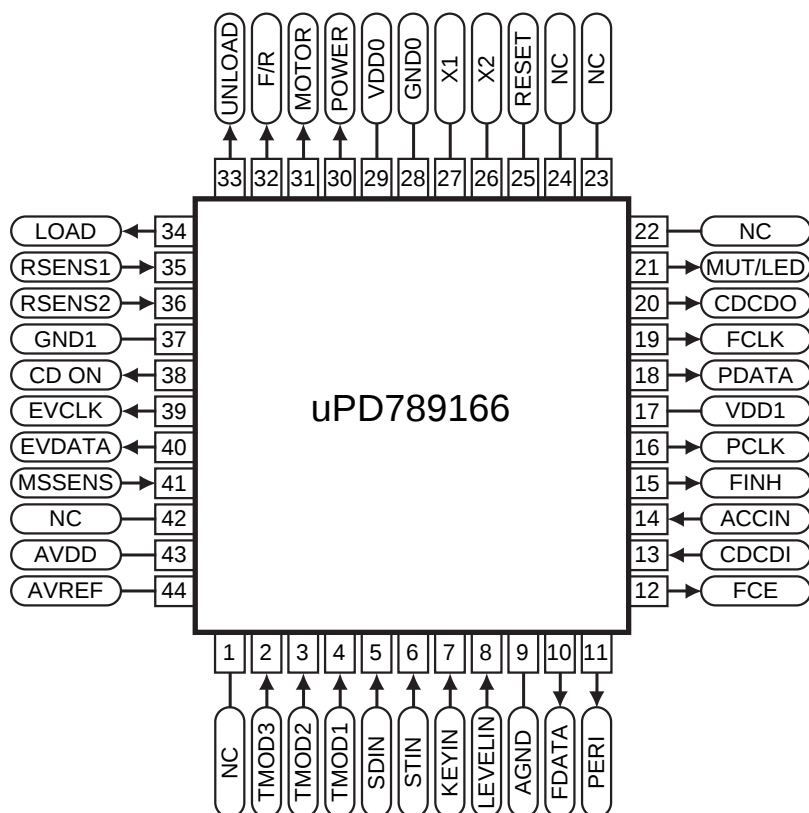
NOTE: Mark terminals are not existence in KIC9256P, KIC9256F
Terminal name of KIC9256P, KIC9256F is shown in parentheses.
Others are common terminals.

■ IC402 uPD789166

1) Overall block diagram



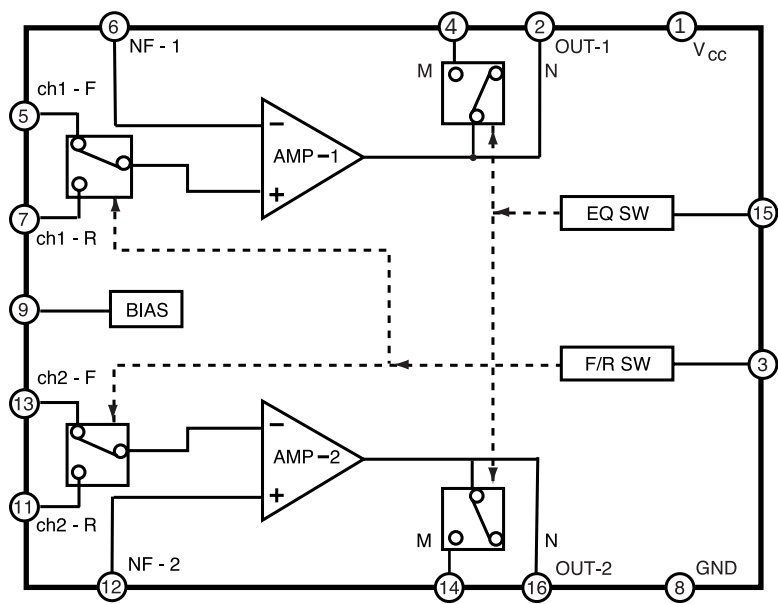
2) Pinning overview



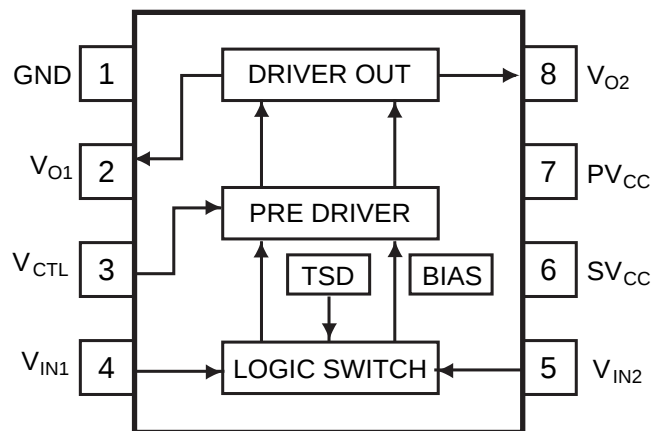
3) Pin function

PIN	Port	P-NAME	I/O	Act	DESCRIPTION	When not used	REMARK
1	P60	NC			NO CONNECTION		
2	P61	TMOD3	I		Tape mode detect input3		
3	P62	TMOD2	I		Tape mode detect input2		
4	P63	TMOD1	I		Tape mode detect input1		
5	P64	SDIN	I		Tuner SEEK Stop detect input.		
6	P65	STIN	I		FM Stereo detect input(LOW='ST' ON)		
7	P66	KEYIN	I		A/D Key input. Used for also front panel detecting. Less than 0.17V: regarded as the panel opened.		
8	P67	LEVELIN	I		Dancing level detect input.		
9		AGND			Analog GROUND		
10	P10	FDATA	O		Front(LCD driver) data communication output. Diode matrix DIO IN0 line		
11	P11	PERI	O		PLL IC Period communication output. Diode matrix DIO OUT2 line		
12	P30	FCE	O I		Front(LCD driver) CE communication output. Diode matrix DIO IN1 line		
13	P31	CDCDI	I		CD CHANGER Data input.		
14	P32	ACCIN	I	L	ACC Detect input(LOW = ACC ON)		
15	P33	FINH	O		Front(LCD driver) INH communication output.		
16	P20	PCLK	O	O	PLL IC clock communication output. Diode matrix DIO OUT0 line		
17		VDD1					
18	P21	PDATA	O		PLL IC data communication output. Diode matrix DIO OUT1 line		
19	P22	FCLK	O		Front(LCD driver) Clock communication output. Diode matrix DIO IN2 line		
20	P23	CDCDO	O		CD CHANGER Data output.		
21	P24	MUT/LED	O		Used as power IC mute. (LOW = MUTE) Used as blinking LED.		
22		IC0					
23		XT2					
24		XT1					
25		RESET					
26		X2					
27		X1					
28		VSS0					
29		VDD0					
30	P25	POWER	O	H	When system is on, this port is used as power out port.		
31	P26	MOTOR	O	H	Main motor out port.(HIGH = MOTOR ON)		
32	P00	F/R	O		Direction select output. LOW = Forward play. High = Rewind play.		
33	P01	UNLOAD	O	H	Sub motor unload output.		
34	P02	LOAD	O	H	Sub motor load output.		
35	P03	RSENS1	I		Reel pulse1 input.		
36	P04	RSENS2	I		Reel pulse2 input.		
37		VSS1					
38	P05	CDON	O	H	When CDC mode, this port is high output.		
39	P50	EVCLK	O		Electric volume IC clock communication output.		
40	P51	EVDATA	O		Electric volume IC data communication output.		
41	P52	MSSENS	O	L	When TAPE mode, this port is tape signal detect input.		
42	P53	NC			NO CONNECTION		
43		AVDD			Analog VDD		
44		AVREF			A/D convert reference voltage input.		

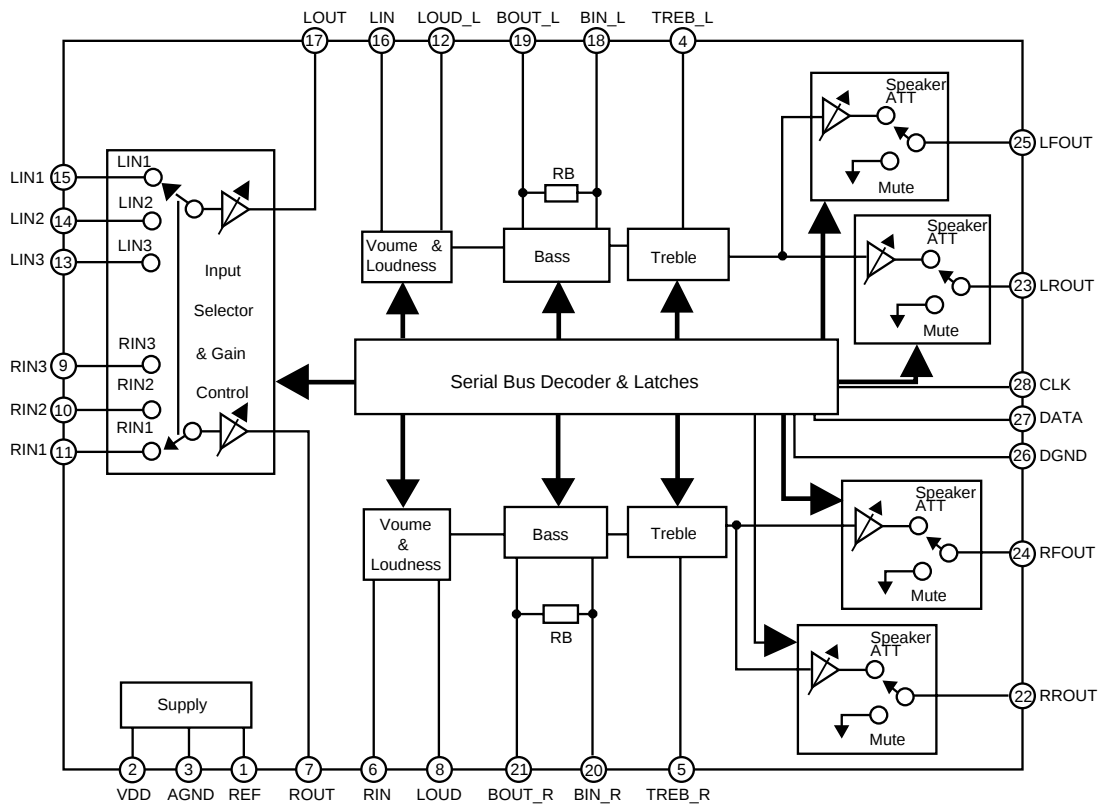
■ IC501 KIA2025



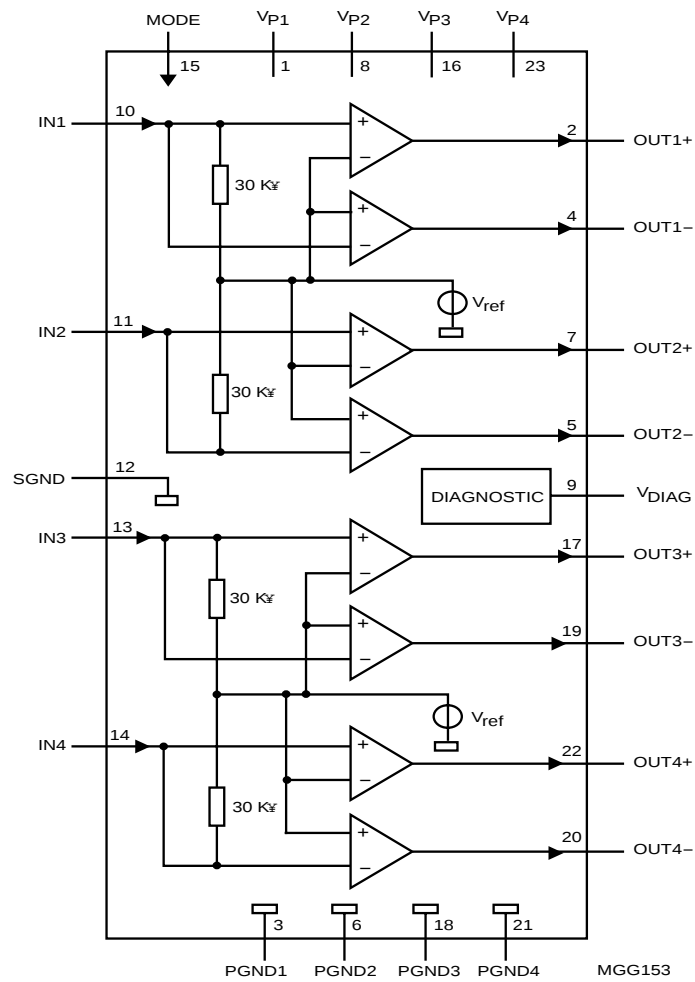
■ IC502 FAN8082



■ IC601 PT2313L



■ IC801 TDA8571J



■ IC901 LC75833E

