



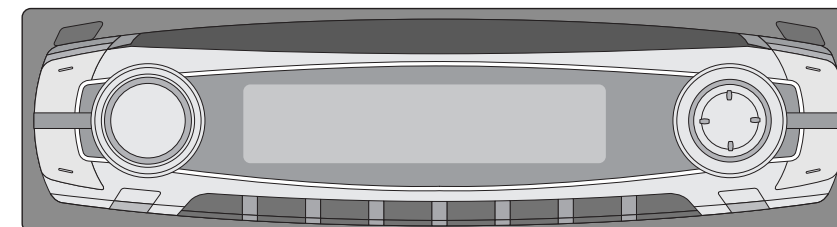
SERVICE MANUAL MODEL:LAC-M3600/LAC-M3600R



DETACHABLE FRONT PANEL CAR CD RECEIVER SERVICE MANUAL

CAUTION

BEFORE SERVICING THE UNIT, READ THE "SAFETY PRECAUTIONS"
IN THIS MANUAL.



MODEL:LAC-M3600/LAC-M3600R

LG Electronics Inc.

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SECTION 1. SUMMARY

□ SERVICING PRECAUTIONS

❶ Always disconnect the power source before:

- 1) Removing or reinstalling any component, circuit board, module or any other instrument assembly.
- 2) Disconnecting or reconnecting any instrument electrical plug or other electrical connection.
- 3) Connecting a test substitute in parallel with an electrolytic capacitor in the instrument.

CAUTION: A wrong part substitution or incorrect polarity installation of electrolytic capacitors may result in an explosion hazard.

❷ Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.

❸ Do not apply power to this instrument and or any of its electrical assemblies unless all solid-state device heat sinks are correctly installed.

❹ Always connect a test instrument's ground lead to the instrument chassis ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.

- 1) The service precautions are indicated or printed on the cabinet, chassis or components. When servicing, follow the printed or indicated service precautions and service materials.
- 2) The Components used in the unit have a specified conflammability and dielectric strength. When replacing any components, use components which have the same ratings. Components marked in the circuit diagram are important for safety or for the characteristics of the unit. Always replace with the exact components.
- 3) An insulation tube or tape is sometimes used and some components are raised above the printed writing board for safety. The internal wiring is sometimes clamped to prevent contact with heating components. Install them as they were.
- 4) After servicing always check that the removed screws, components and wiring have been installed correctly and that the portion around the service part has not been damaged. Further check the insulation between the blades of attachment plug and accessible conductive parts.

❑ ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

CAUTION. GRAPHIC SYMBOLS

	THE LIGHTNING FLASH WITH APOWHEAD SYMBOL. WITHIN AN EQUILATERAL TRIANGLE, IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF UNINSULATED "DANGEROUS VOLTAGE" THAT MAY BE OF SUFFICIENT MAGNITUDE TO CONSTITUTE A RISK OF ELECTRIC SHOCK.
	THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.

SPECIFICATIONS

1. GENERAL

Power requirements	DC12V~15V
Ground system	Negative
Dimensions(W x H x D)	188 x 58 x 166mm
Weight	Net: 1.3kg

2. RADIO SECTION

	FM	AM(MW)
Frequency range	65.0~74.0MHz(Optional), 87.5~108MHz	522~1,620kHz (Optional:530~1,710kHz/ 520~1,620kHz)
Intermediate frequency	10.8MHz	450kHz
Usable sensitivity	10dB μ V	28dB μ V
Signal to noise ratio	55dB	45dB

3. COMPACT DISC SECTION

Frequency response	40Hz~20kHz
Channel separation (Line out)	90dB (1kHz)
Signal to noise ratio (Line out)	110dB

4. AUDIO SECTION

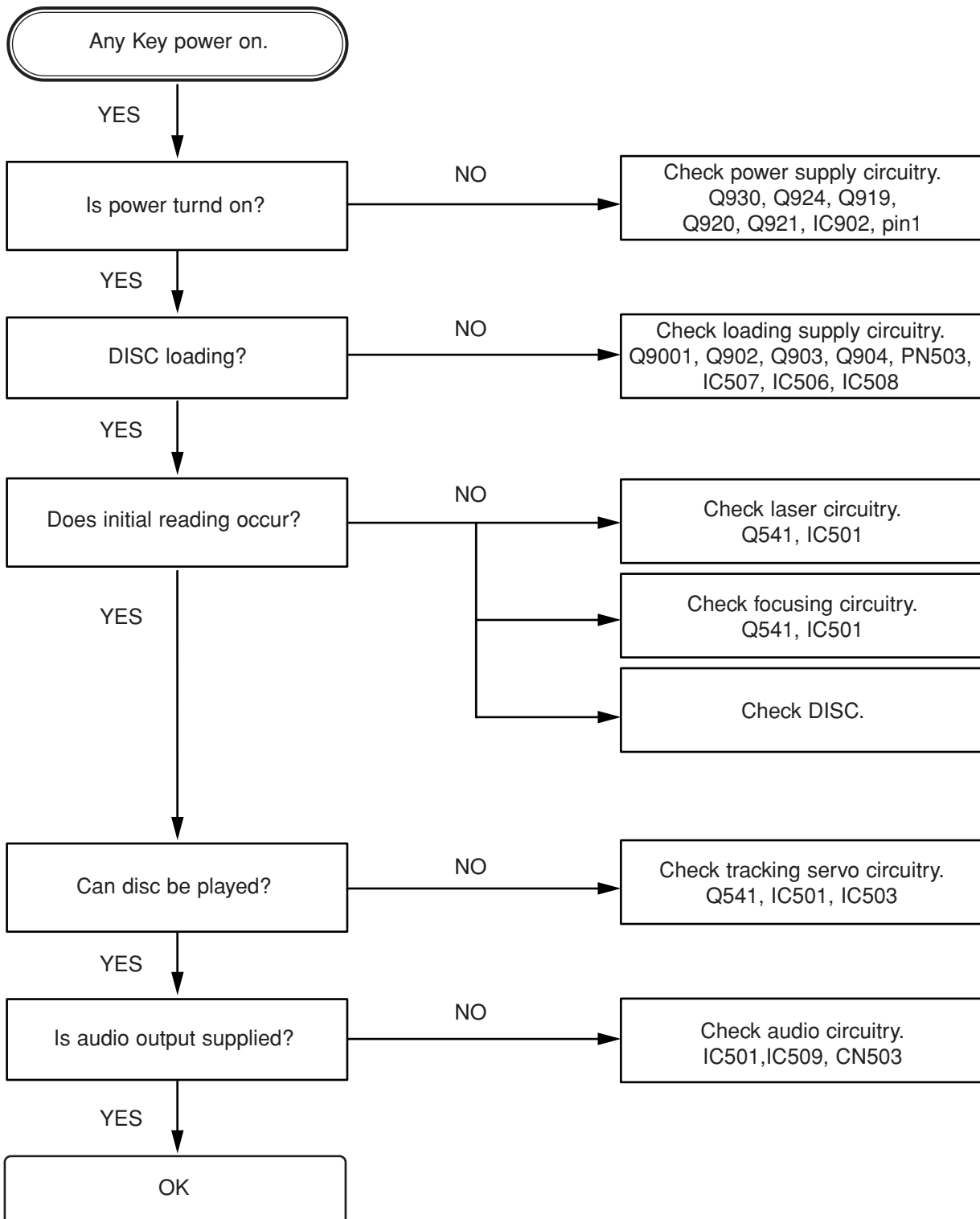
Maximum output power	50W x 4
Speaker impedance	4 Ω x 4 or 8 Ω x 4

NOTE: The design and specifications are subject to change without notice in the source of product improvement.

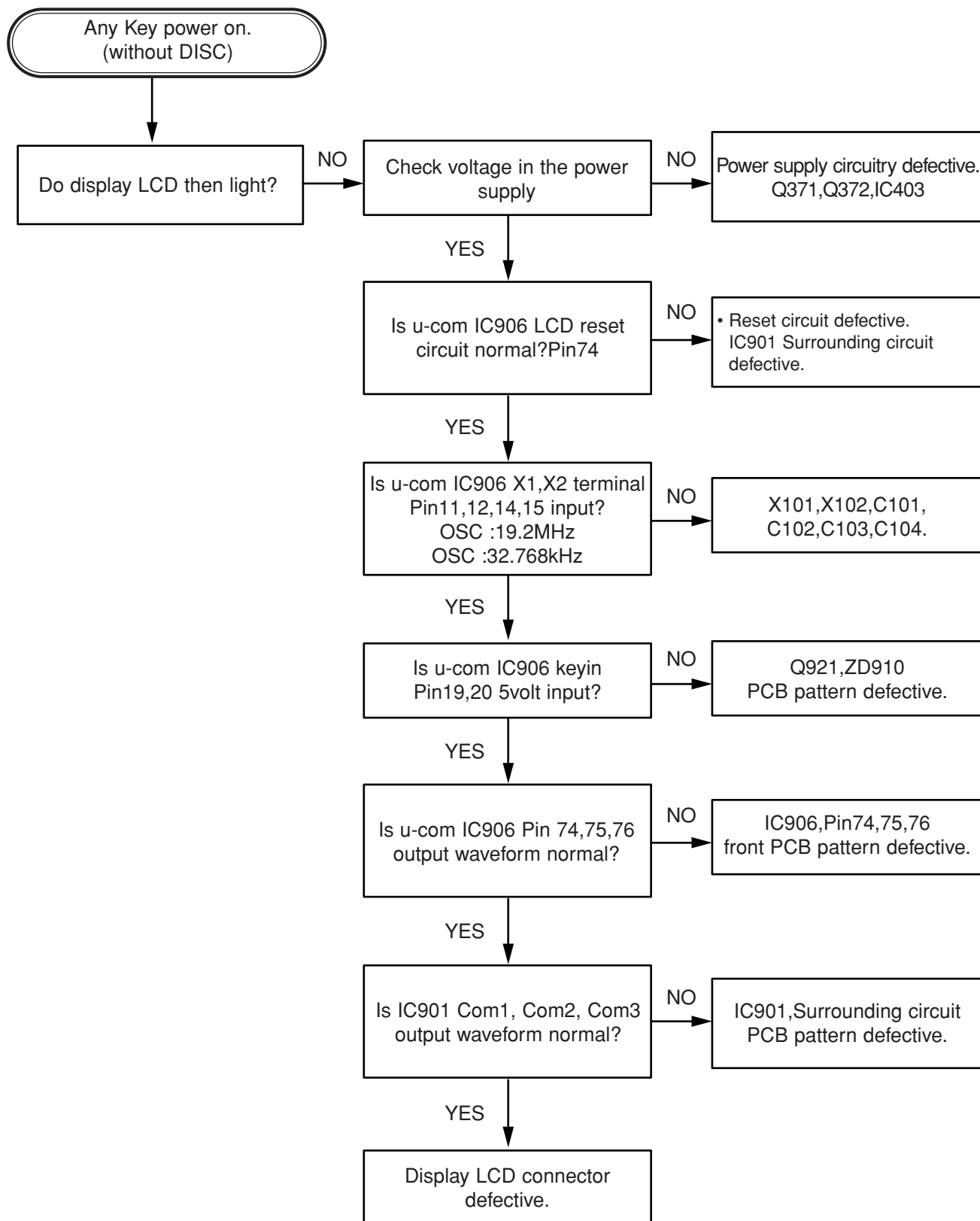
SECTION 2. ELECTRICAL

□ ELECTRICAL TROUBLESHOOTING GUIDE

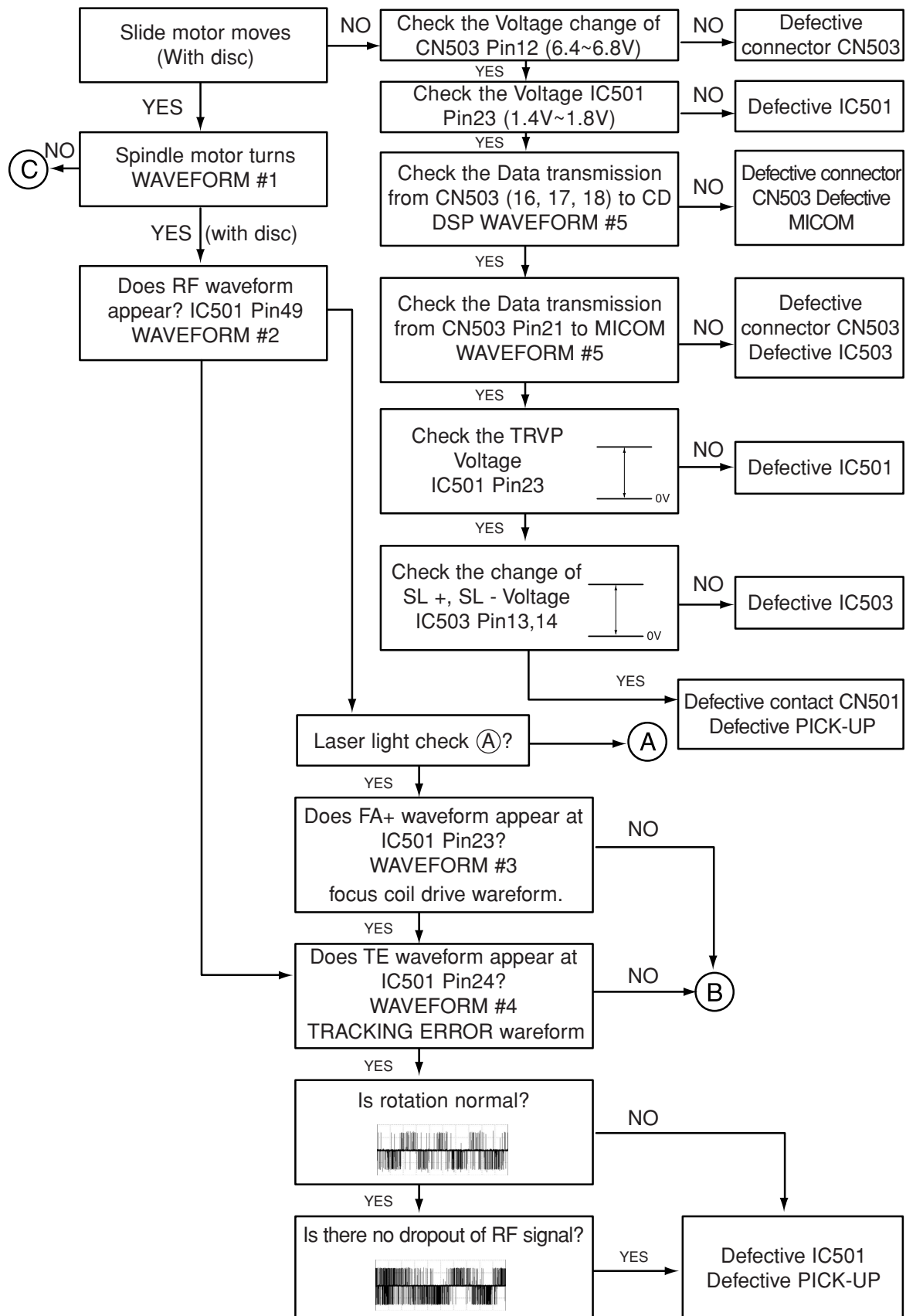
1. No Power.



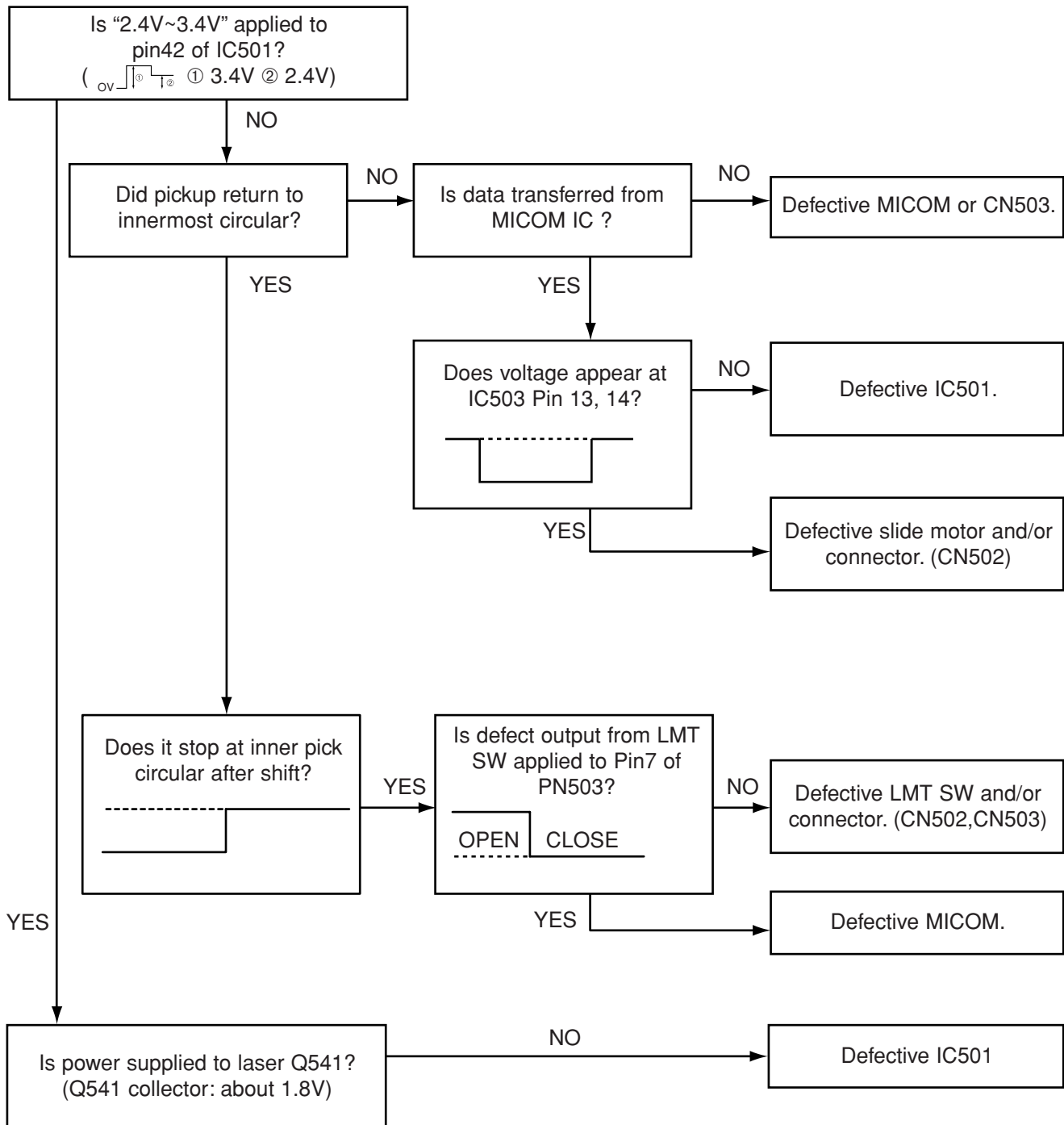
2. LCD light abnormal.



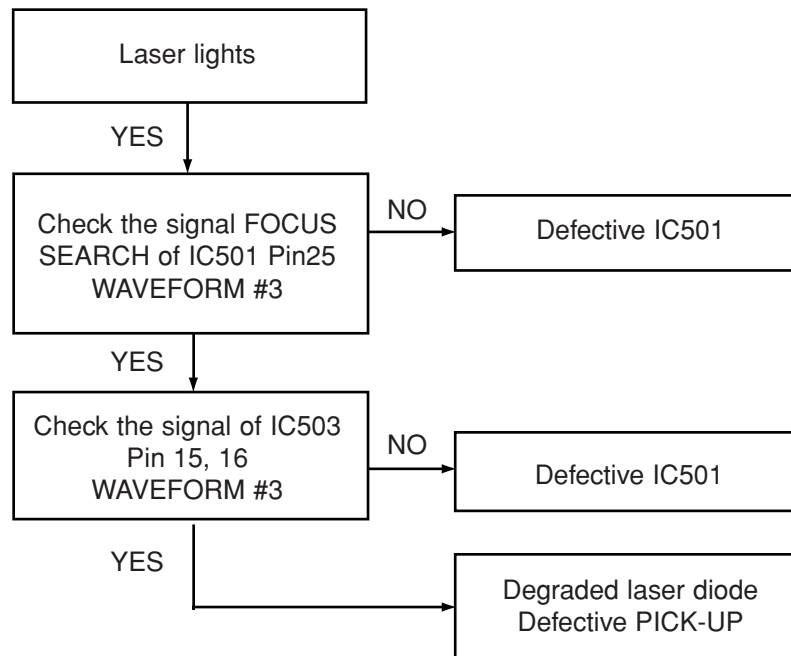
3. Initial reading is not carried out.



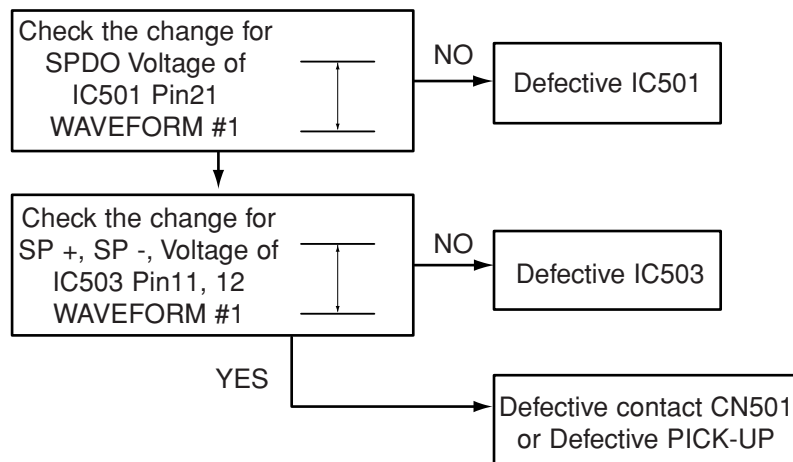
Ⓐ When laser does not light.



Ⓑ When laser light.

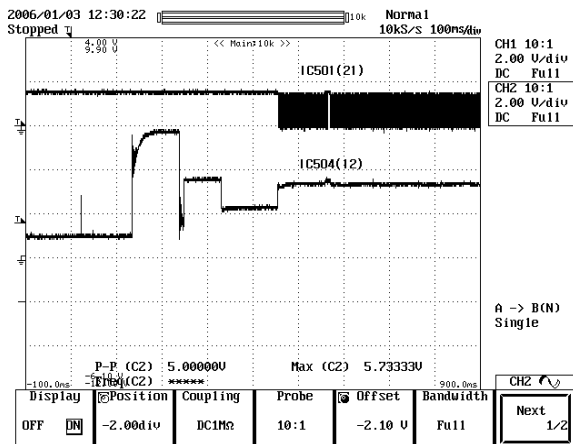


Ⓒ When SPINDLE motor dose not turn

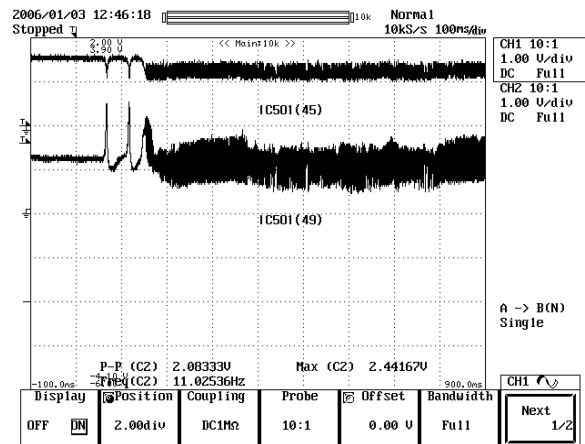


WAVEFORMS OF MAJOR CHECK POINT

#1. SPINDLE DRIVE AND MOTOR WAVEFORM IC501(21), IC504(12) during TOC reading

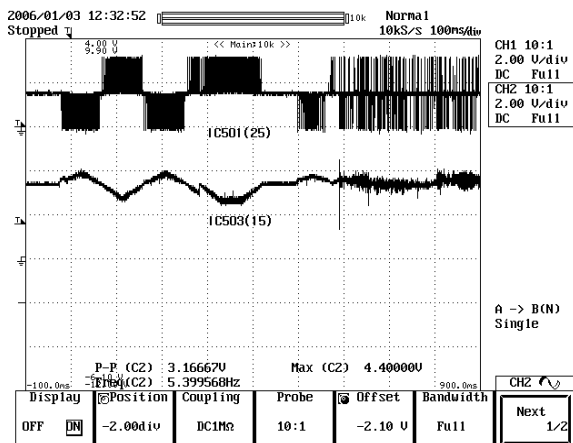


#2. RF WAVEFORM IC501(45), IC501(49) during TOC reading

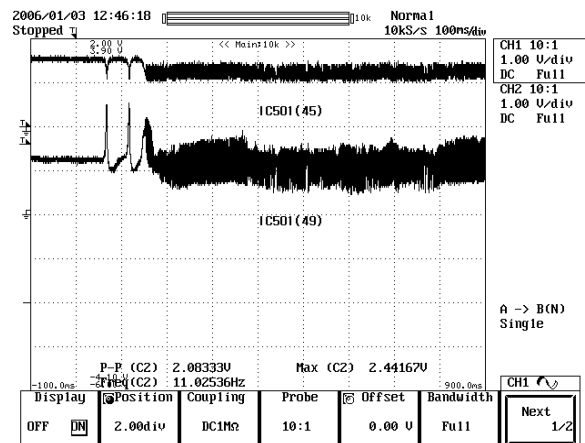


#3. FOCUS DRIVE AND MOTOR WAVEFORM IC501(25), IC503(15)

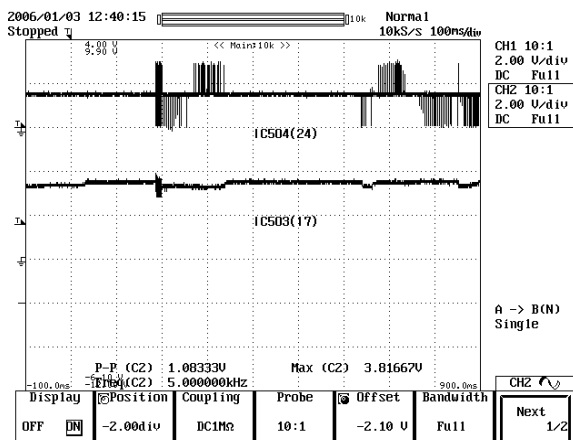
- When focus search failed or there is no disc on tray



- There is disc on tray and focus search success



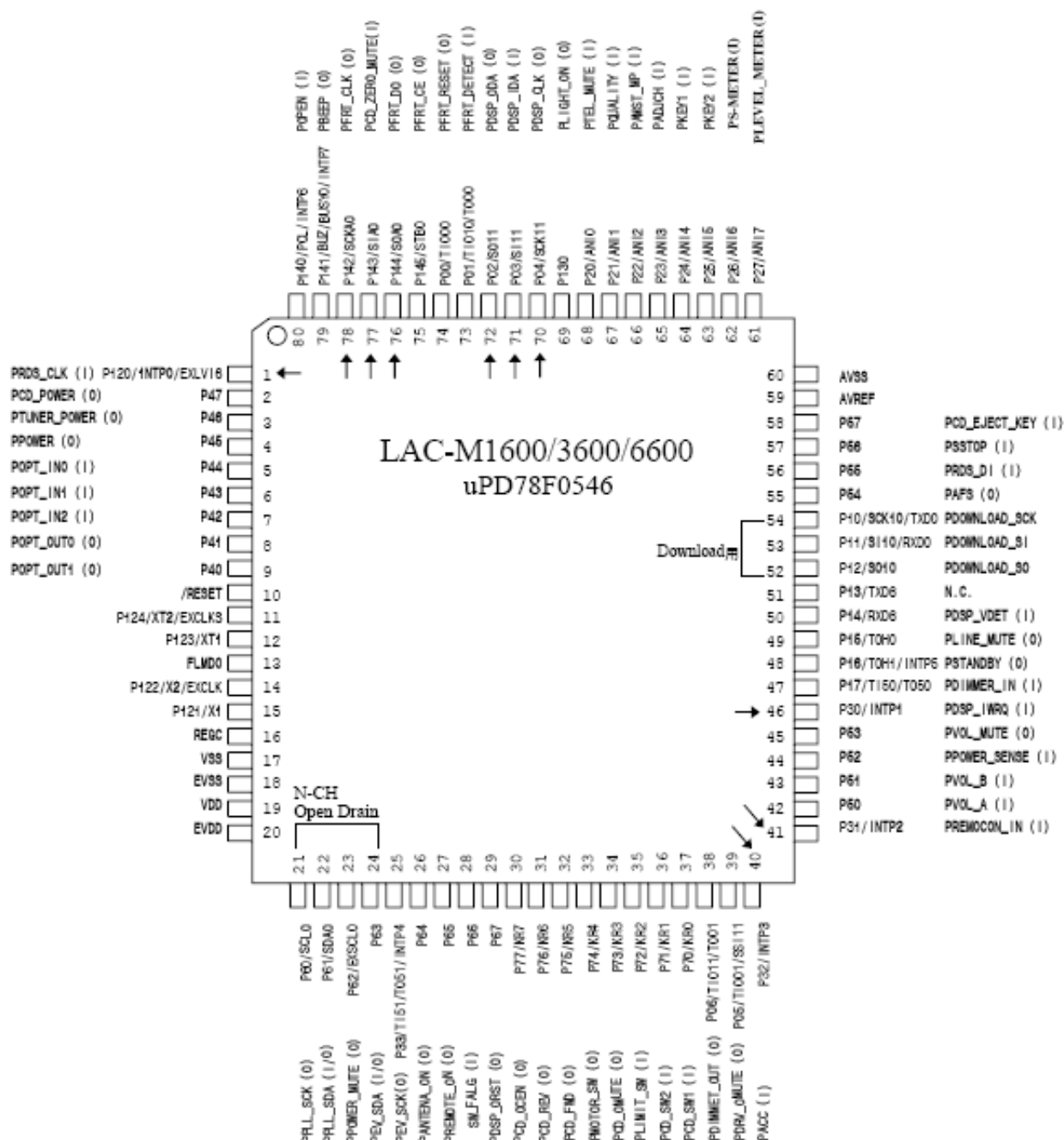
#4. TRACK DRIVE AND MOTOR WAVEFORM IC504(24), IC503(17) during TOC reading



INTERNAL BLOCK DIAGRAM of ICs

■ **AV CAR**

1) Micom Port Assignment



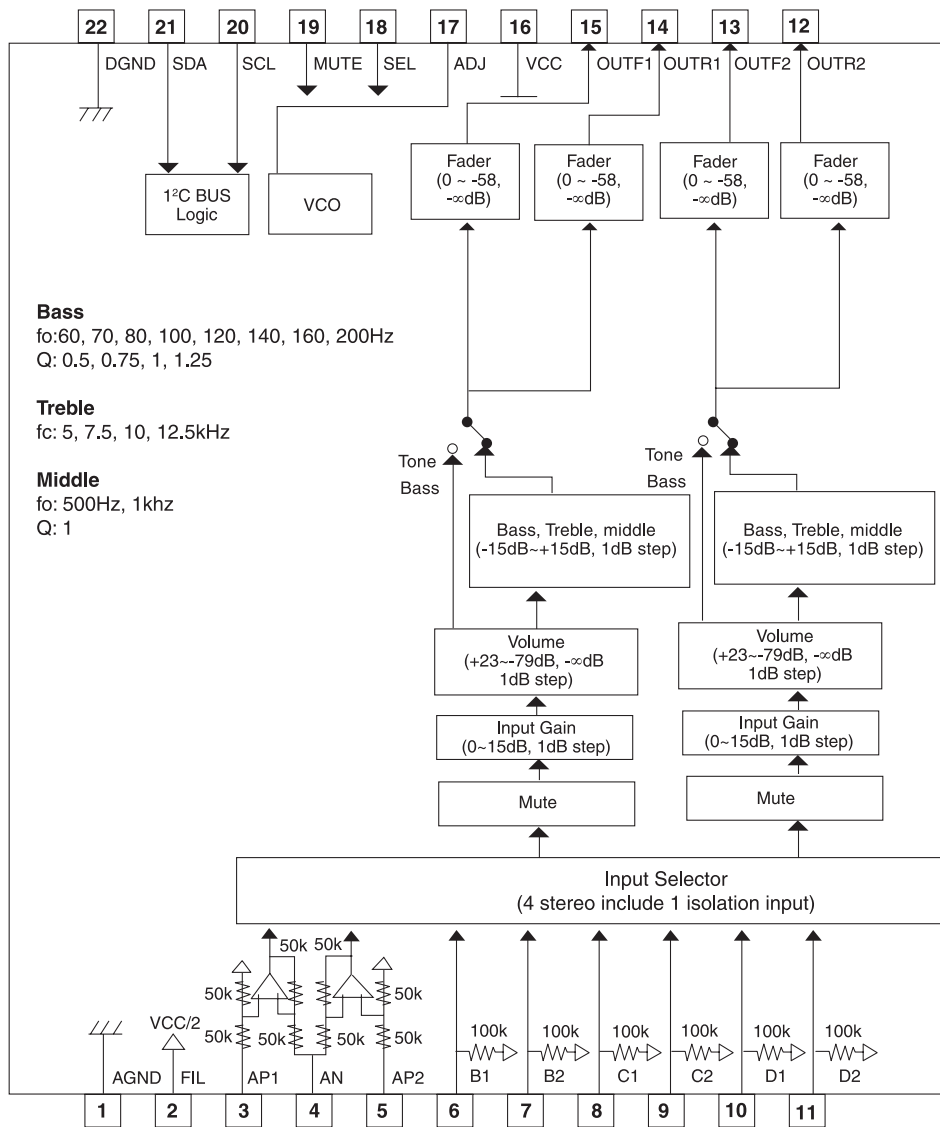
2) Pin Descriptions

Pin	Name in Micom	Name in Model	Enable I/O	I/O settet	Output Format	Description
1	P120/INTP0/EXLVI	PRDS_CLK	I/O	I	-	From tuner pack, RDS clock input
2	P47	PCD_PWR	I/O	O	CMOS	DSP power supplier ON ouptut
3	P46	PTUN_PWR	I/O	O	CMOS	Tuner power supplier ON output
4	P45	PPWR	I/O	O	CMOS	System Power supplier ON output
5	P44	POPT_IN0	I/O	I	-	For diode option check, signal 1 or 2 input0
6	P43	POPT_IN1	I/O	I	-	For diode option check, signal 1 or 2 input1
7	P42	POPT_IN2	I/O	I	-	For diode option check signal 1 or 2 input2
8	P41	POPT_OUT0	I/O	O	CMOS	For diode option check, signal 1 output
9	P40	POPT_OUT1	I/O	O	CMOS	For diode option check, signal 2 output
10	/RESET	RESET	-	-	-	System reset input
11	P124/XT2/EXCLKS	XT2	-	-	CMOS	Sub clock 32.768 KHz
12	P123/XT1	XT1	I	-	CMOS	Sub clock 32.768 KHz
13	FLMD0	FLMD0	-	-	-	Flash Memory Programming Mode Setting pull down (470 ? ~ 10k?)
14	P122/X2/EXCLK	X2	-	-	CMOS	X'tal 9.8304 MHz
15	P121/X1	X1	I	-	CMOS	X'tal 9.8304 MHz
16	REGC	REGC	-	-	-	Connect to VSS Via 0.47uF Capacitor
17	VSS	Vss	-	-	-	Ground
18	EVSS	EVss	-	-	-	Ground Potential for Ports
19	VDD	VDD	-	-	-	Positive power supply (+5V)
20	EVDD	EVDD	-	-	-	Positive power supply (+5V) For Ports
21	P60/SCL0	PPLL_SCLK	I/O	O	N-CH	Clock output for interface with PLL IC
22	P61/SDA0	PPLL_SDA	I/O	O	N-CH	PLL IC, data output/input
23	P62/EXSCL0	PPWR_MUTE	I/O	O	N-CH	To Power amp, "MUTE" command output
24	P63	PEV_DO	I/O	O	N-CH	To volume controller, data output
25	P33/TI51/TO51/INTP4	PEV_CLK	I/O	O	CMOS	Clock for interface with volume controller
26	P64	PANT	I/O	O	CMOS	Antenna control output
27	P65	PREMOTE	I/O	O	CMOS	External power amplifier enable output
28	P66	PSW_FALG	I/O	I	-	
29	P67	PDSP_ORST	I/O	O	CMOS	DSP reset output
30	P77/KR7	PCD_OCEN	I/O	O	CMOS	DSP chip enable output
31	P76/KR6	PCD_REV	I/O	O	CMOS	In MD, load motor "reverse" command output
32	P75/KR5	PCD_FWD	I/O	O	CMOS	In MD, load motor "forward" command output
33	P74/KR4	PMOTOR_SW	I/O	O	CMOS	In MD, switching load and sled motor
34	P73/KR3	PCD_MUTE	I/O	O	CMOS	CD audio mute output
35	P72/KR2	PLMT_ISW	I/O	I	-	In MD, limit switch state input
36	P71/KR1	PCD_SW2	I/O	I	-	In MD, SW2 state input
37	P70/KR0	PCD_SW1	I/O	I	-	In MD, SW1 state input
38	P06/TI011/TO01	PDIMMER_OUT	I/O	O	CMOS	Dimmer control output
39	P05/TI001/SSI11	PDRV_OMUTE	I/O	O	CMOS	In MD, all motor's output "cut off" command ouput
40	P32/INTP3	PACC	I/O	I	-	Remote Controller's signal input(interrupt3)
41	P31/INTP2	PREMOCON_IN	I/O	I	-	From CD changer data input
42	P50	PVOLA	I/O	I	-	Encoder volume terminal #A input
43	P51	PVOLB	I/O	I	-	Encoder volume terminal #B input
44	P52	N.C.	I/O	I	-	
45	P53	PVOL_MUTE	I/O	O	CMOS	Direct volume mute signal output
46	P30/INT1	PDSP_IWRQ	I/O	I	-	Sub-Q read standard level signal input
47	P17/TI50/TO50	PDIM_IN	I/O	I	-	
48	P16/TOH1/INTP5	PSTANDBY	I/O	O	CMOS	To PowerR amp, "STAND-BY" command output
49	P15/TOH0	PLINE_MUTE	I/O	O	CMOS	LINE MUTE ON/OFF
50	P14/RxD6	PCD_VDET	I/O	I	-	CD DSP Tracking Error Detect Port
51	P13/TxD6	PTUNER_MUTE	I/O	I	-	Tuner Mute Port
52	P12/SO10	DOWNLOAD_SO	I/O	O	CMOS	For Download Data output
53	P11/SI10/RxD0	DOWNLOAD_SI	I/O	I	-	For Download Data input
54	P10/SCK10/TxD0	DOWNLOAD_SCK	I/O	O	CMOS	For Download Clock output
55	P54	PAFS	I/O	O	CMOS	Connect to Tuner Pack AFS Port For AF Mute
56	P55	PRDS_DI	I/O	I	-	From tuner pack, RDS data input
57	P56	PSSTOP	I/O	I	-	Connect to Tuner Pack SSTOP For Stop Detect
58	P57	PCD_EJT	I/O	I	-	Eject key input
59	AV REF	AV REF	-	-	-	Reference voltage applied to D/A converter
60	AVss	AVss	-	-	-	Ground for A/D converter and D/A converter Connect to Vss
61	P27/ANI7	PLVL_MTR	I/O	I	-	Sound level s signal input
62	P26/ANI6	PS_MTR	I/O	I	-	Radio station's strength signal input
63	P25/ANI5	PKEY2	I/O	I	-	Key #2 line input

Pin	Name in Micom	Name in Model	Enable I/O	I/O settled	Output Format	Description
64	P24/ANI4	PKEY1	I/O	I	-	Key #1 line input
65	P23/ANI3	PADJCH	I/O	I	-	Connect to tuner pack ADJCH for adjacent Ch. Level
66	P22/ANI2	PAMST_MP	I/O	I	-	Connect to tuner pack AMST_MP for Multi-path Ch.
67	P21/ANI1	PQUALITY	I/O	I	-	Connect to tuner pack QUALITY
68	P20/ANI0	PTL_MUTE	I/O	I	-	Telephone mute input
69	P130	PLIGHT	O	O	CMOS	
70	P04/SCK11	PDSP_OCLK	I/O	O	CMOS	Clock output for interface with DSP
71	P03/SH11	PDSP_IDA	I/O	I	-	From DSP, data input
72	P02/SO11	PDSP_ODA	I/O	O	CMOS	To DSP, data output
73	P01/TI010/TO00	PFRT_DET	I/O	I	-	Front pannel existence signal input
74	P00/TI000	PFRT_RES	I/O	O	CMOS	LCD driver reset output
75	P145/STB0	PFRT_CE	I/O	O	CMOS	LCD driver enable output
76	P144/SOA0	PFRT_DO	I/O	O	CMOS	To LCD driver, data output
77	P143/SIA0	N.C.	I/O	O	CMOS	Not to be used (Open)
78	P142/SCKA0	PFRT_CLK	I/O	O	CMOS	Clock output for interface with LCD driver
79	P141/BUZBUSY0/INTP7	PBEEP	I/O	O	CMOS	Beep sound output (2 KHz)
80	P140/PCL/INTP6	POPEN	I/O	I	-	Front open/close detect

BD3805F

1) BLOCK DIAGRAM



■ MN6627933CN(DSP)

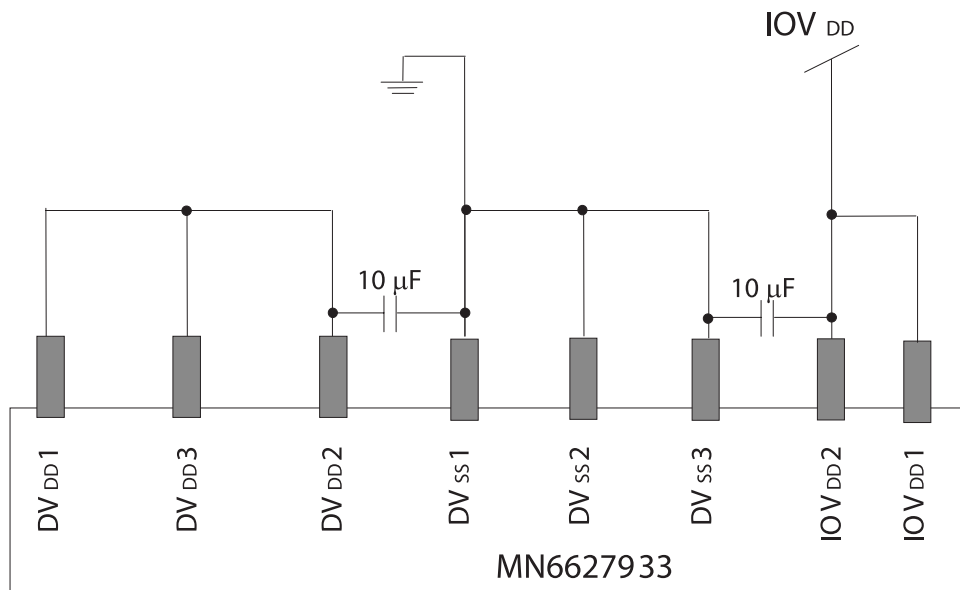
1) Connection Diagram

MN6627933

Power Supply Connection Diagram



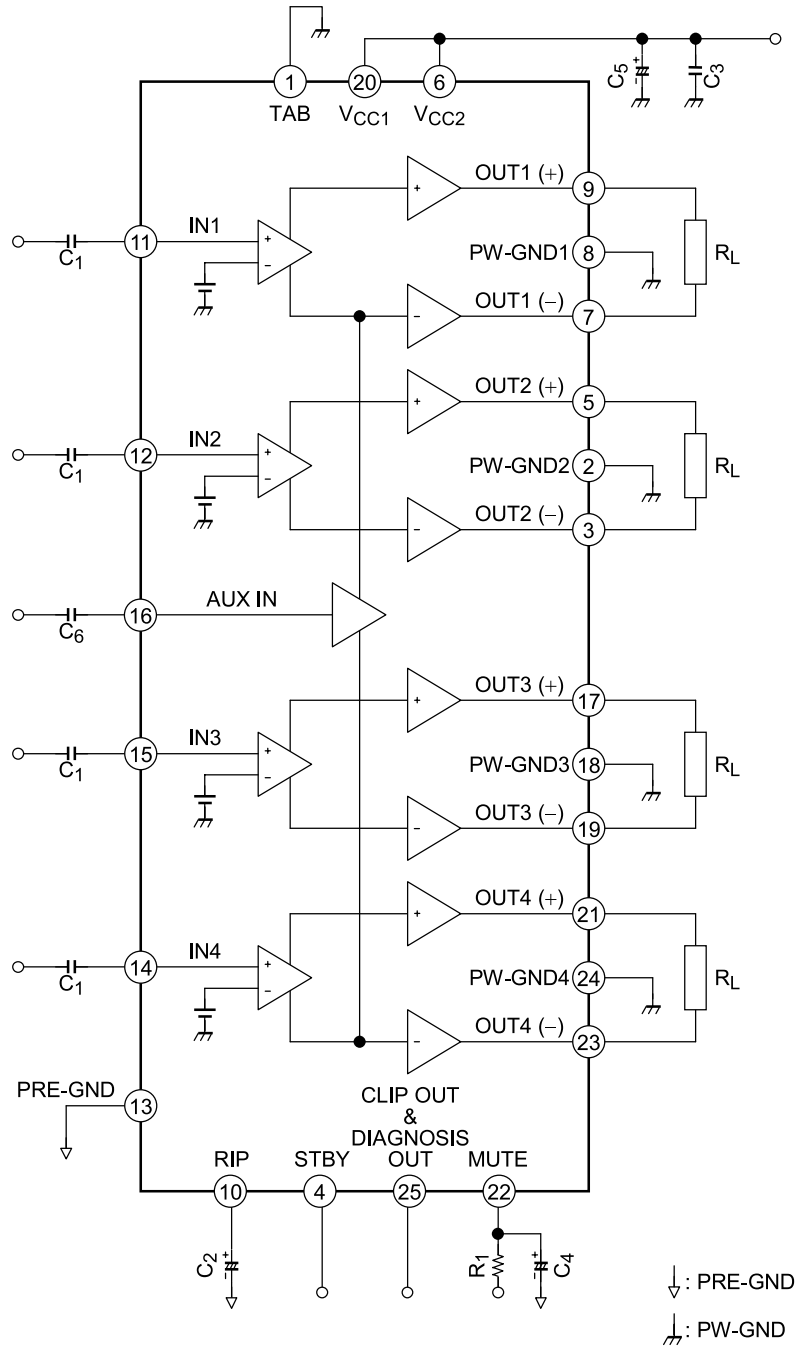
Power supply pin



The connections for AVDD and LOVDD are not shown.

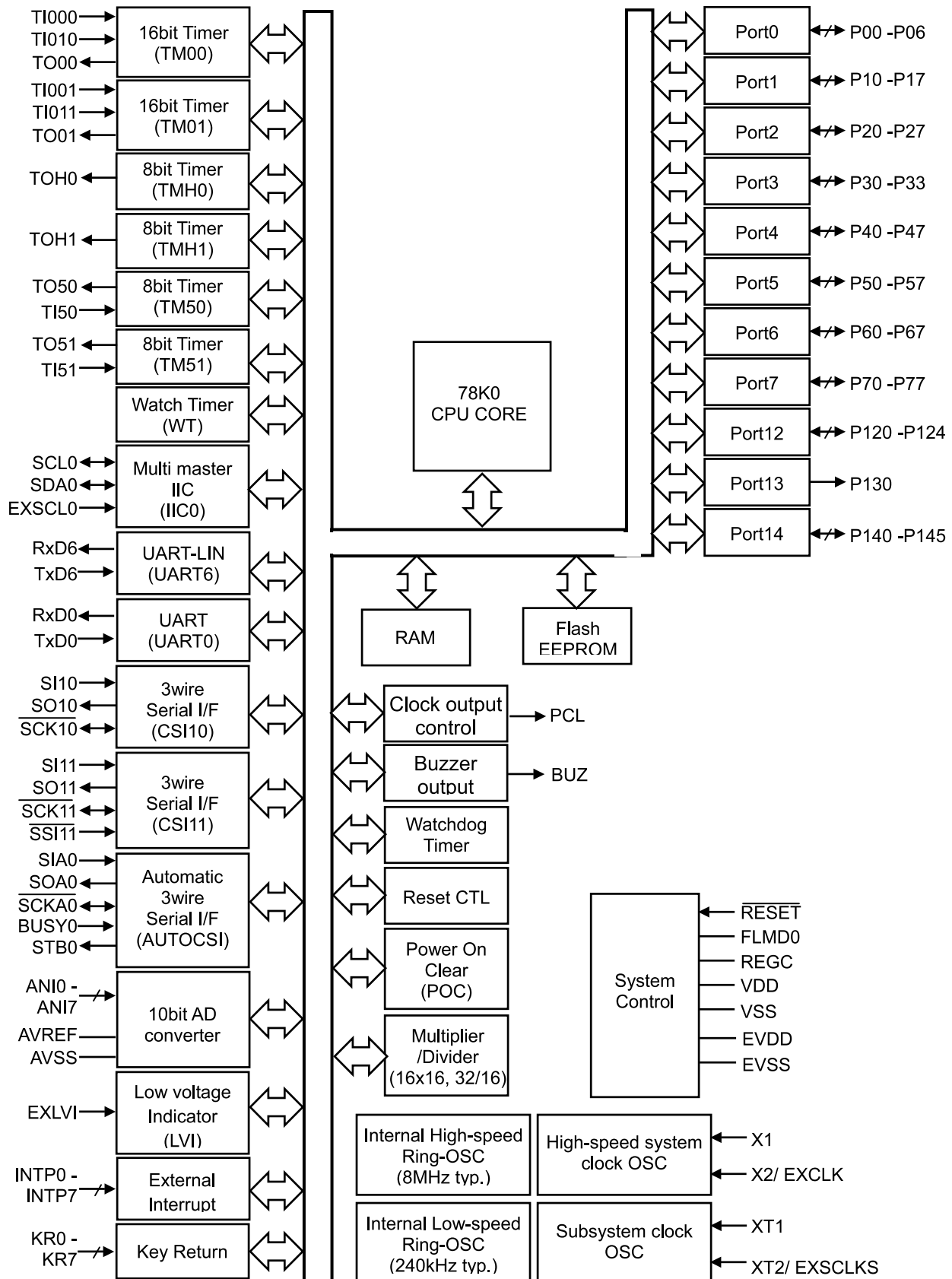
■ TA8275HQ

1) Block Diagram

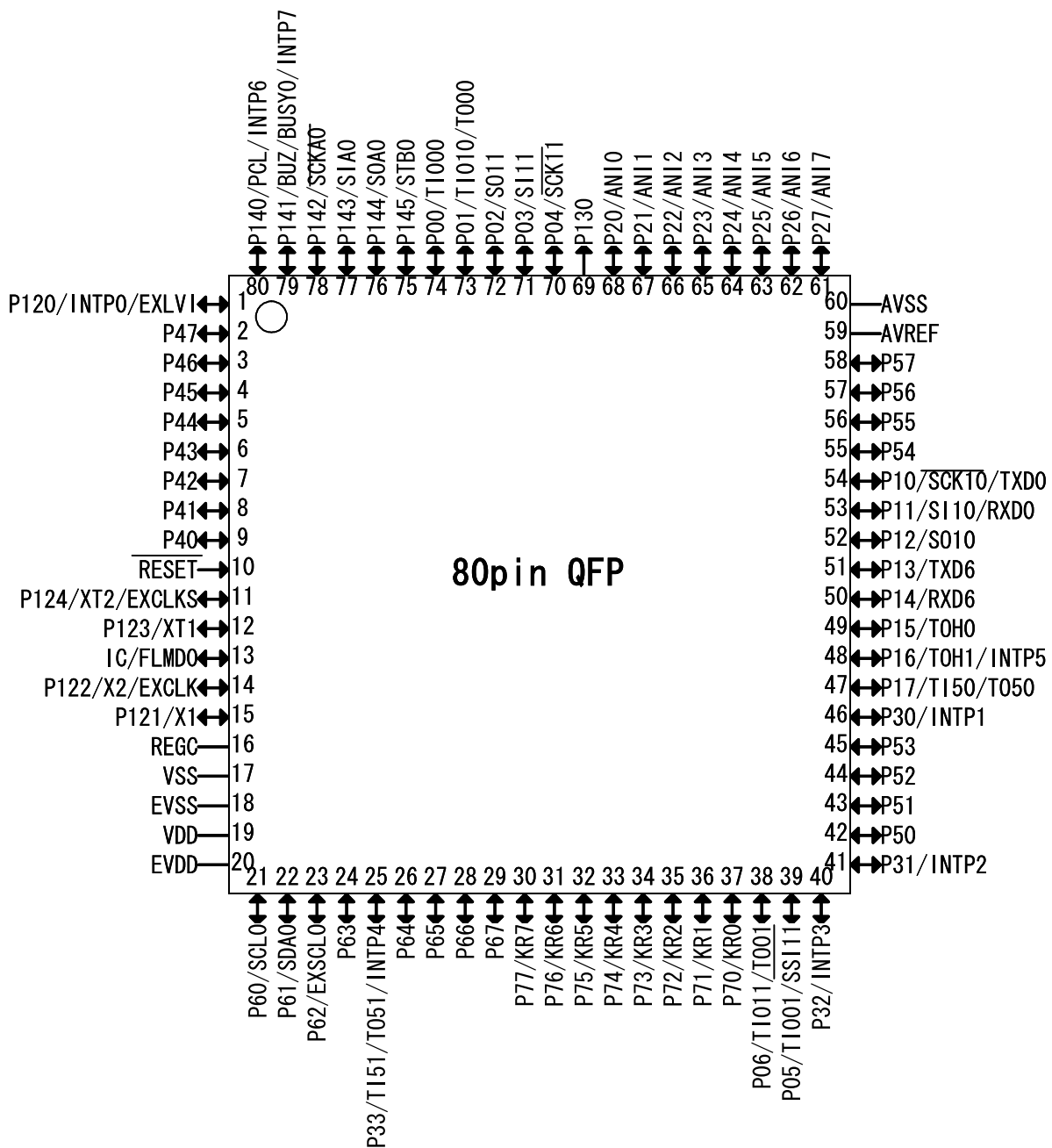


■ upd78f0546(Micom)

1) Block Diagram



2) Pin lay out



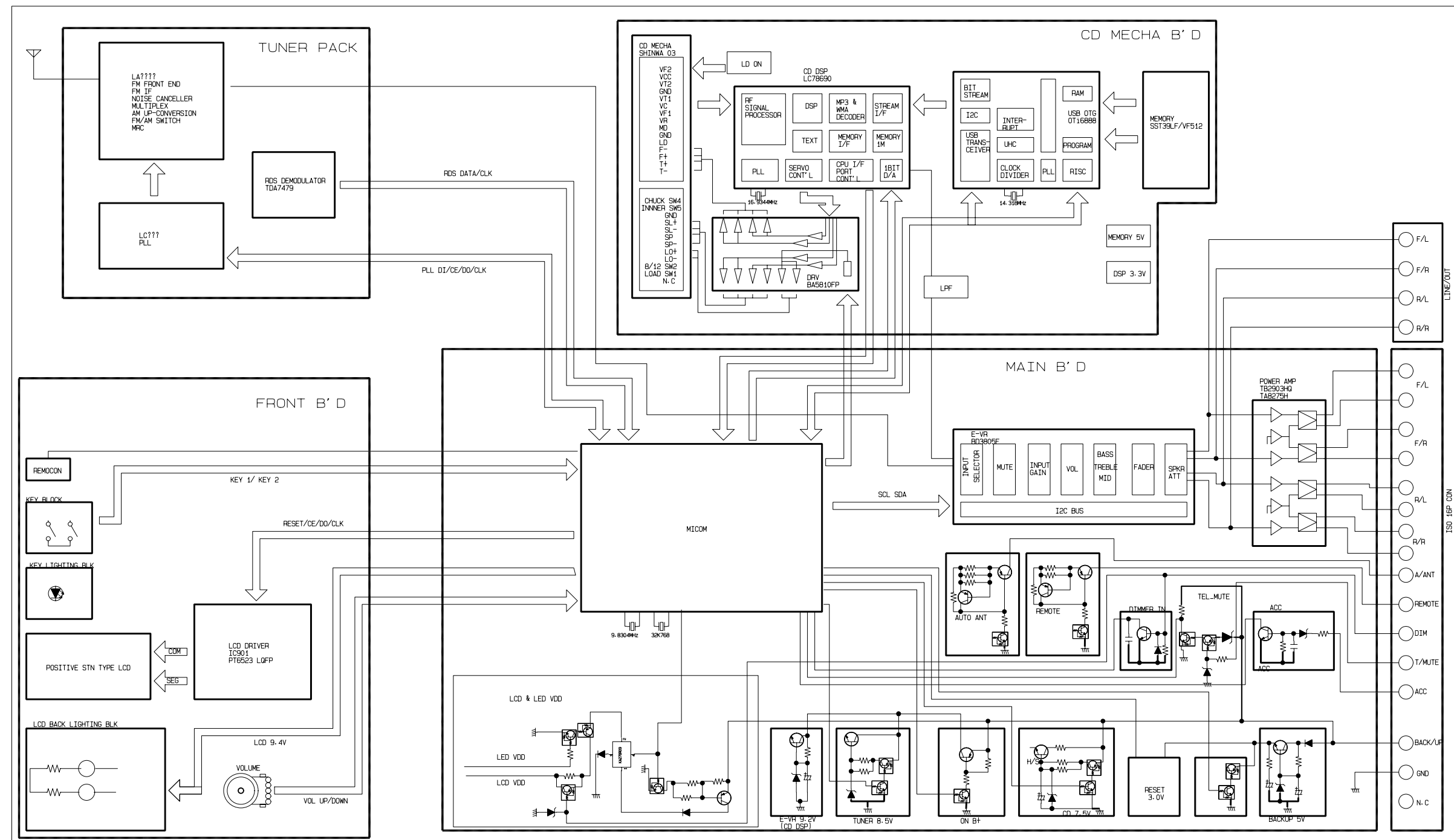
3) Pin Function

PIN NAME	Function
VDD	Positive power supply except for ports (except P20-P27 and P121-P124) and AD converter
VSS	Ground potential except for ports (except P20-P27 and P121-P124) and AD converter
EVDD	Positive power supply for ports (expect p20-p27 and p121-p124)
EVSS	Ground potential for ports (except p20-p27 and p121-p124)
RESET	System reset input
FLMDO	Flash EEPROM programming mode setting
REGC	Connecting regulator stabilization capacitor. Connect to GND via a capacitor (0.47μF).
AVREF	A/D converter analog power supply and power supply for p20-p27
AVSS	Ground potential for A/D convert and p20-p27
P00/T1000	I/O port External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00(TM00)
P01/TI010/TO00	I/O port Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00 (TM00) 16-bit timer/event counter 00 outout (TM00)
P02/SO11	I/O port Serial data output from serial interface (CSI11)
PO3/SI11	I/O port Serial data input to serial interface (CSI11)
P20/SCK11	I/O port Clock input/output for serial interface (CSI11)
P05/TI001/SSI11	I/O port External count clock input to 18-bit timer/event counter 01 Capture trigger input to capture registers (CR001, CR011) of 16-bit timer/event counter 01(TM01) Chip input/output for serial interface (CSI11)
P06/TI011/TO01	I/O port Capture trigger input to capture register (CR001) of 160bit timer/evrnt counter 01 (TM01) 16-bit timer/evrnt counter 01 output (TM01)
P10/SCK10/TXD0	I/O port Clock input/output for serial interface (CSI10) Serial data output from asynchronous serial interface (UART0)
P11/SI10/RXD0	I/O port Serial data input to serial interface (CSI10) Serial data input to asynchronous serial interface (UART0)
P12/SO10	I/O port Serial data input to serial interface (CSI10)
P13/TXD6	I/O port Serial data output from asynchronous serial interface (UART6)
P14.RXD6	I/O port Serial data input to asynchronous serial interface (UART6)
P15/TOH0	I/O port 8-bit timer H0 output (TMH0)
P16/TOH1/NTP5	I/O port 8-bit timer H1 output (TMH1) External interrupt request input with specifiable valia edges
P17/TI50/TO50	I/O port External count clock input to 8-bit timer/event counter 50 (TM50) 8-bit timer/event counter 50 output (TM50)
P20-P27/ANI0-ANI7	I/O ports A/D converter analog input
P30/INTP1	I/O port
P31/INTP2	External interrupt request input with specifiable vaild edges
P31/INTP2	
P33	I/O port
/TI51	External count clock input to 8-bit time/event counter 51 (TM51)
/TO51	8-bit timer/event counter 51 output (TM51)
/INTP4	External interrupt request input with specifiable valid edges
P40-P47	I/O port
P50-P57	I/O port
P60/SCL0	I/O port (N-ch open drain) Clock input/output for serial interface (IIC0)
P61/SDA0	I/O port (N-ch open drain) Serial data input/output for serial interface (IIC0)

PIN NAME	Function
P62/EXSCL0	I/O port (N-ch open drain)
	External clock input for serial interface (IIC0)
P63	I/O port (N-ch open drain)
P64-P67	I/O ports
P70-P77	I/O ports
/KR0-KR7	Key interrupt input
P120	I/O port
/INTP0	External interrupt request input with specifiable vaild edges
/EXLVI	Reference voltsge input for low voltage indicator
P121	I/O port (An external oscillation circuit is not used)
/X1	Connecting resonator for main system clock oscillation
P122	I/O port (An external oscillation circuit is not used)
/X2	Connecting resonator for main system clock oscillation
/EXCLK	External clock input for main system clock
P123	I/O port (An external oscillation circuit is not used)
XT1	connecting resonator for subsystem clock oscillation
P123	I/O port (An external oscillation circuit is not used)
XT1	Connecting resonator for subsystem clock oscillation
P124	I/O port (An external oscillation circuit is not used)
/XT2	Connecting resonator for subsystem clock oscillation
/EXCLKS	External clock input for subsystem clock
P130	Output port
P140	I/O port
/PCL	Clock output
/INTP6	External interrupt request input with specifiable vaild edge
P141	I/O port
/PCL	Clock output
/INTP7	External interrupt requwst input with specifiable vaild edge
/BUSY0	Busy signal input for serial interface (AUTOCSI)
P142	I/O port
/SCKA0	Clock input/output for serial interface (AUTOCSI)
P143	I/O port
/SIA0	Serial data input to serial interface
P144	I/O port
/SOA0	Serial data output from serial interface (AUTOCSI)
P145	I/O port
/STB0	Strobe signal input to serial interface (AUTOCSI)

❑ BLOCK DIAGRAM

LAC-M3600 BLOCK DIAGRAM



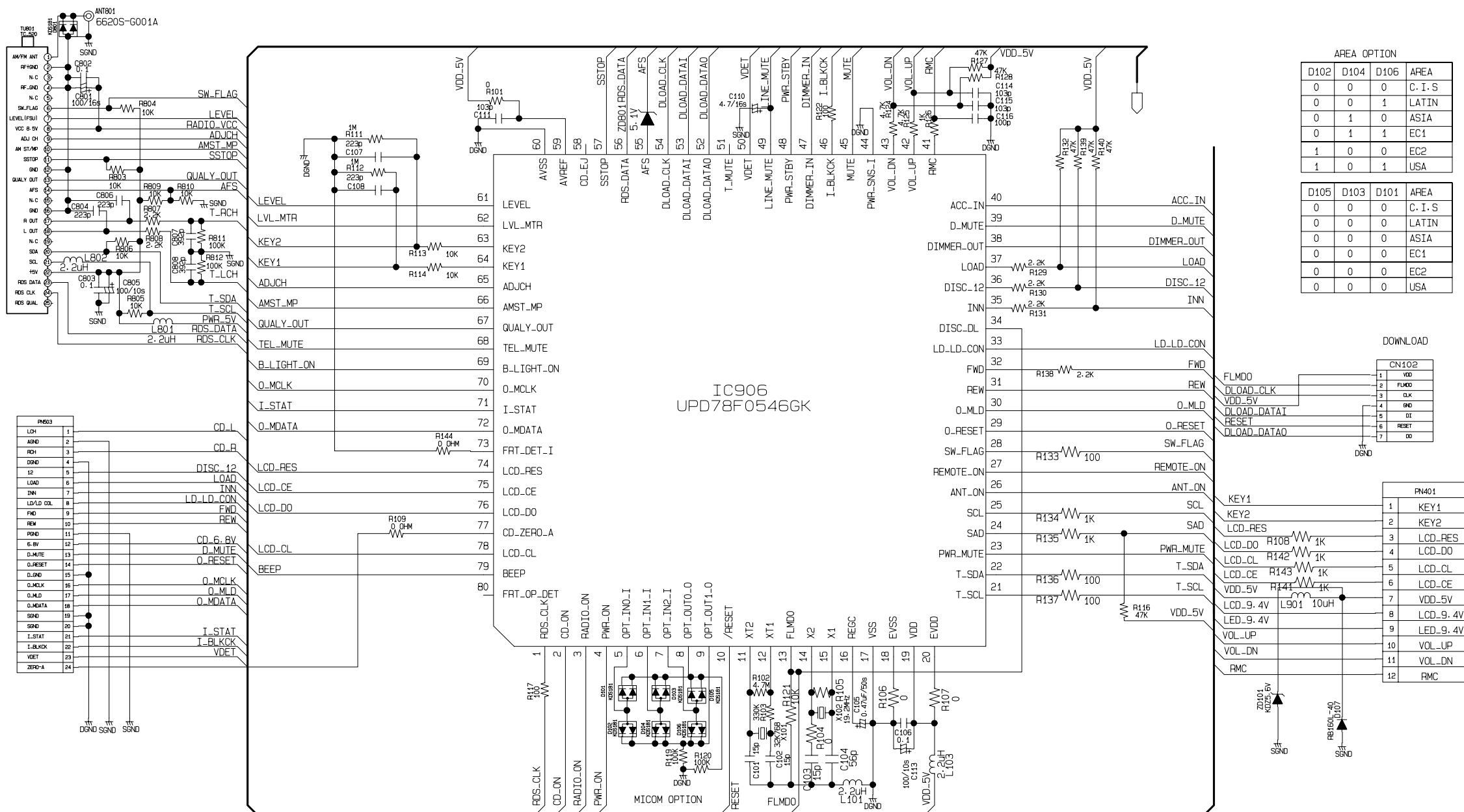
LAC-M3600 BLOCK DIAGRAM

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SD0502512

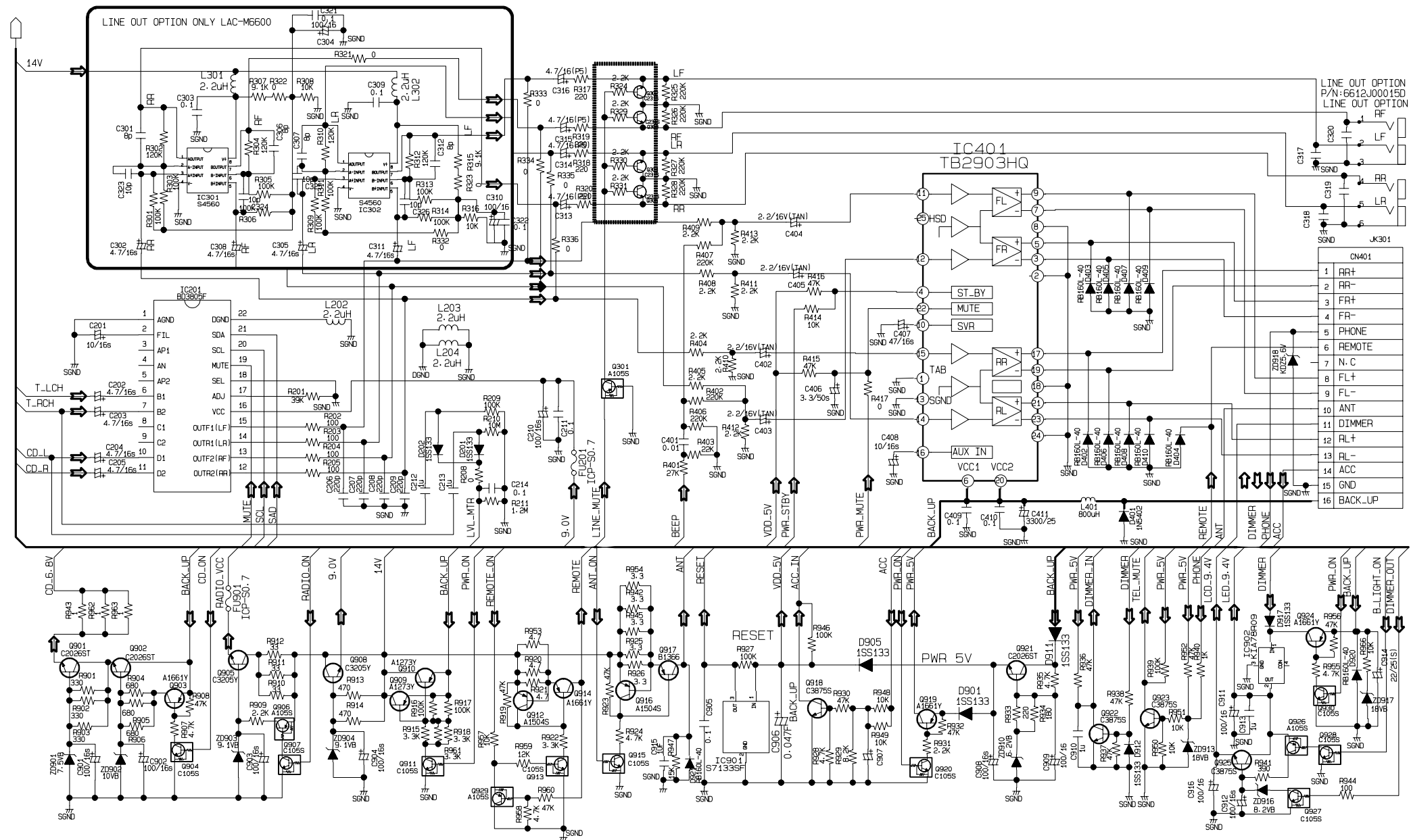
SCHEMATIC DIAGRAMS

MAIN SCHEMATIC DIAGRAM



LAC-M1600, 3600MAINPART
2006 . 1. 2. E/S 2ND
3854R13620A

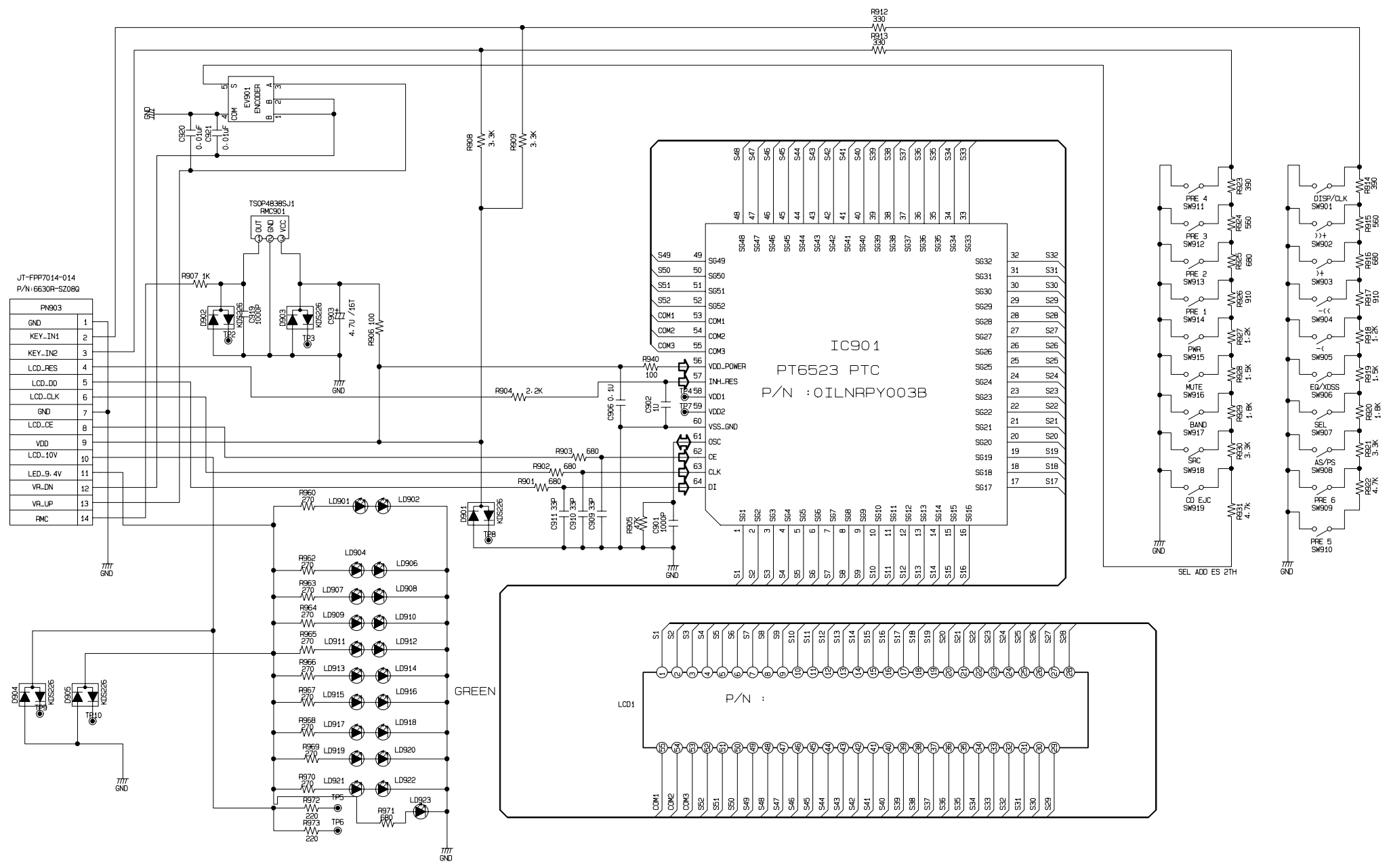
- **MAIN-2 SCHEMATIC DIAGRAM**



LAC-M1600, 3600 MAIN
2006. 01. 02

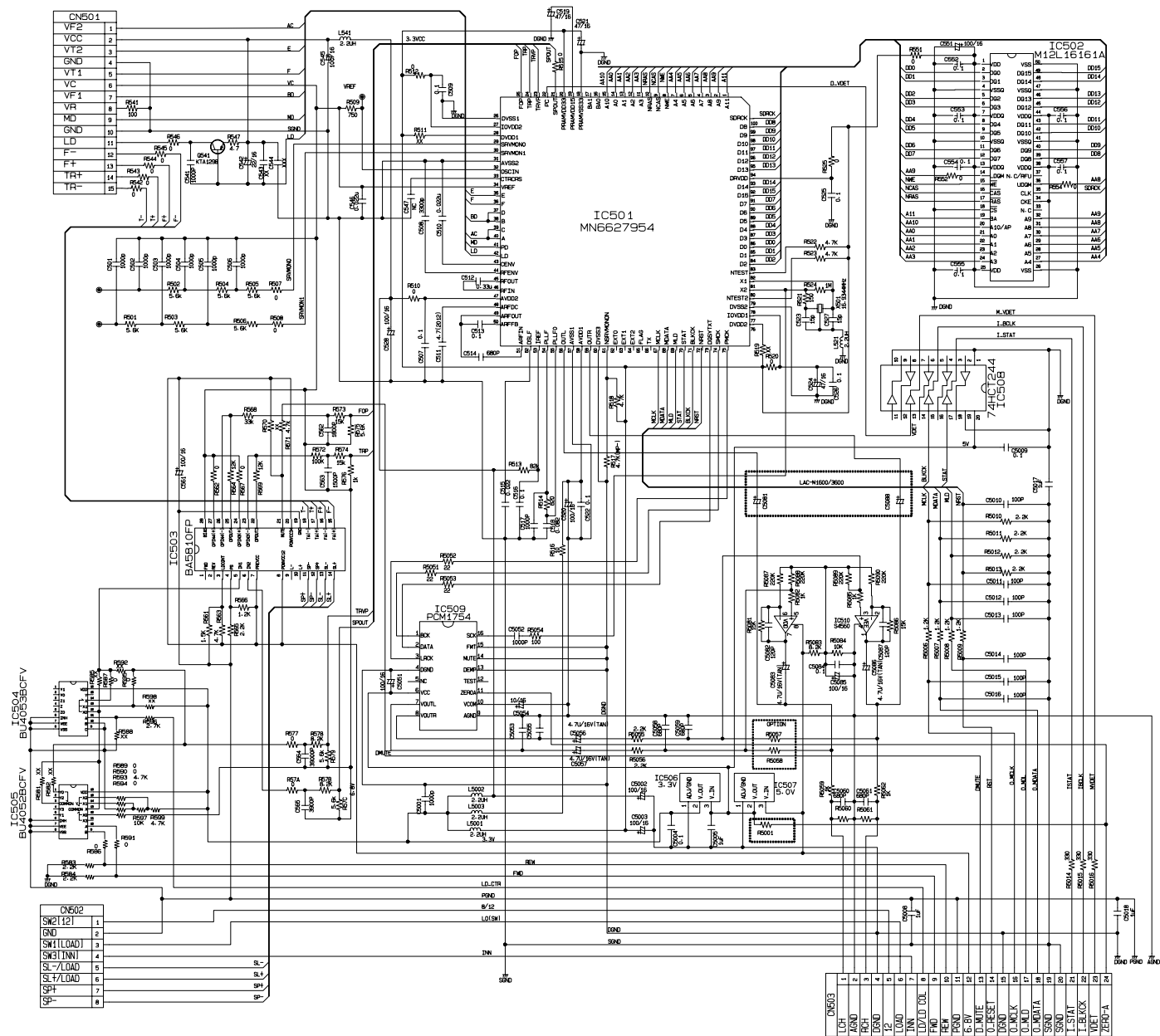
3854R13620A

• FRONT SCHEMATIC DIAGRAM



LAC-M3600 FRONT
2005. 09. 27
3854R13621A

• CD SCHEMATIC DIAGRAM

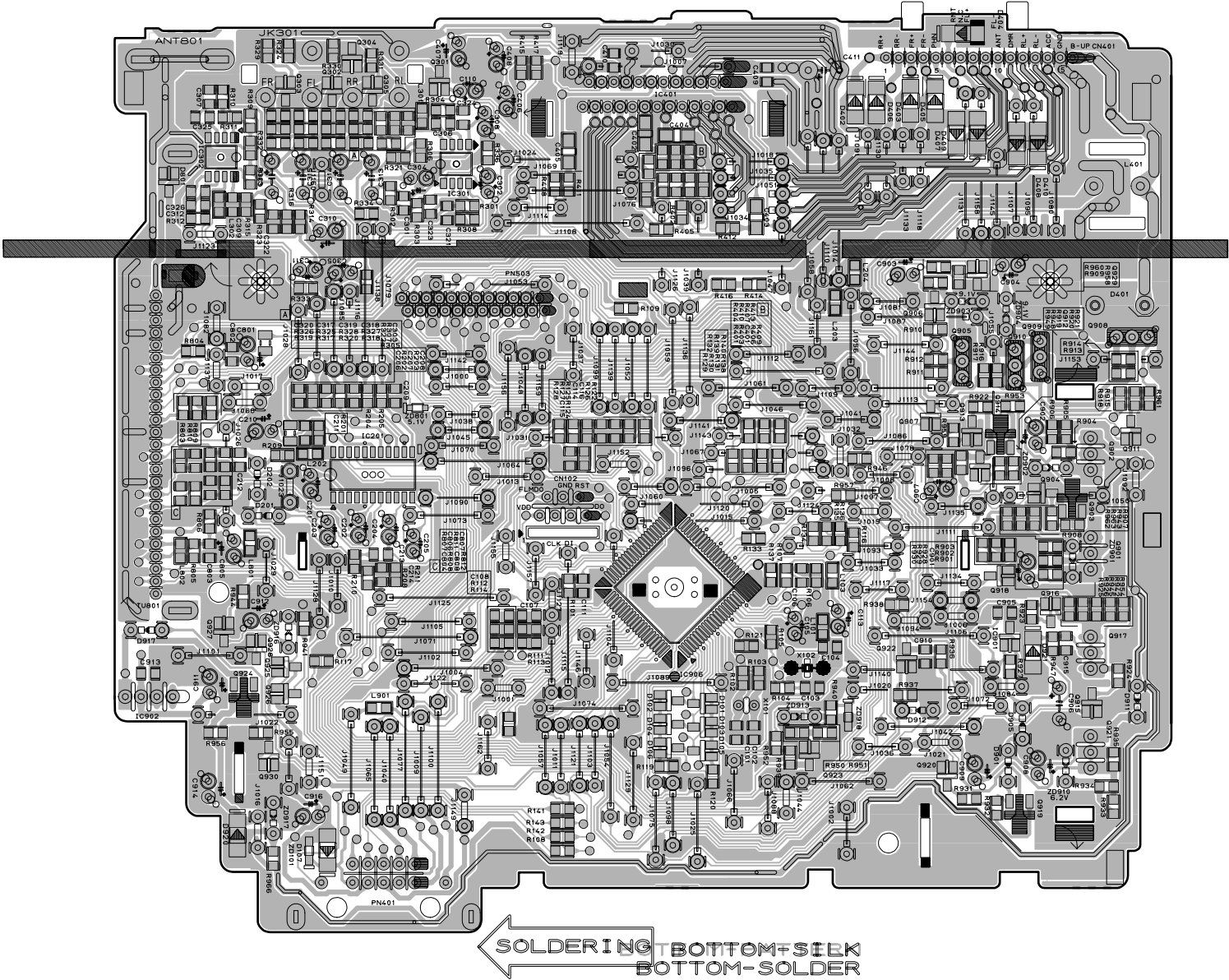


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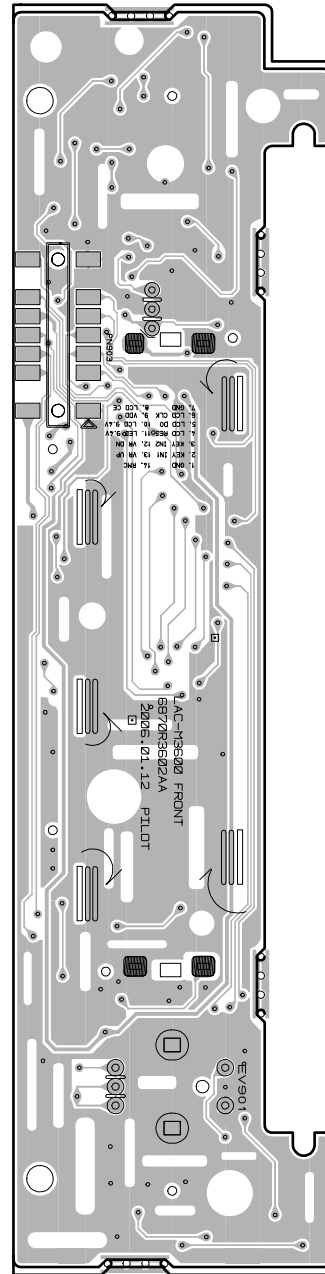
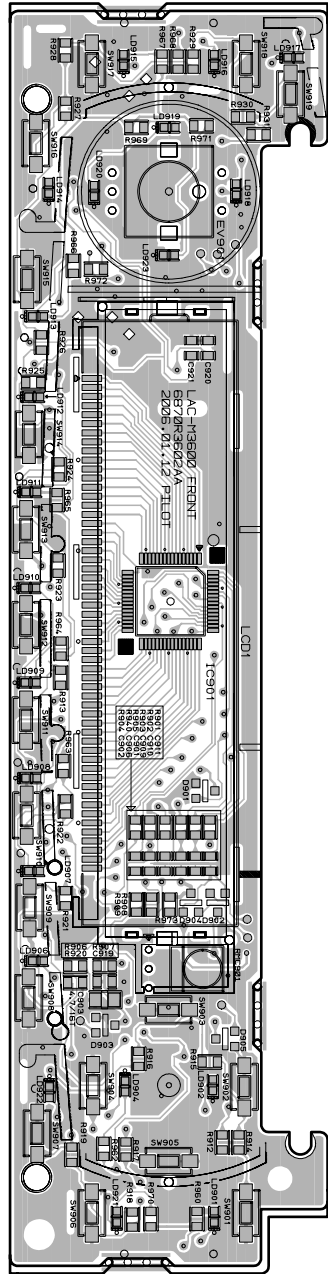
LAC-M6600
2006 01 24 CD PART
3854R19695A

❑ PRINTED CIRCUIT BOARD DIAGRAMS

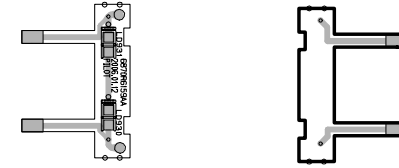
- MAIN P.C. BOARD DIAGRAM



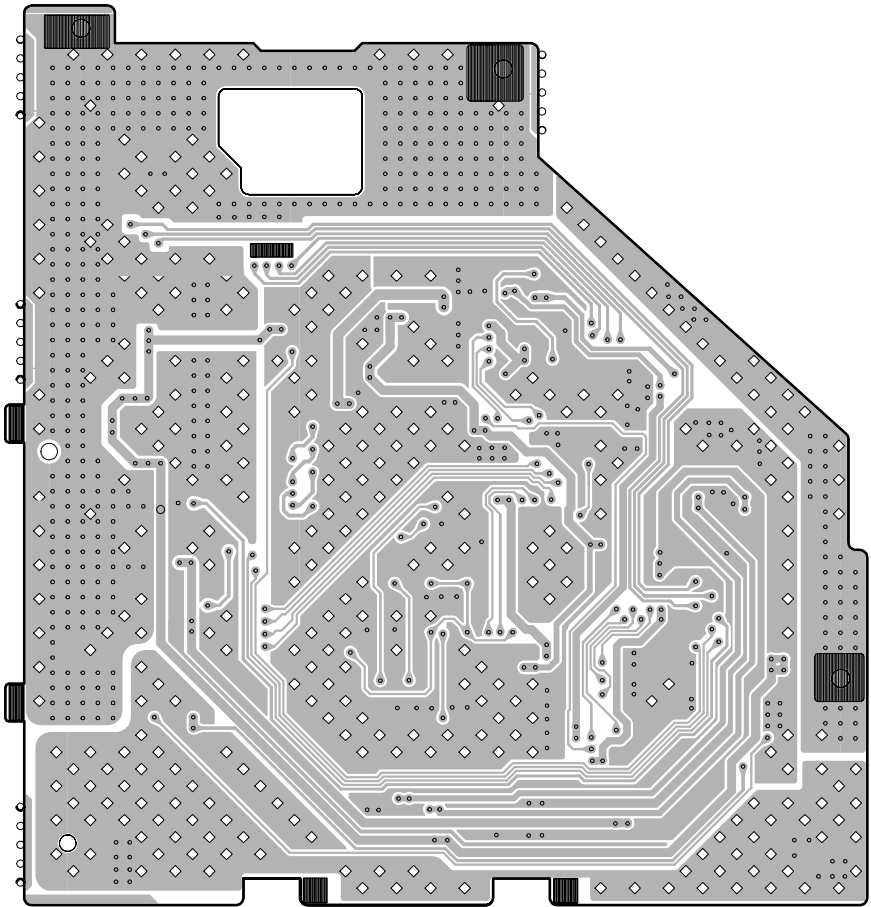
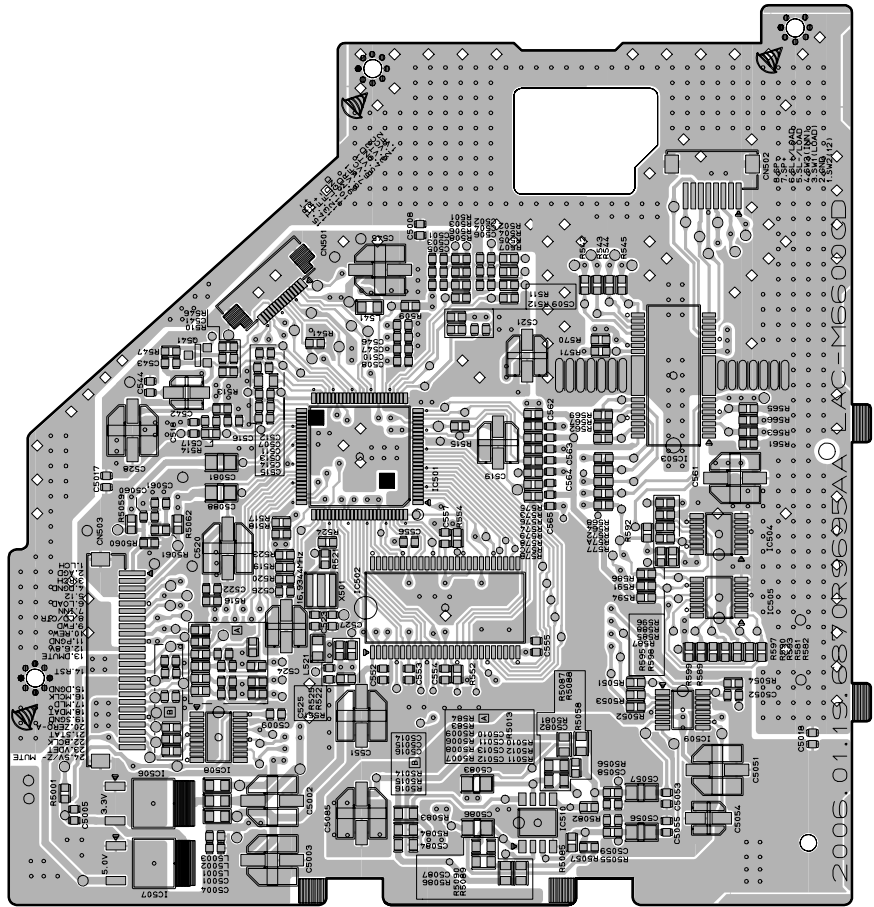
• **FRONT/TRIM P.C. BOARD DIAGRAM**



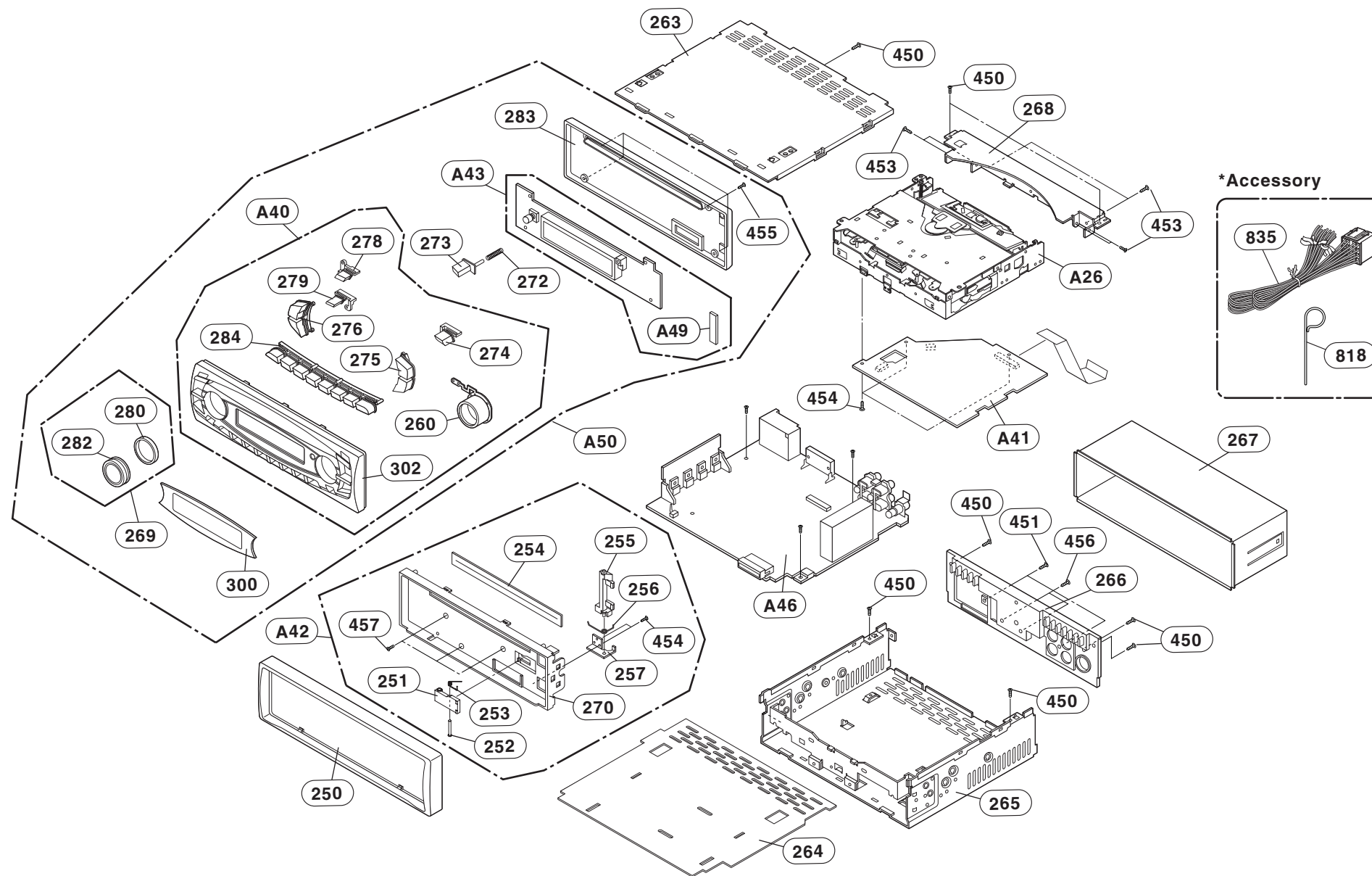
- **LED P.C. BOARD**



• CD P.C. BOARD



CABINET AND MAIN FRAME SECTION



MECHANISM (PICK-UP)

