

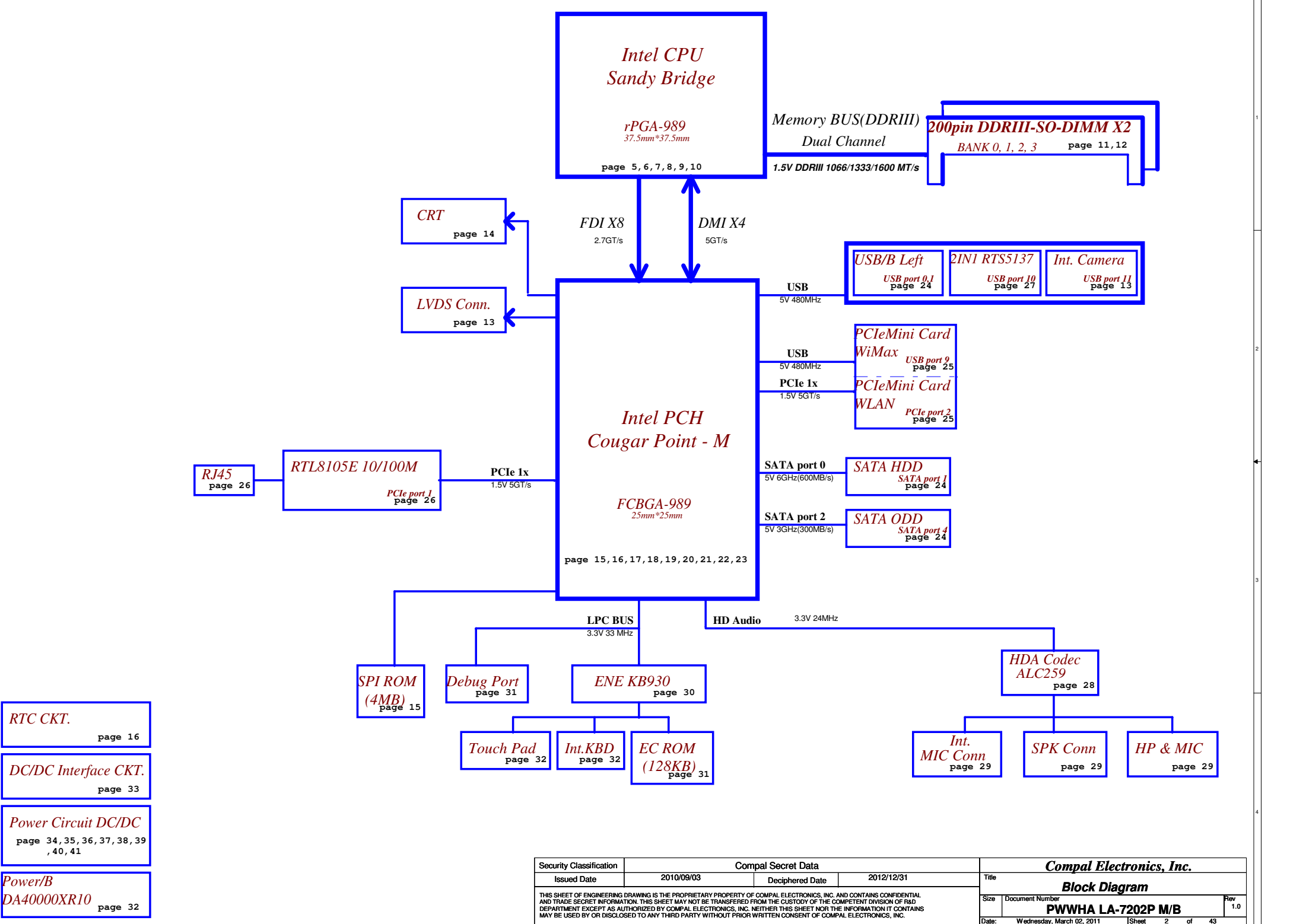
PWWHA

Delhi 10R

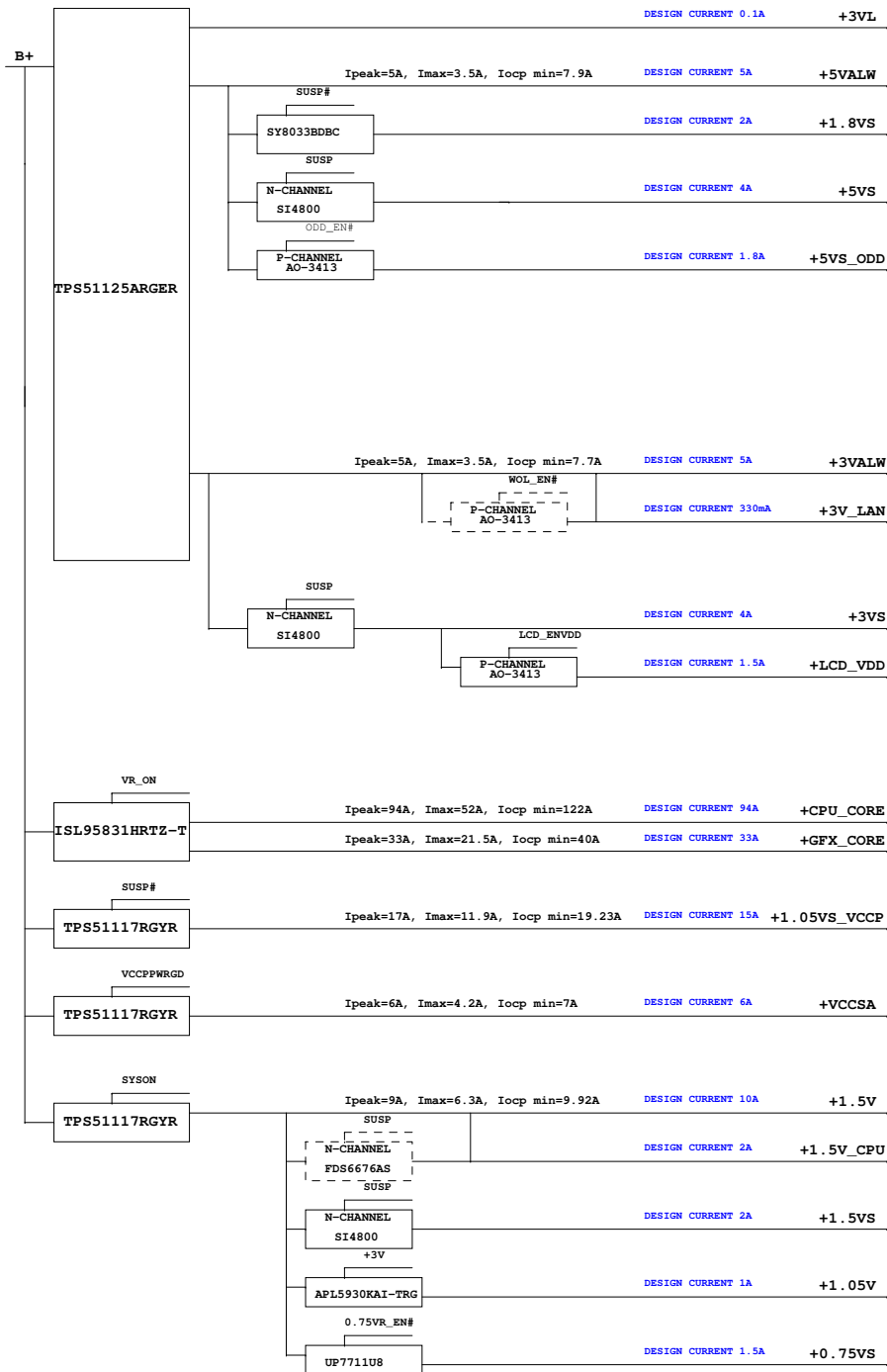
LA-7202P REV 1.0 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2011-02-08 Rev 1.0

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

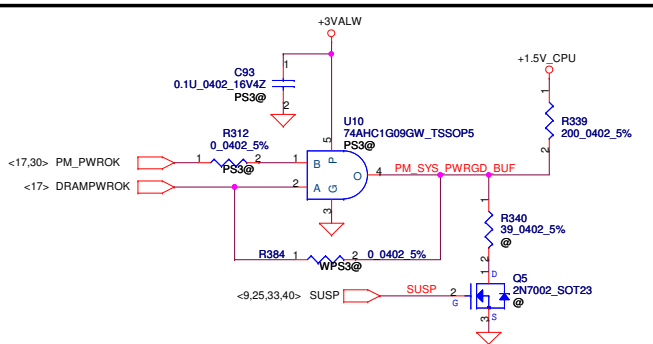
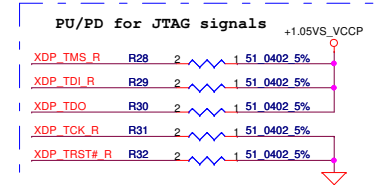
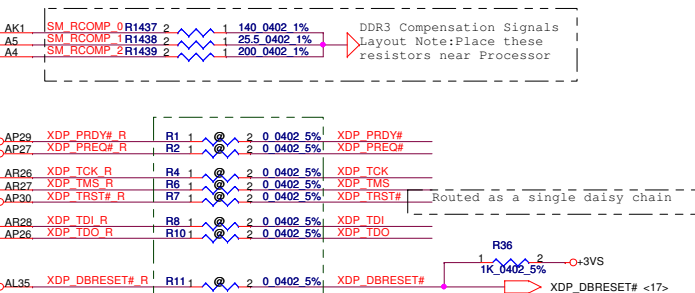
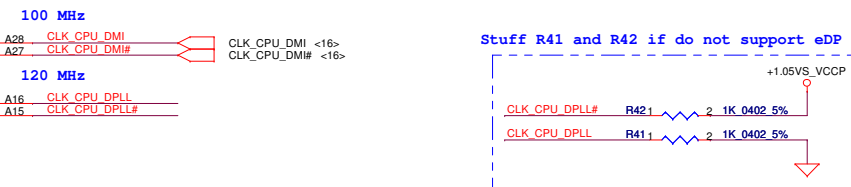
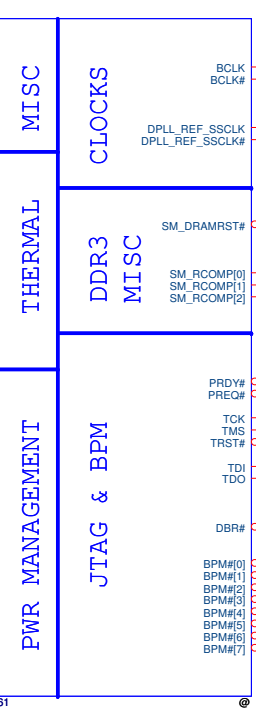
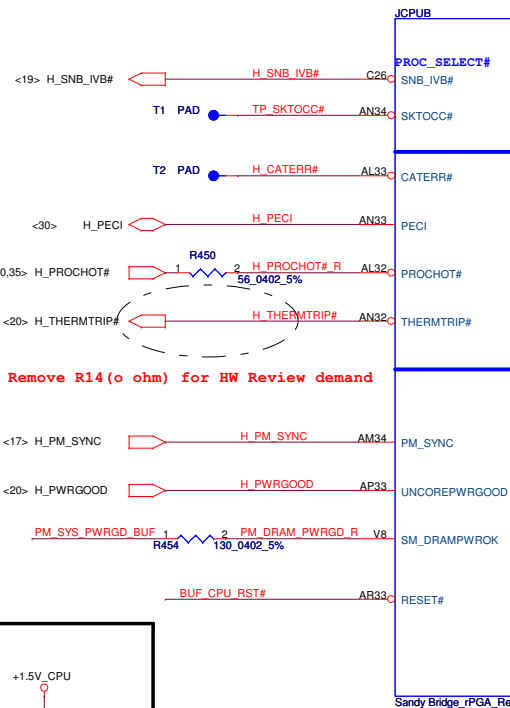
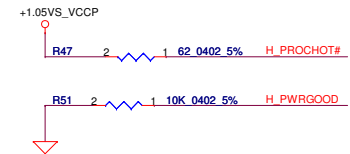
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

BTO Option Table

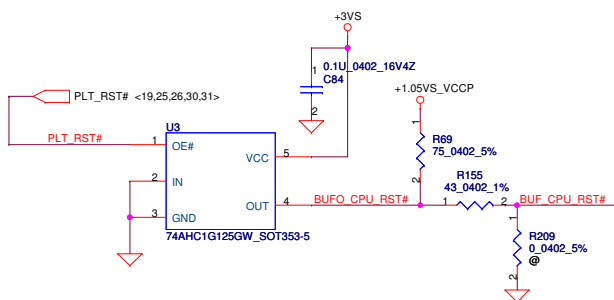
Function	MINI PCI-E SLOT	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
description	SLOT1	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
explain	WIMAX	10/100M	Giga	Camera & Mic	PWM	RPM	1.5V	1.5VS	Old Sch.	New Sch.
BTO	WIMAX@	8105E@	8111E@	CAM@	PWM@	RPM@	WPS3@	PS3@	OLS@	NLS@

STATE SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

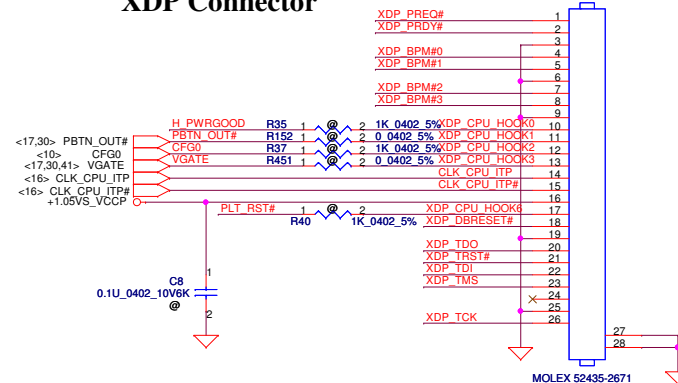
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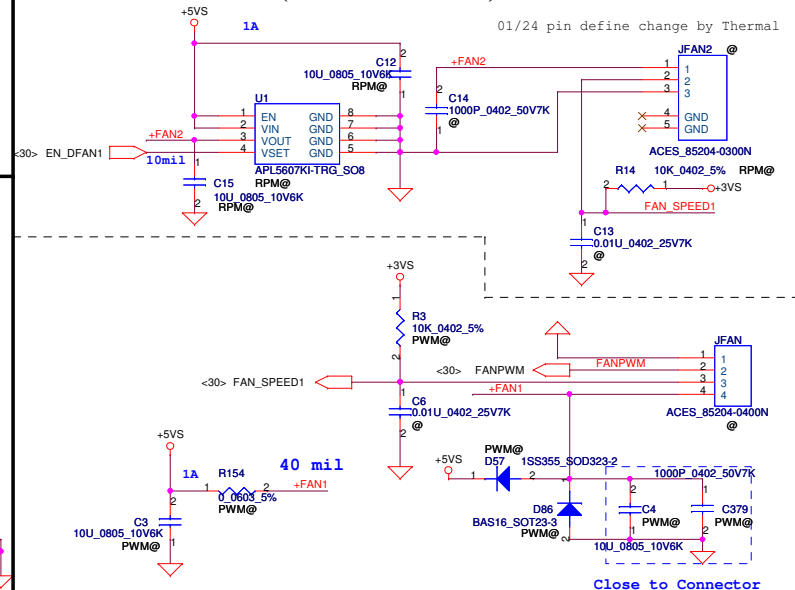
Buffered Reset to CPU



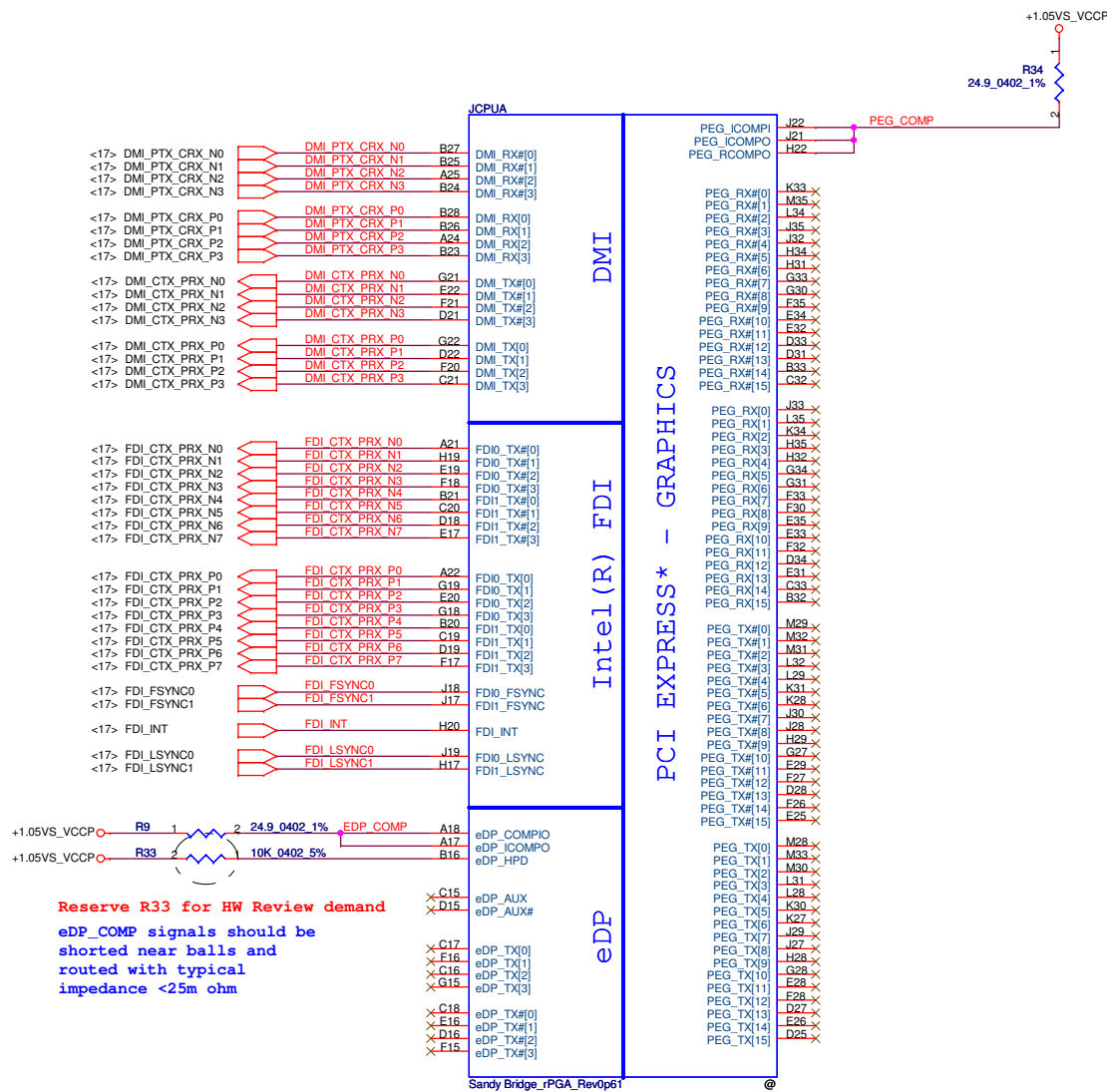
XDP Connector



FAN Control Circuit (RPM and PWM)

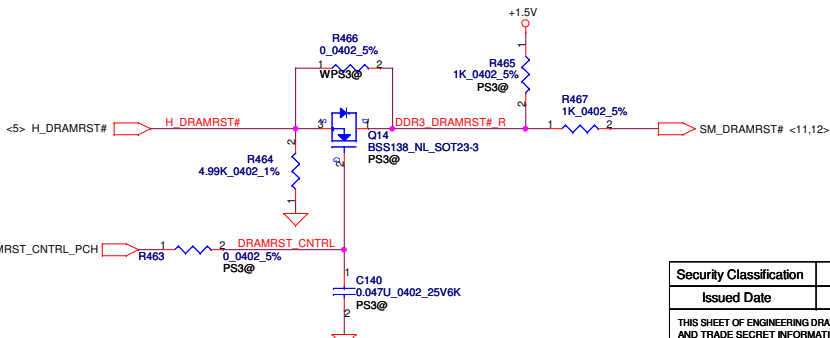
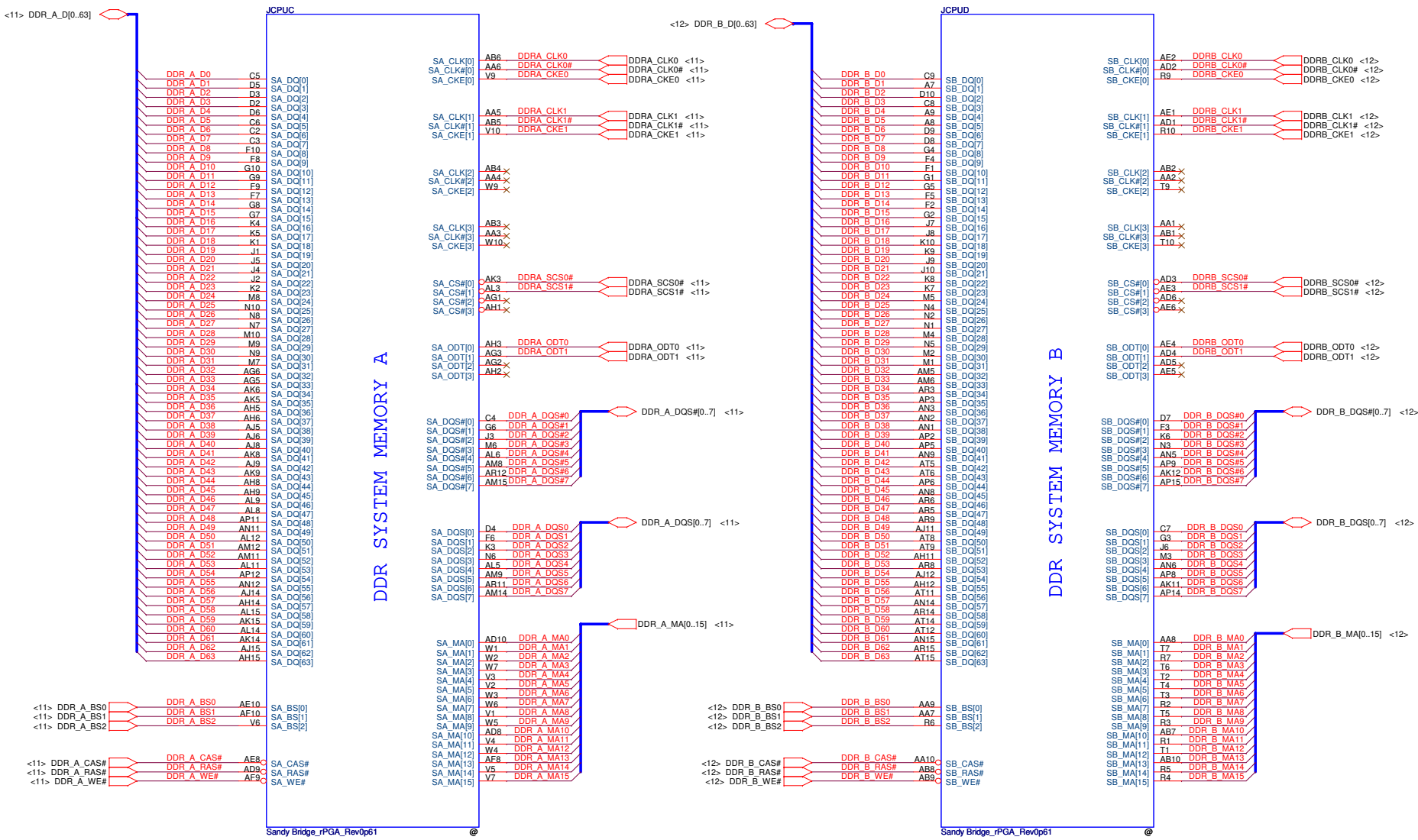


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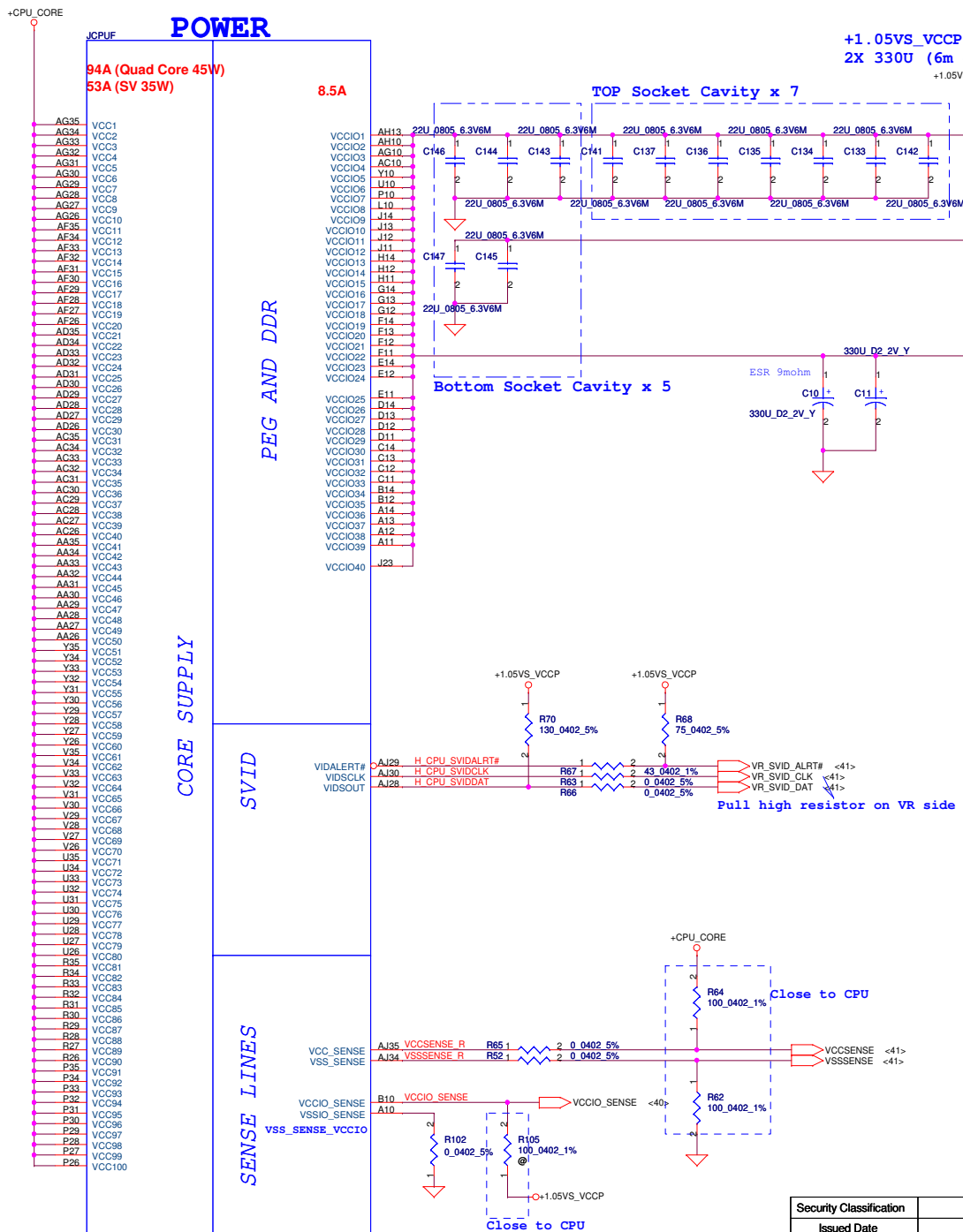


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

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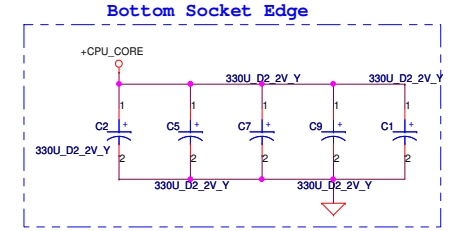
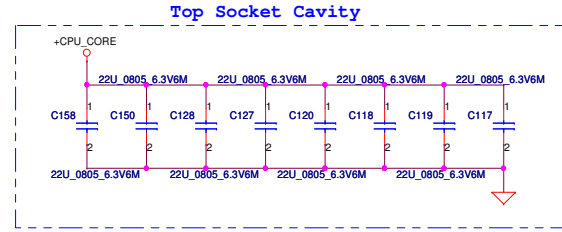
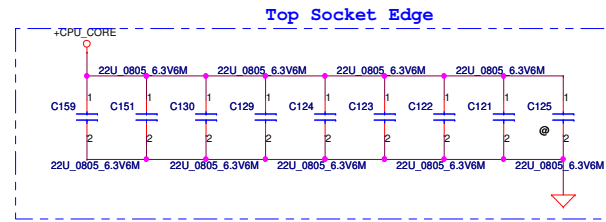
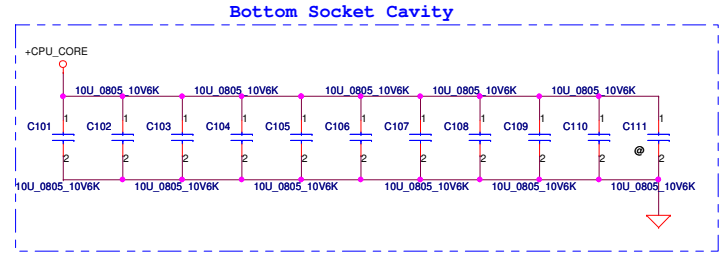


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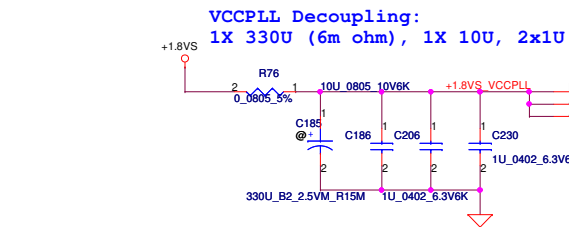
+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



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+GFX_CORE
Change C873 from 330uF to 560uF for power issue



SENSE
LINES

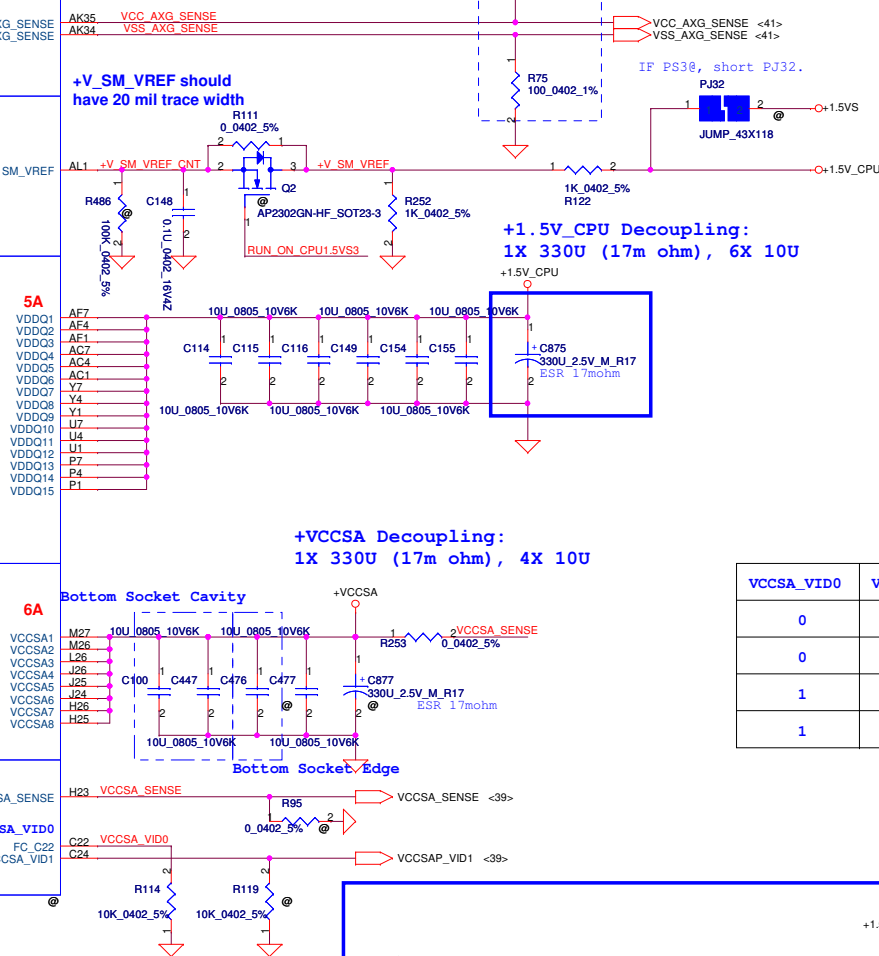
1.8V RAIL

VREF

DDR3 -1.5V RAILS

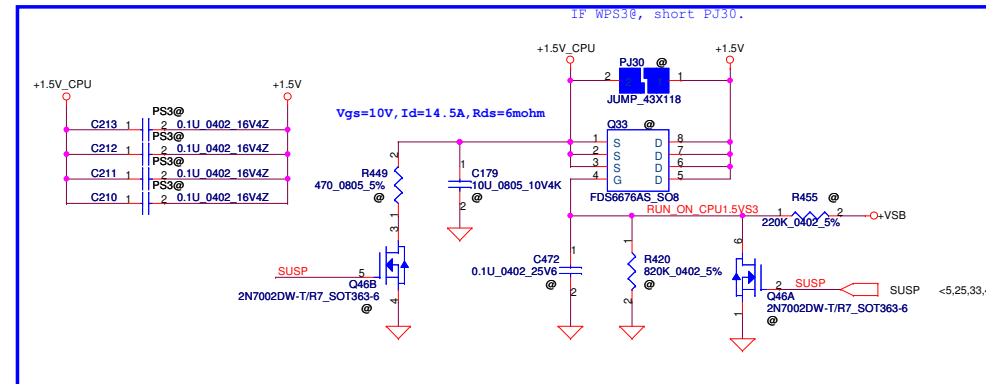
A RAIL

MISC

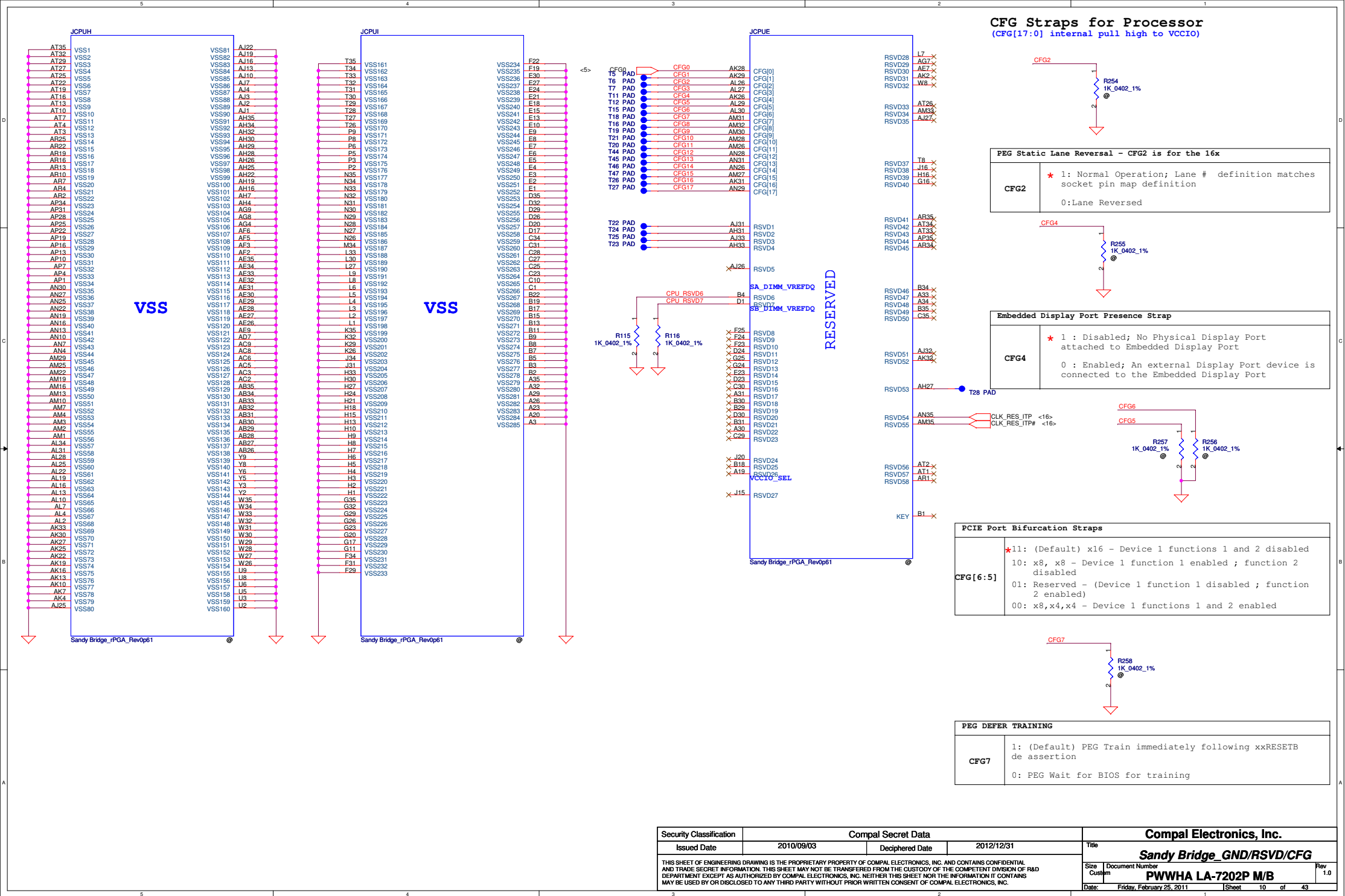


VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge

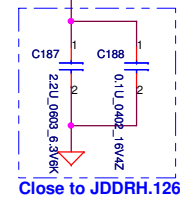
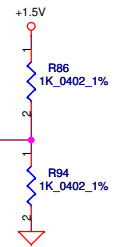
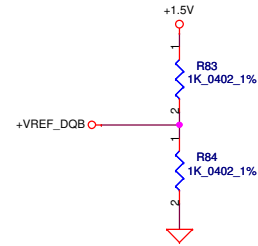
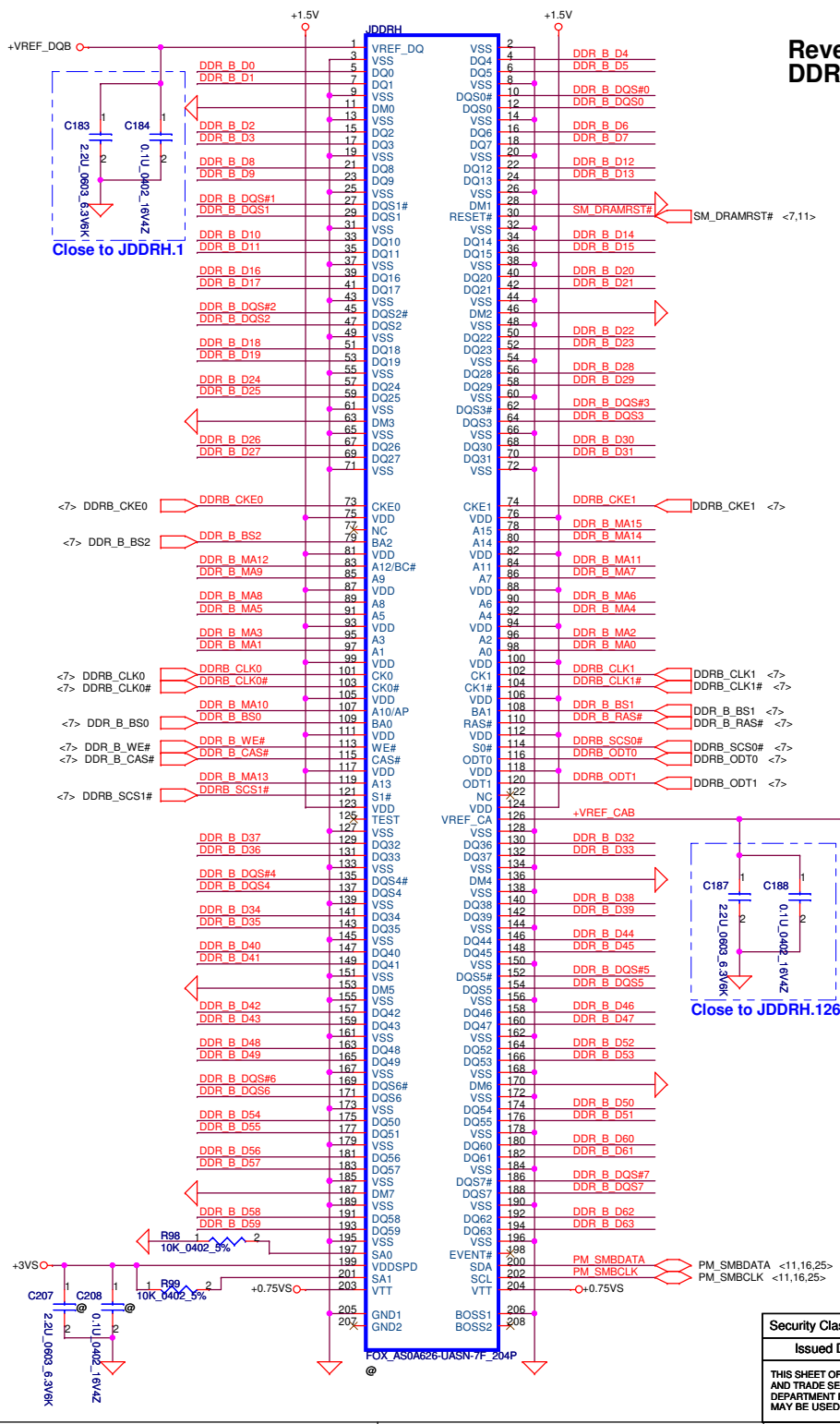


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				Sandy Bridge_GND/RSVD/CFG	
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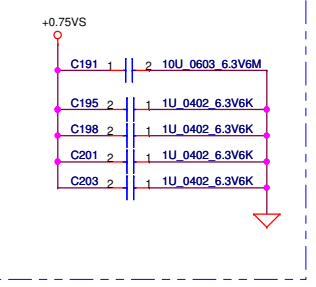
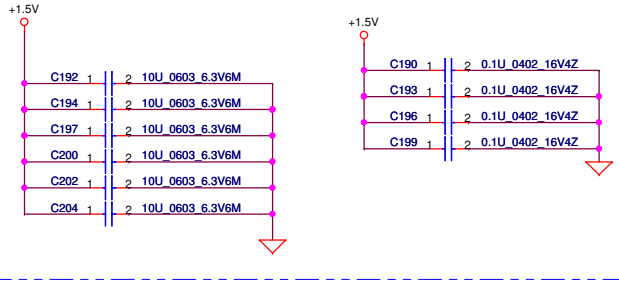
Reverse Type DDR3 SO-DIMM B



Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204



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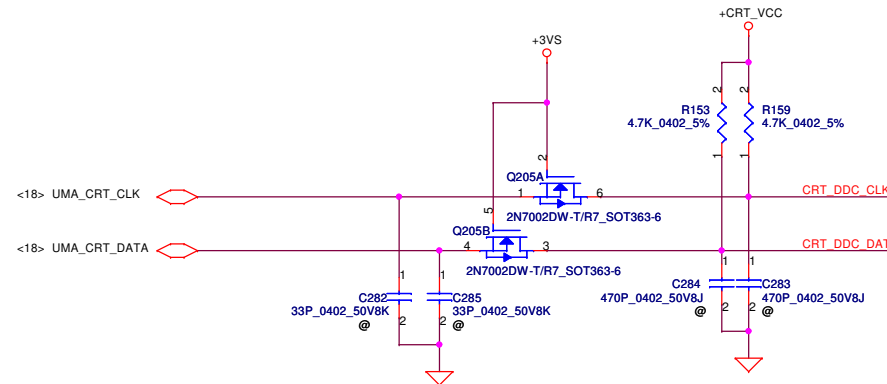
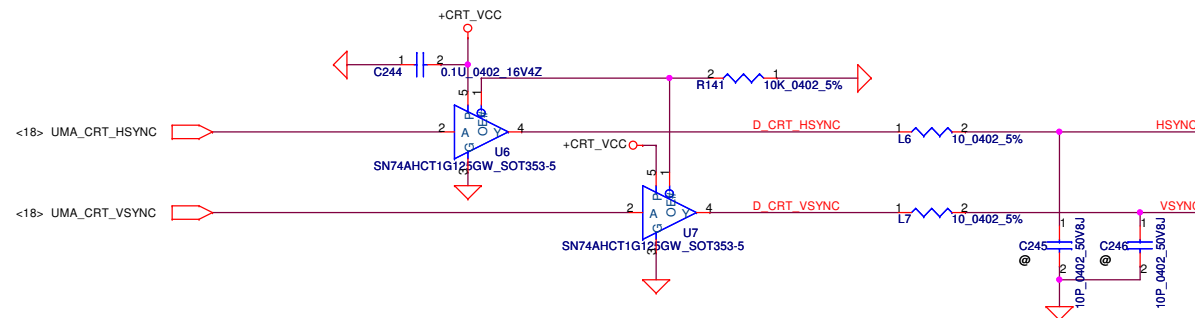
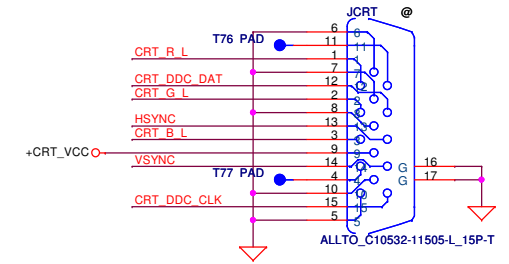
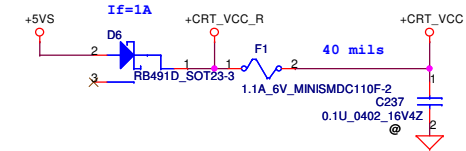
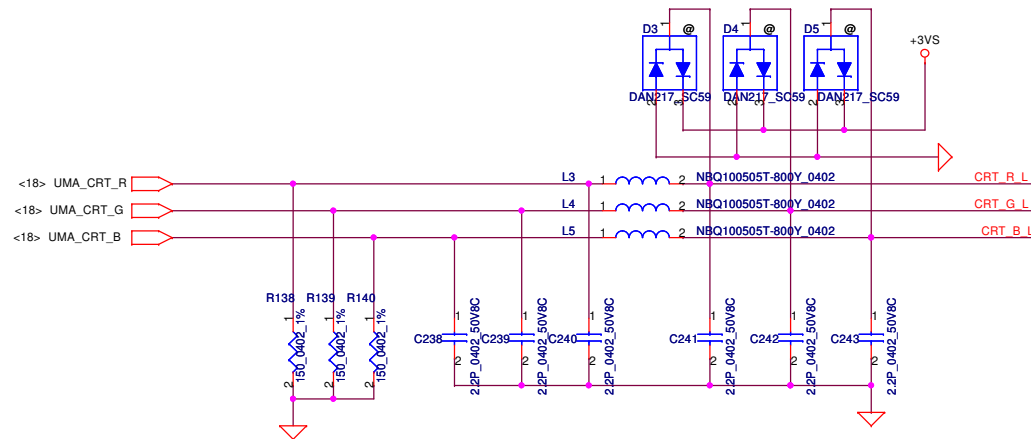


LCD/PANEL BD. Conn.

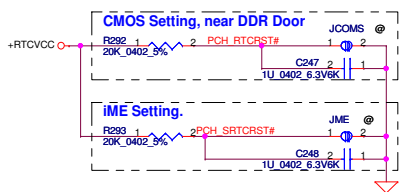


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CRT CONNECTOR

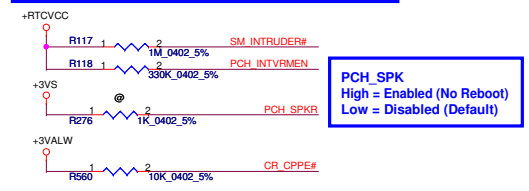


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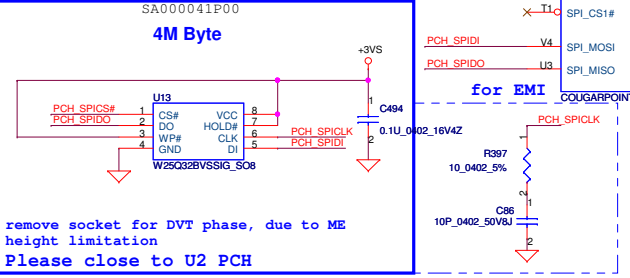
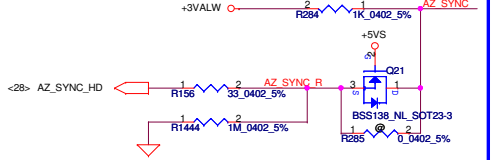
Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

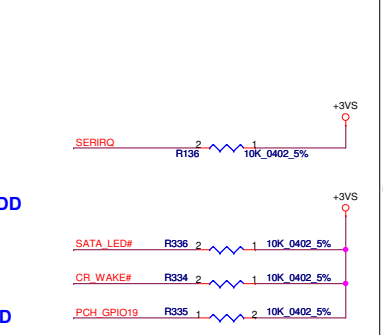
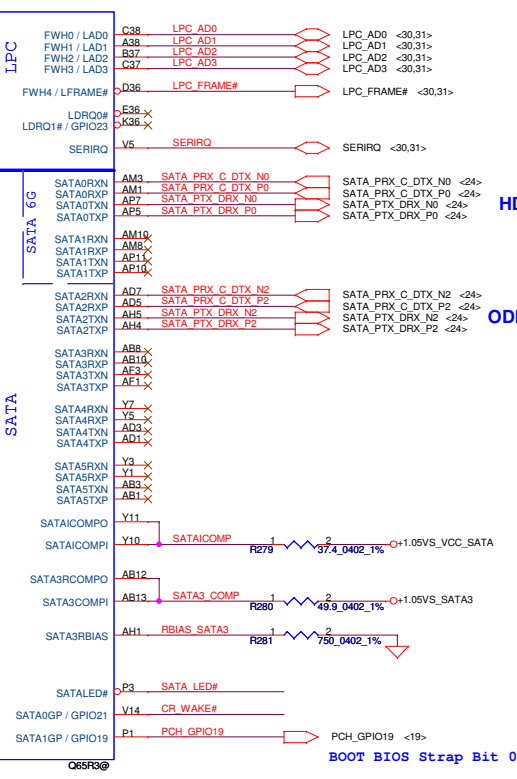
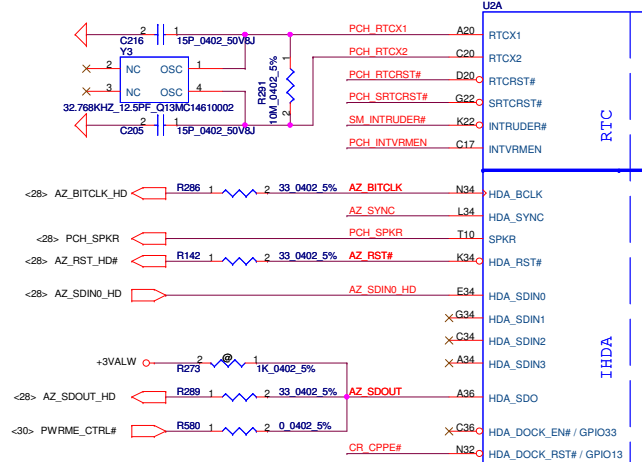


HDA_SDO
ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

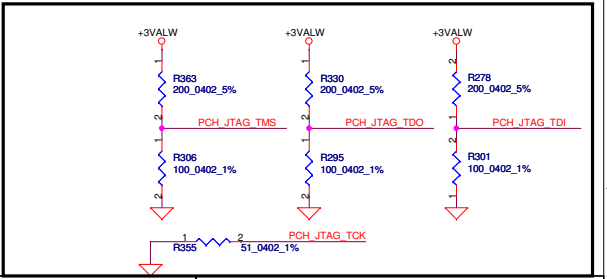
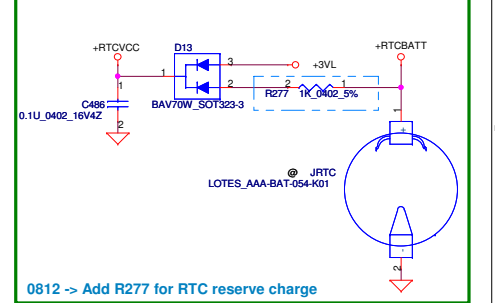
HDA_SYNC
★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



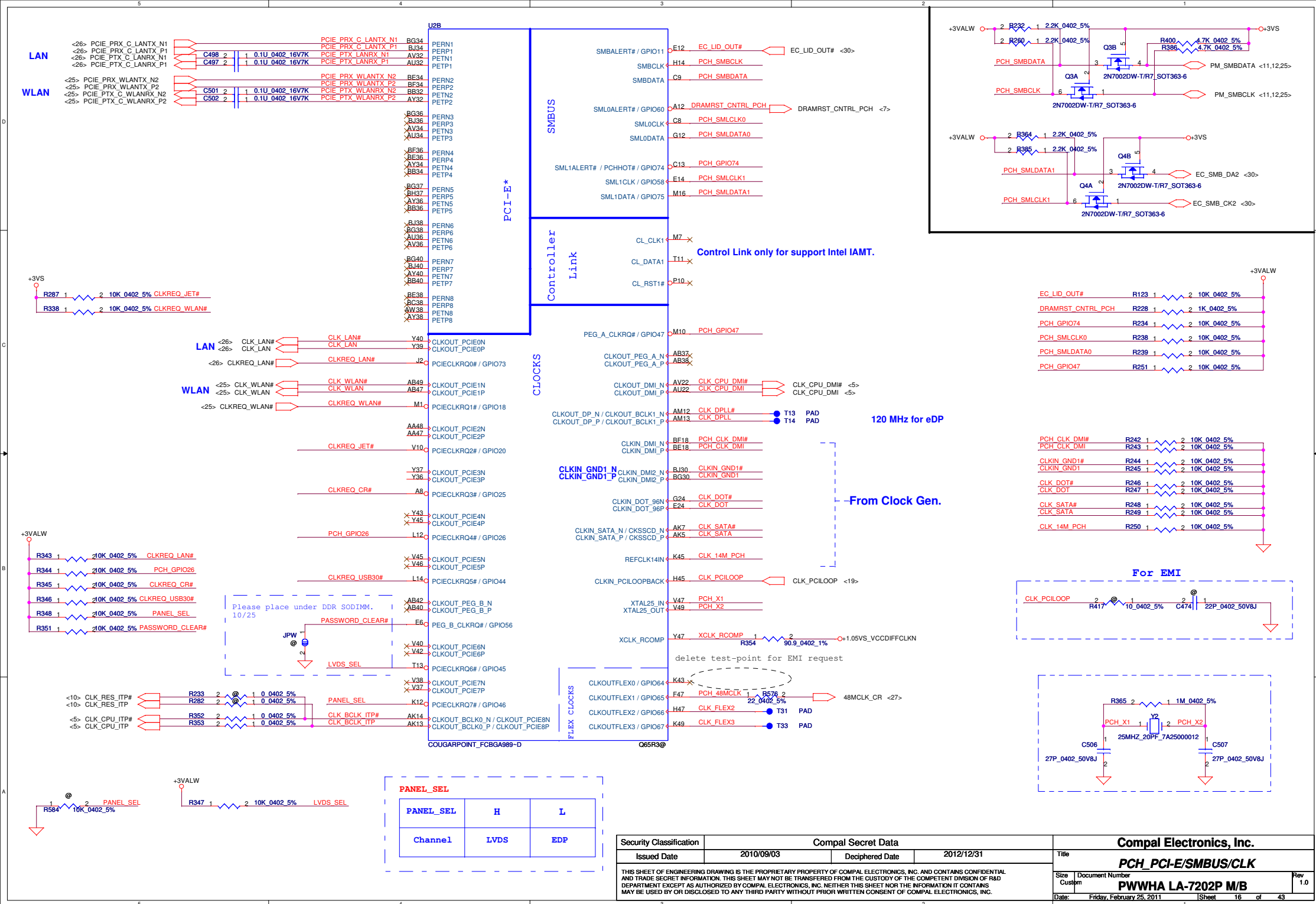
remove socket for DVT phase, due to ME height limitation
Please close to U2 PCH

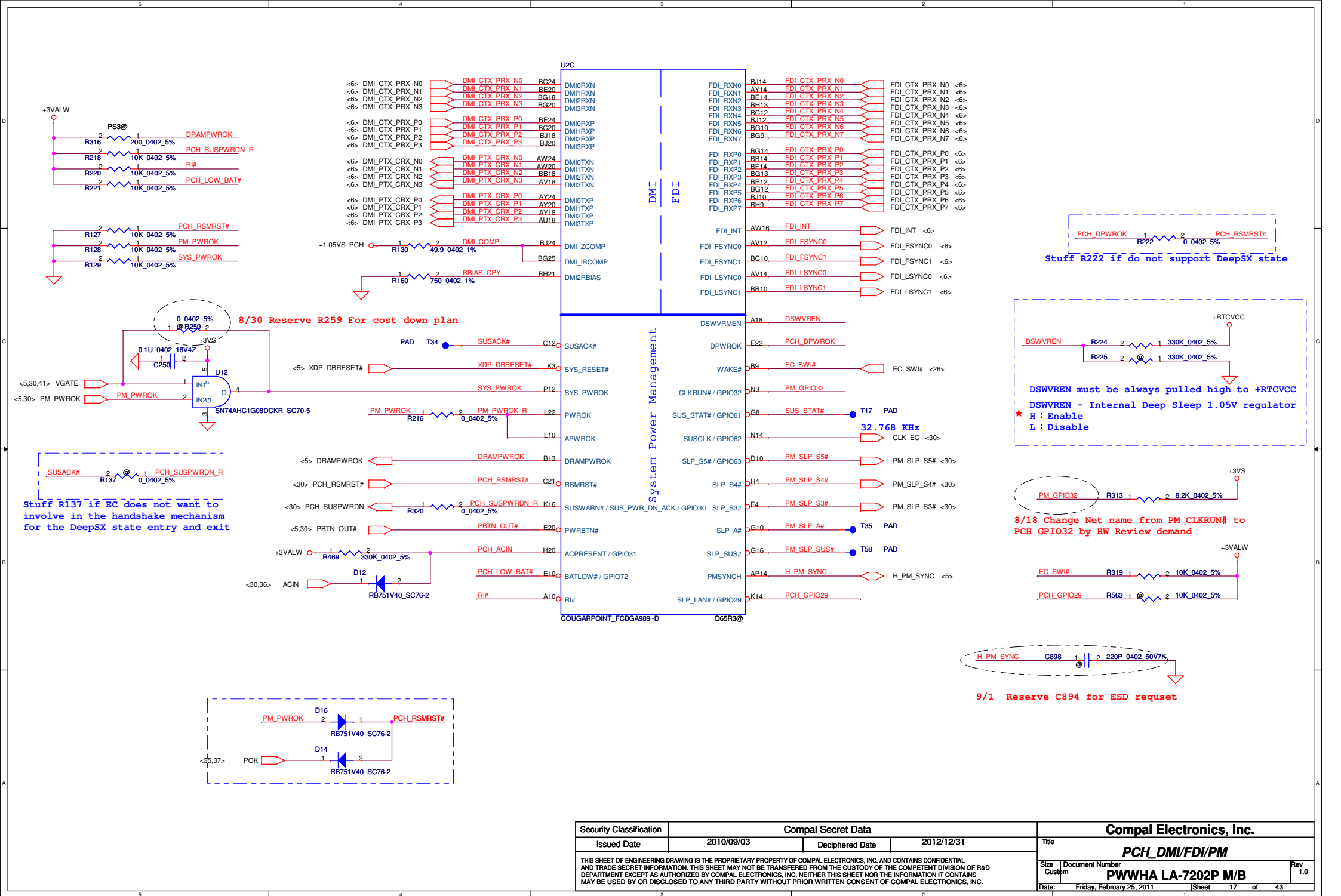


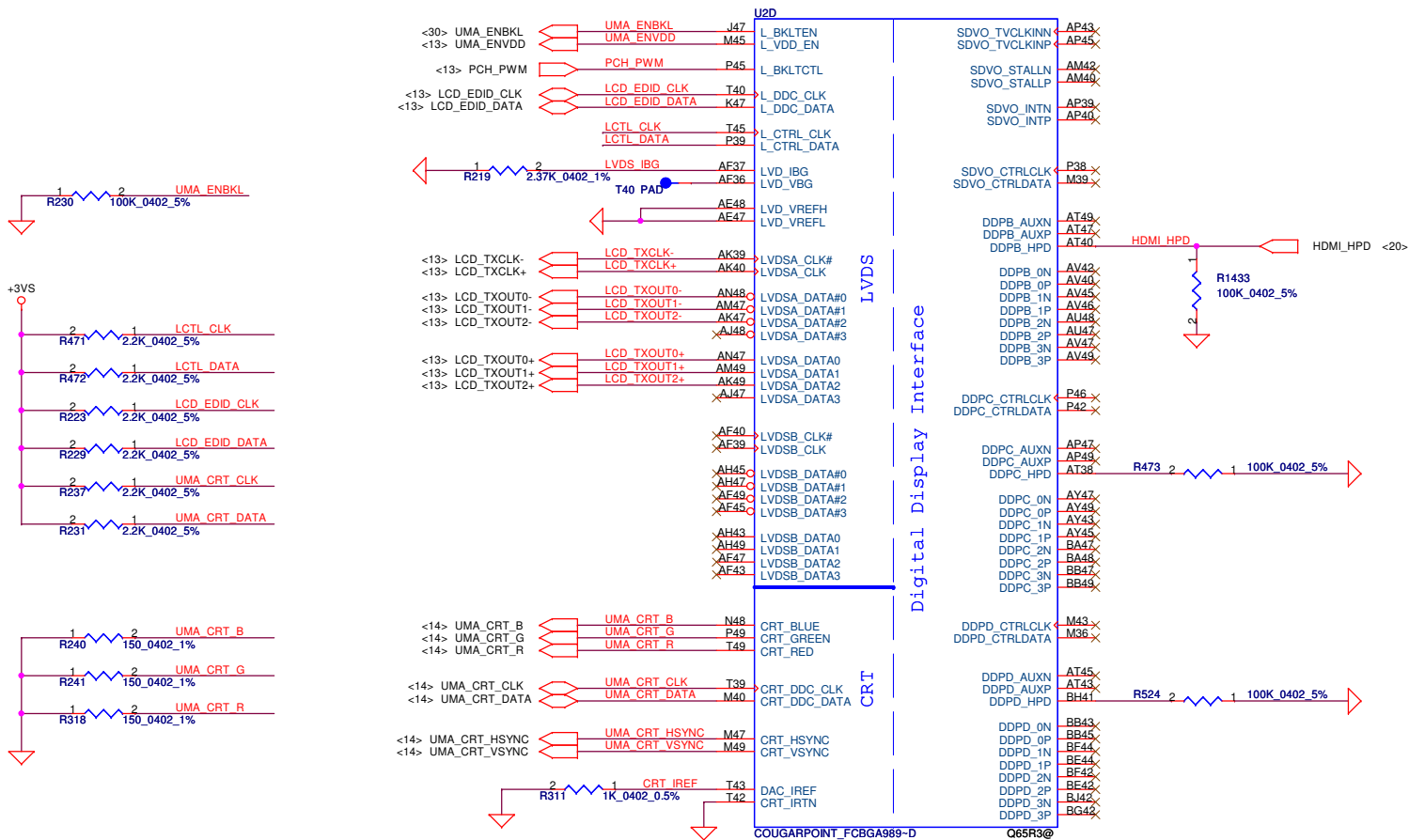
RTC schematic for non-chargeable



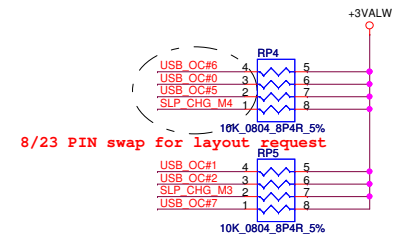
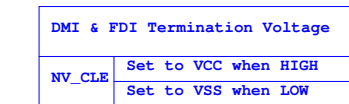
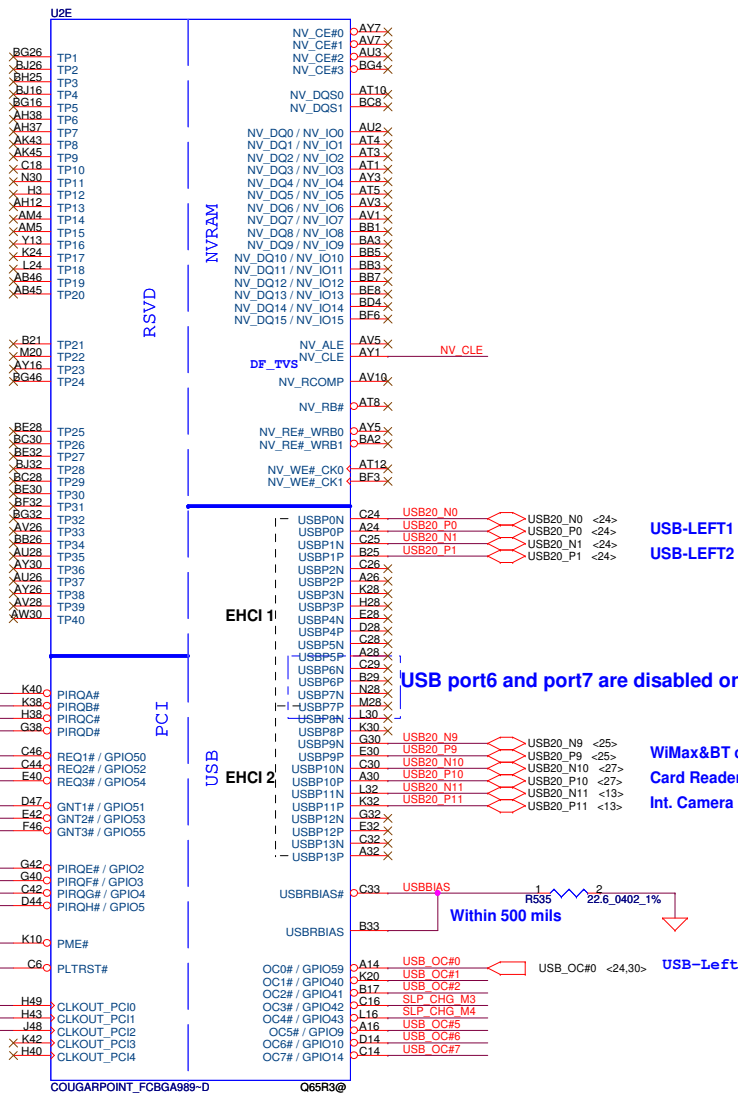
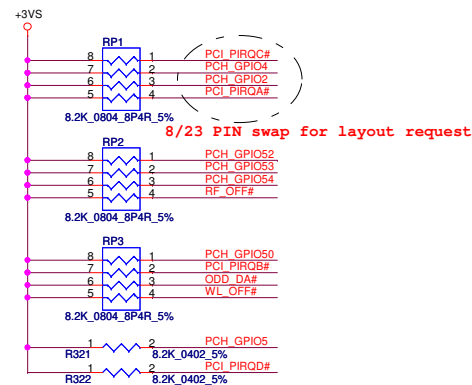
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	PCH_HDA/JTAG/SATA/SPI/LPC	
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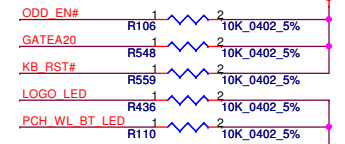
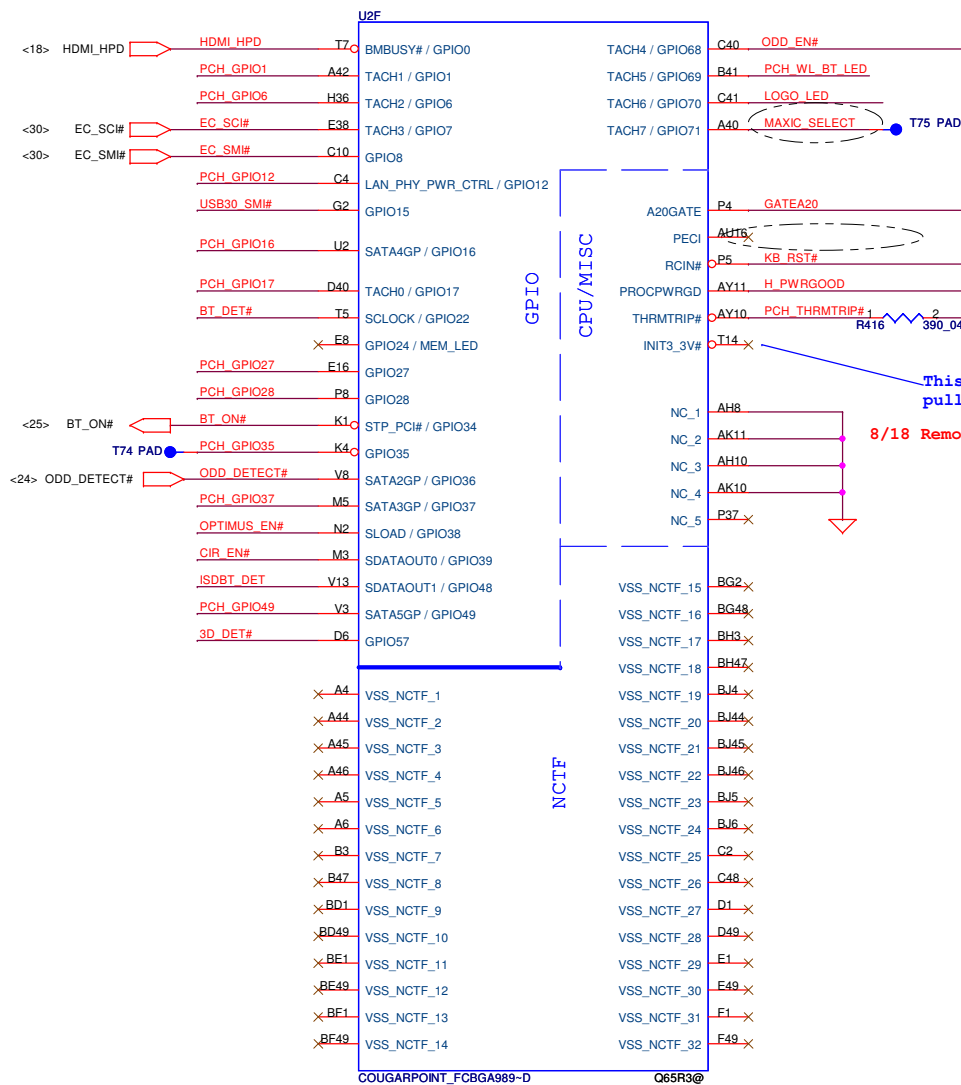
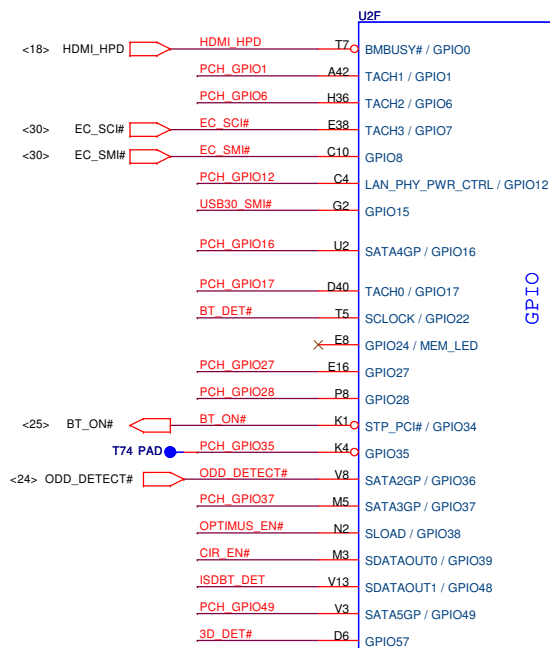
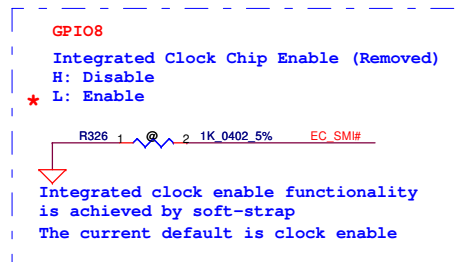
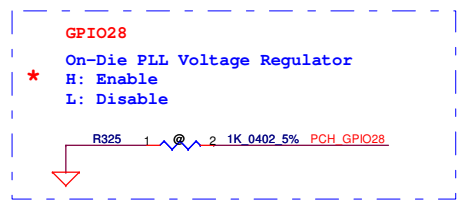
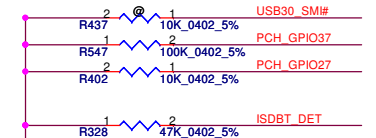
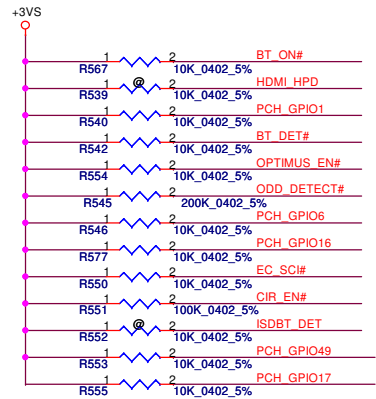
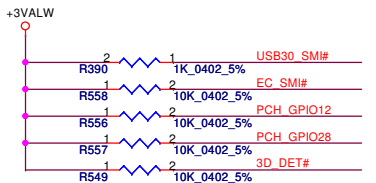


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Size	Custom	Document Number	PWWHA LA-7202P M/B	Rev	1.0
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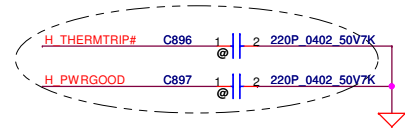


Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

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				Custom	PWWHA LA-7202P M/B		1.0
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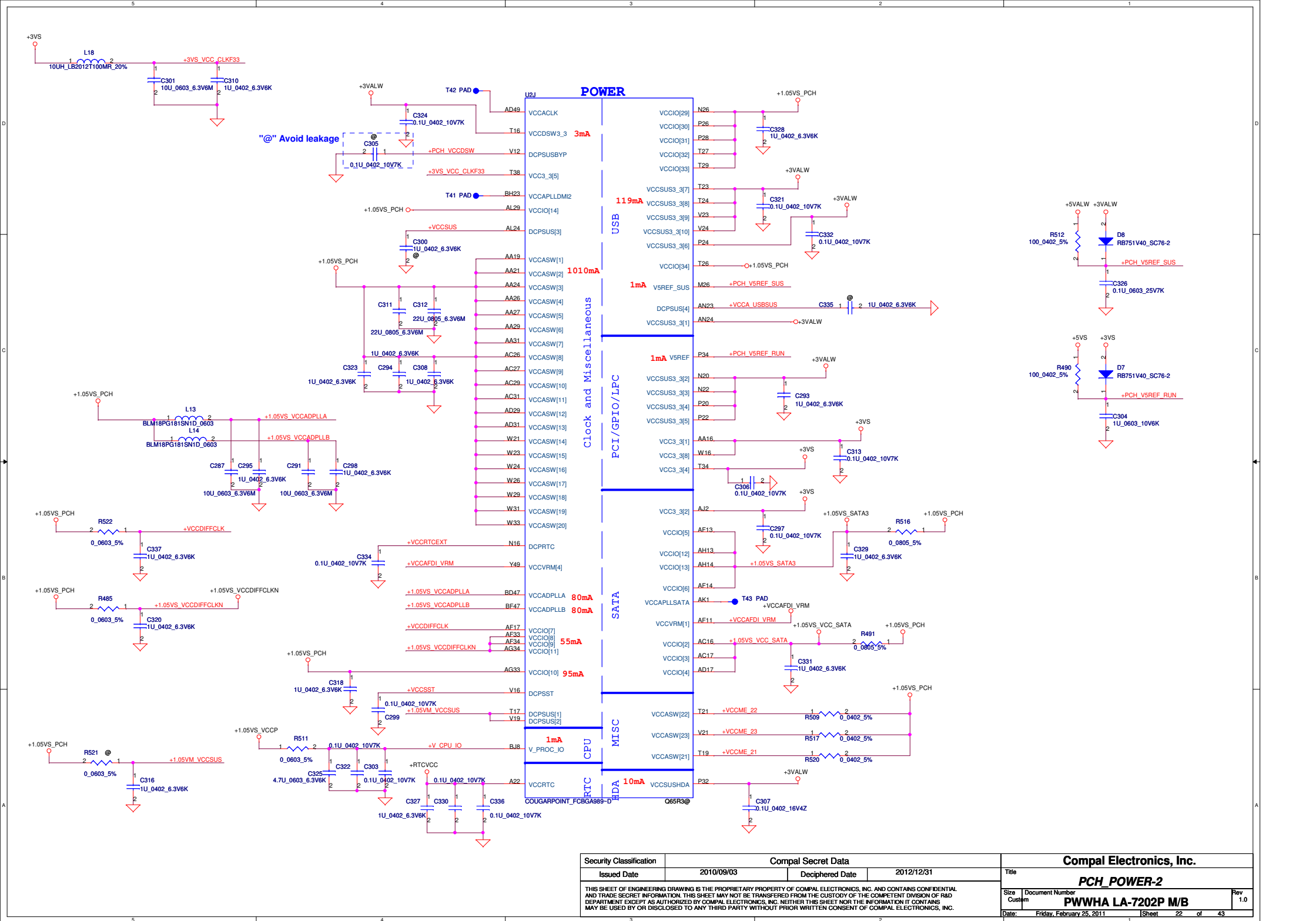


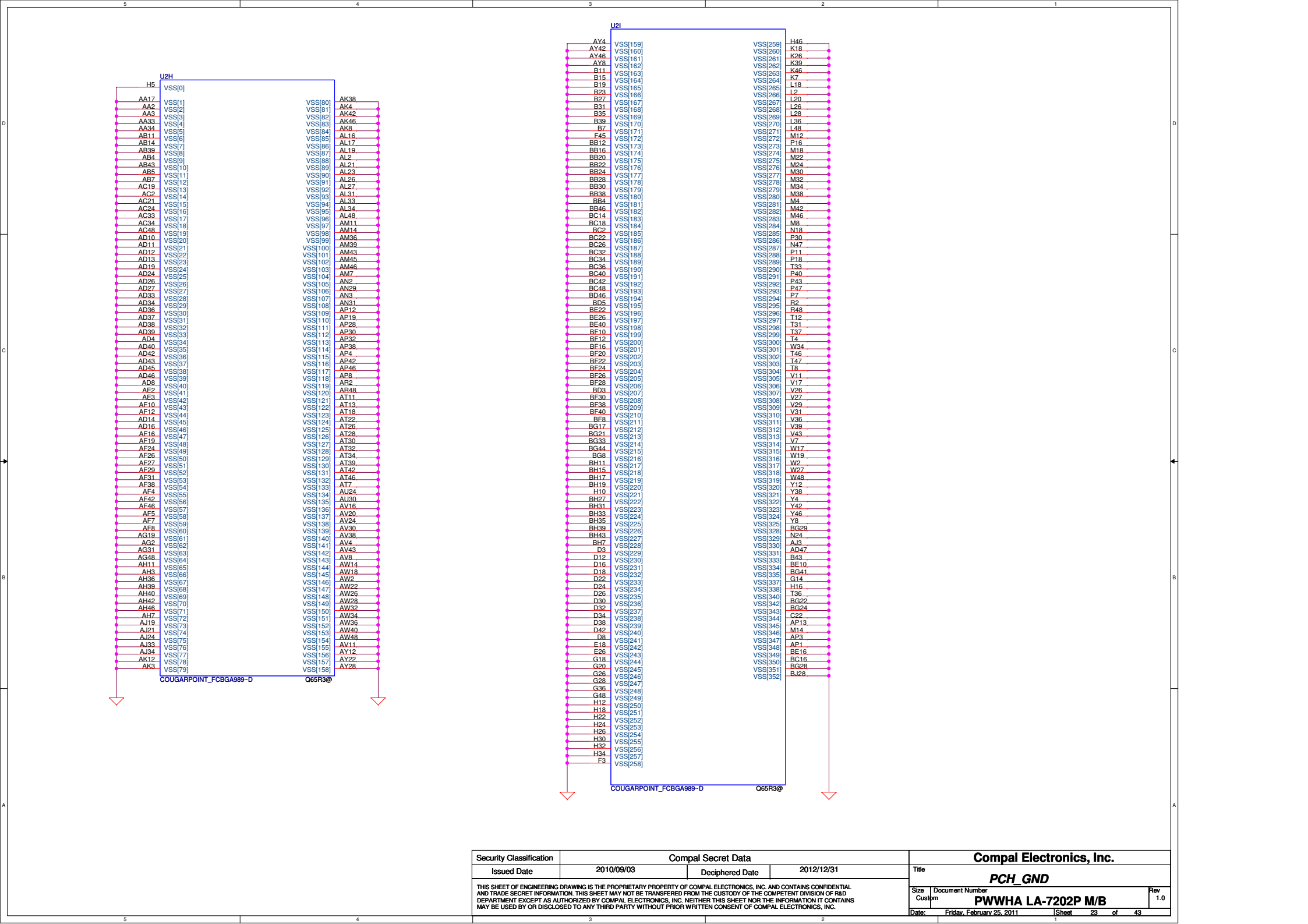
This signal has weak internal pull-up, can't be pulled low
8/18 Remove PCH Peci by HW Review demand



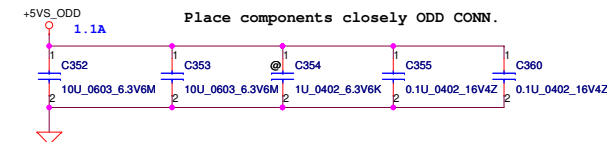
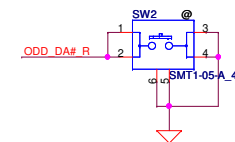
9/1 Reserve C896, C897 for ESD request

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Size	B	Document Number	PWWHA LA-7202P M/B	Rev	1.0
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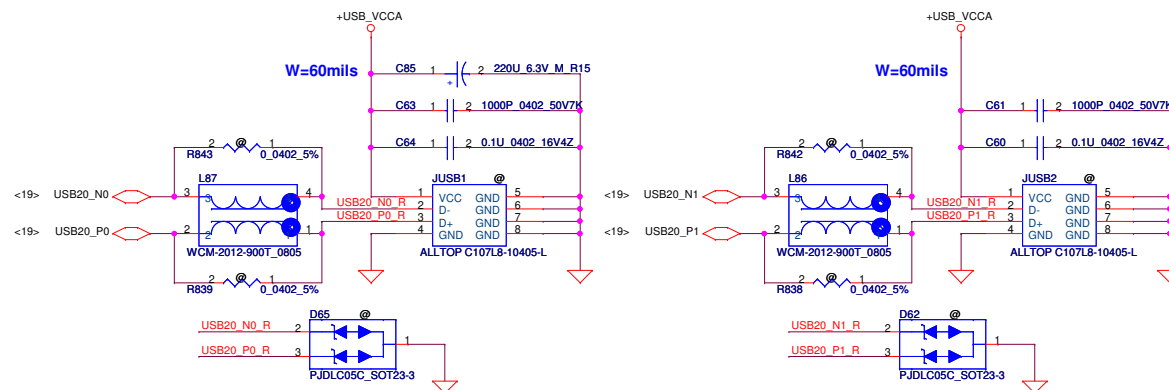
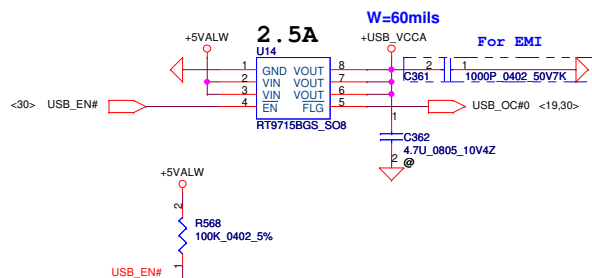




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Size		Document Number		Rev	
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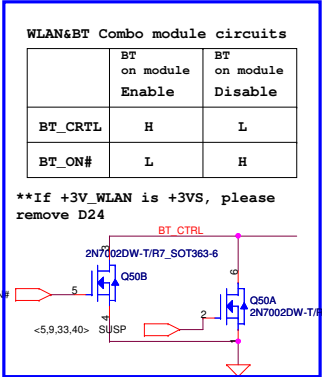


USB Conn. Left Side



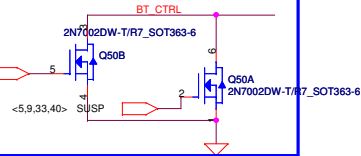
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Issued Date		2010/09/03	Deciphered Date		2012/12/31	
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				SATA-HDD/ODD/USB		
				Size	Document Number	Rev
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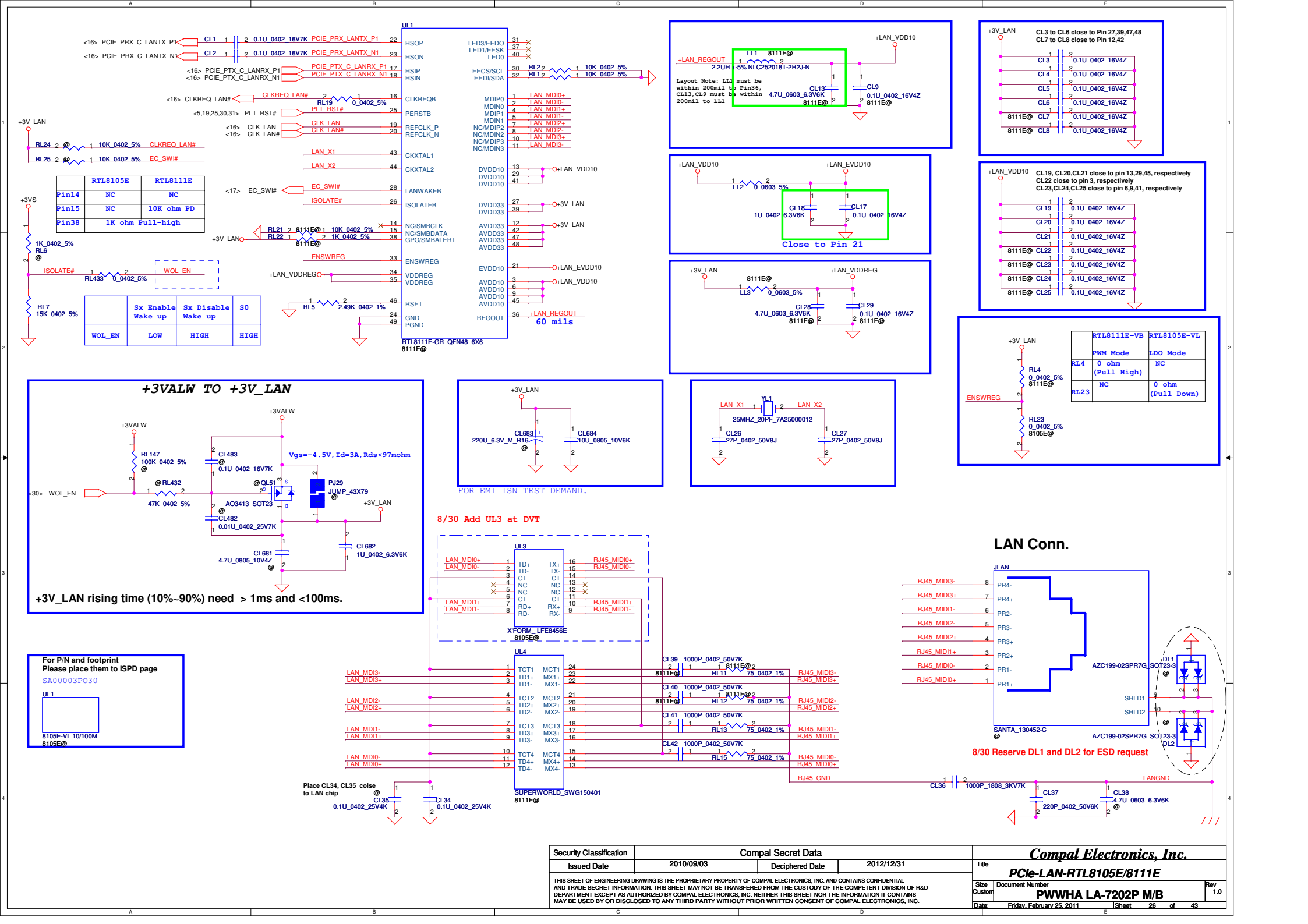
Short PJ27 for Wimax
Short PJ26 for WLAN

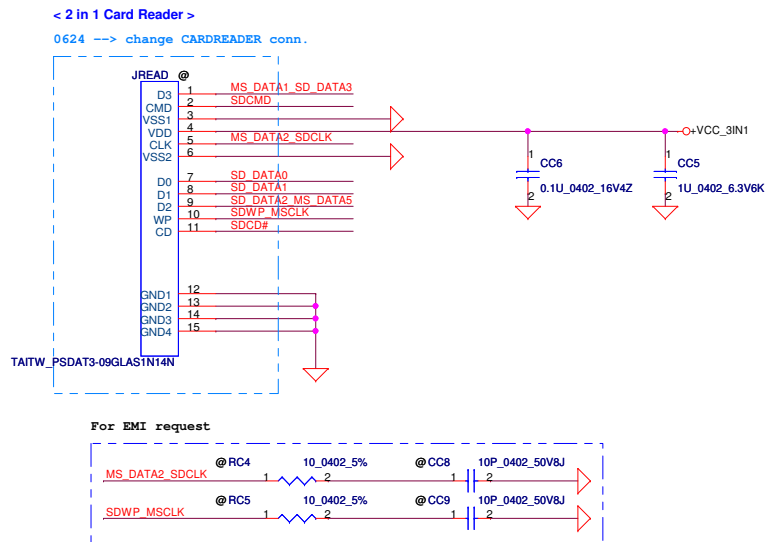
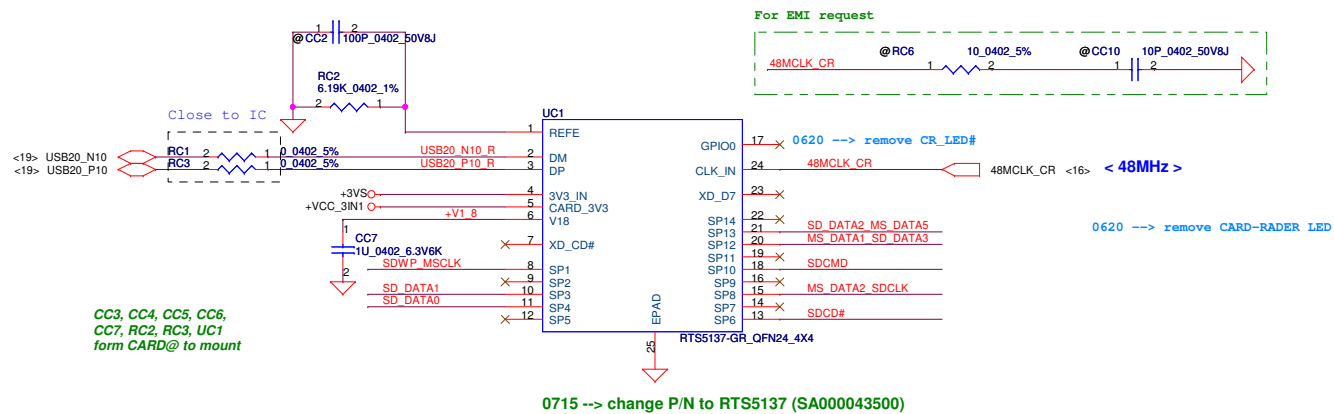


	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H

****If +3V_WLAN is +3VS, please
remove D24**

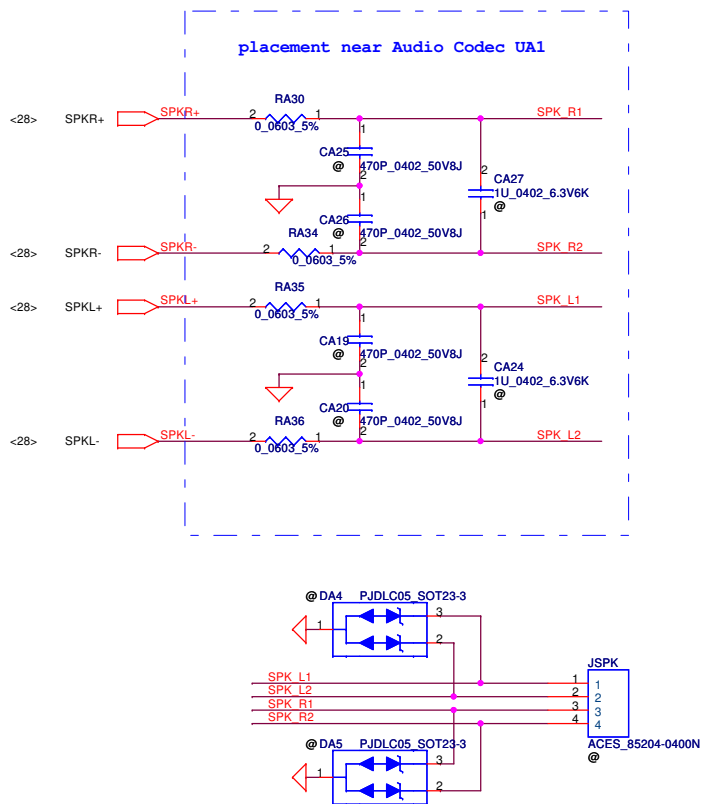




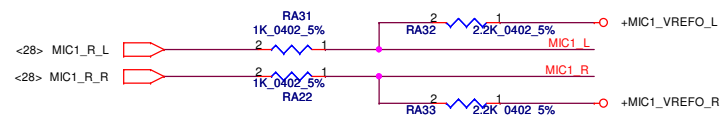


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Size	Custom	Document Number	PWWHA LA-7202P M/B	Rev	1.0
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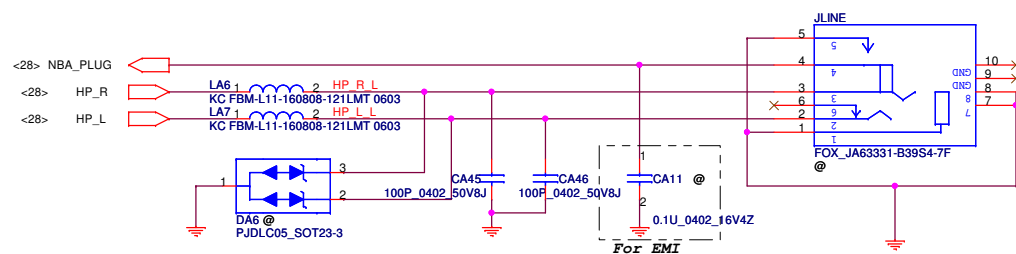
Speaker Connector



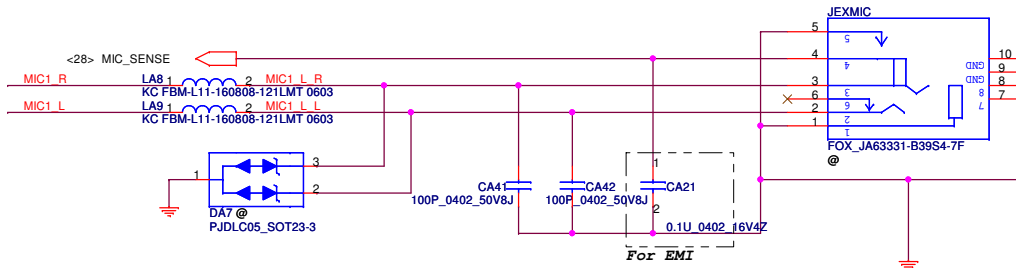
Ext. Mic



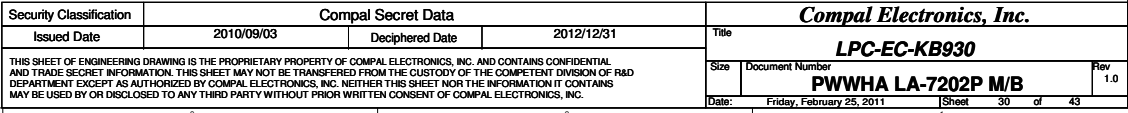
HeadPhone/LINE Out JACK



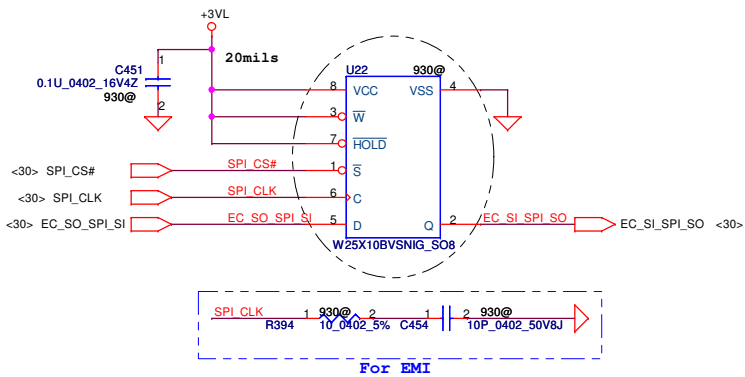
Ext.MIC/LINE IN JACK



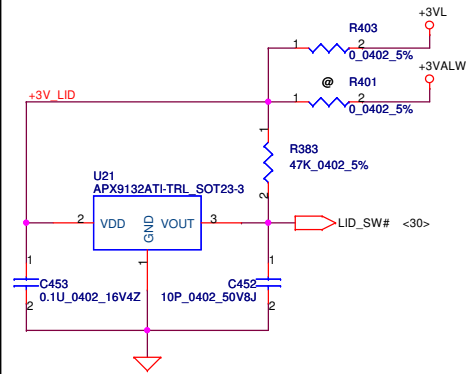
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title AUDIO AMP/MIC/SPK/VR		
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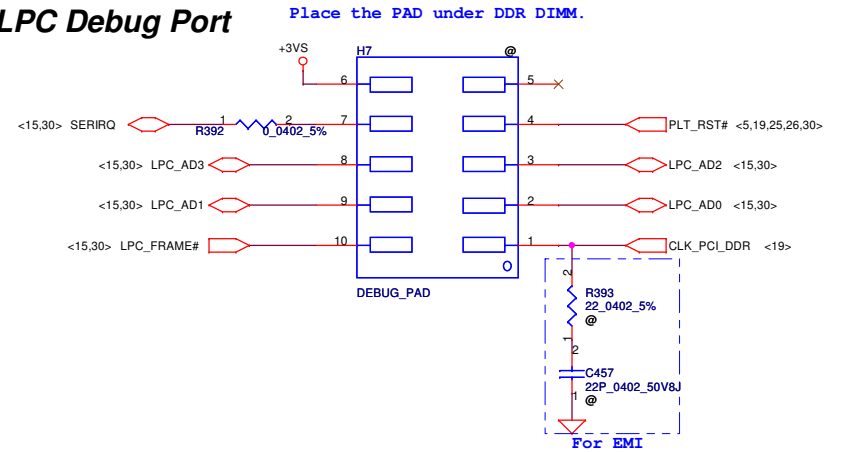
SPI Flash (256KB)



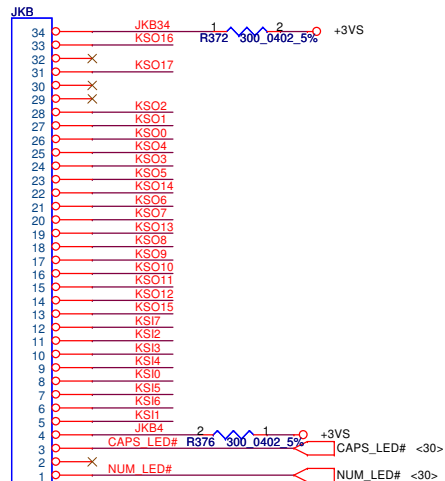
Lid SW



LPC Debug Port

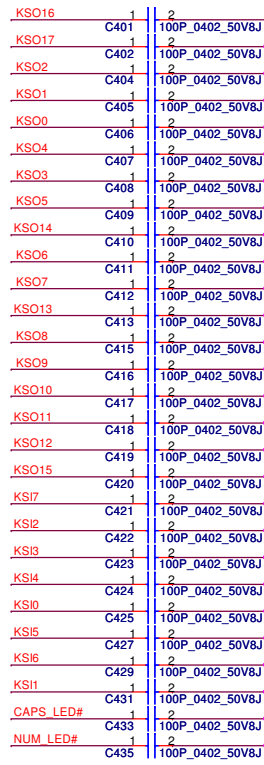


KEYBOARD CONN.



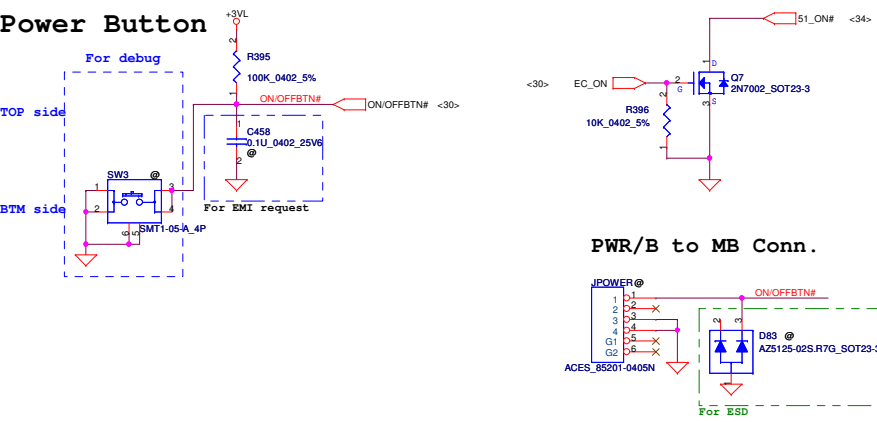
For EMI

Close to JKB

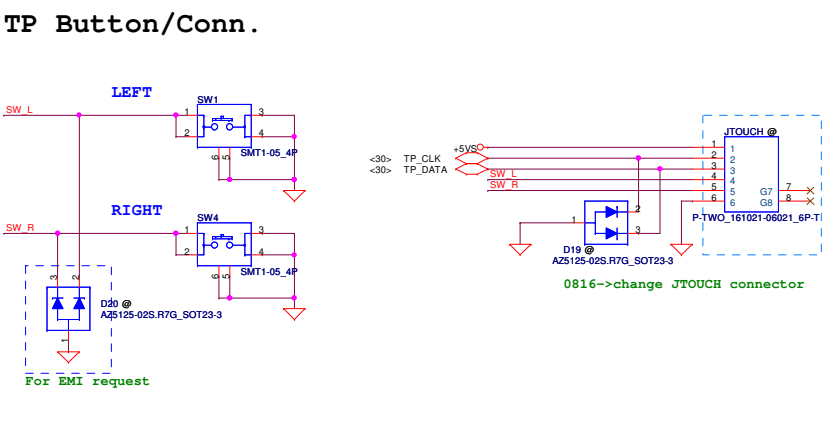


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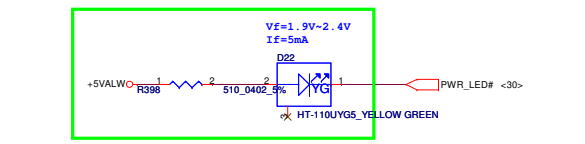
Power Button



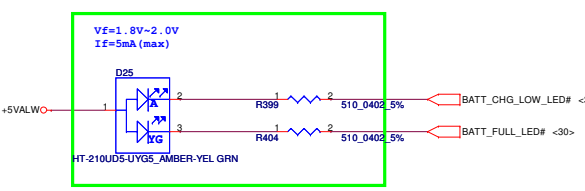
TP Button/Conn.



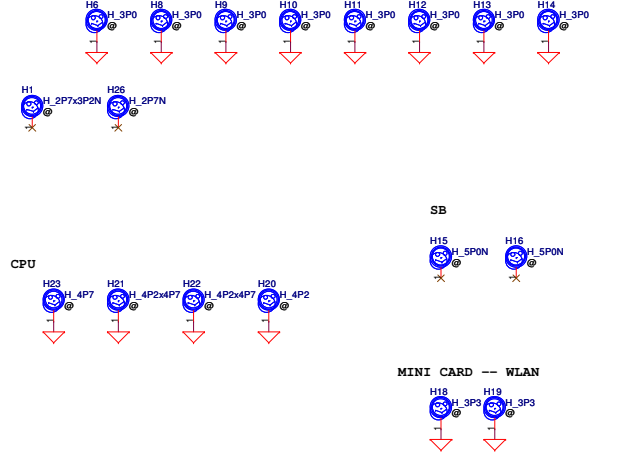
POWER/SUSPEND LED



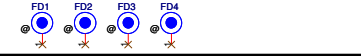
BATT CHARGE/FULL LED



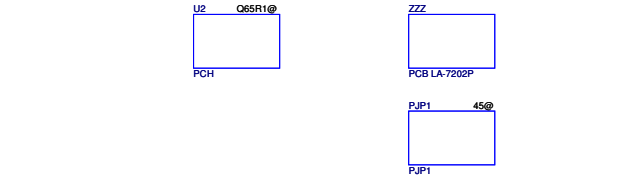
Screw Hole



PCB Fedical Mark PAD

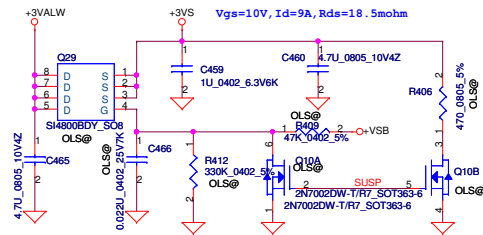


ISPD

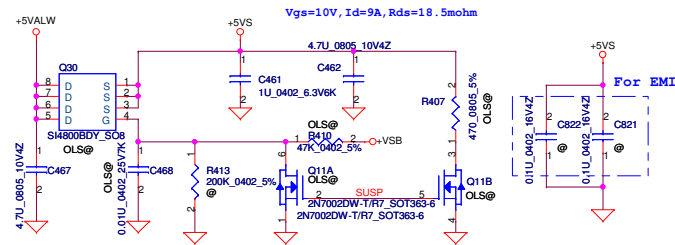


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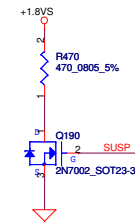
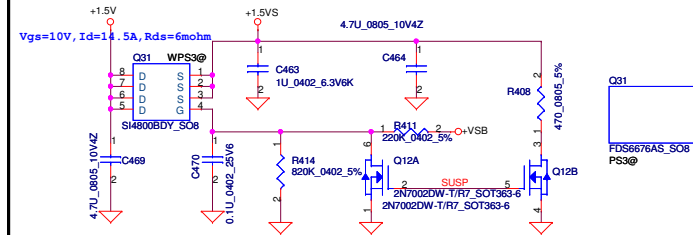
+3VALW TO +3VS



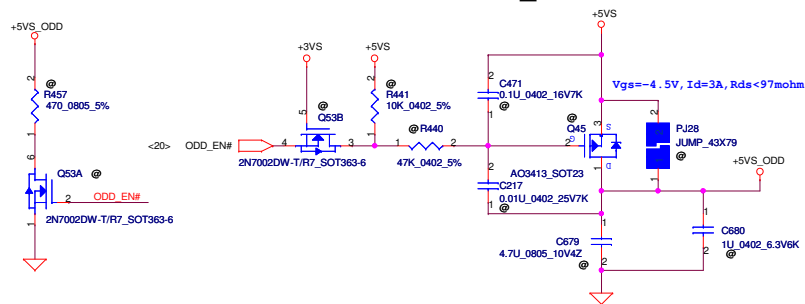
+5VALW TO +5VS



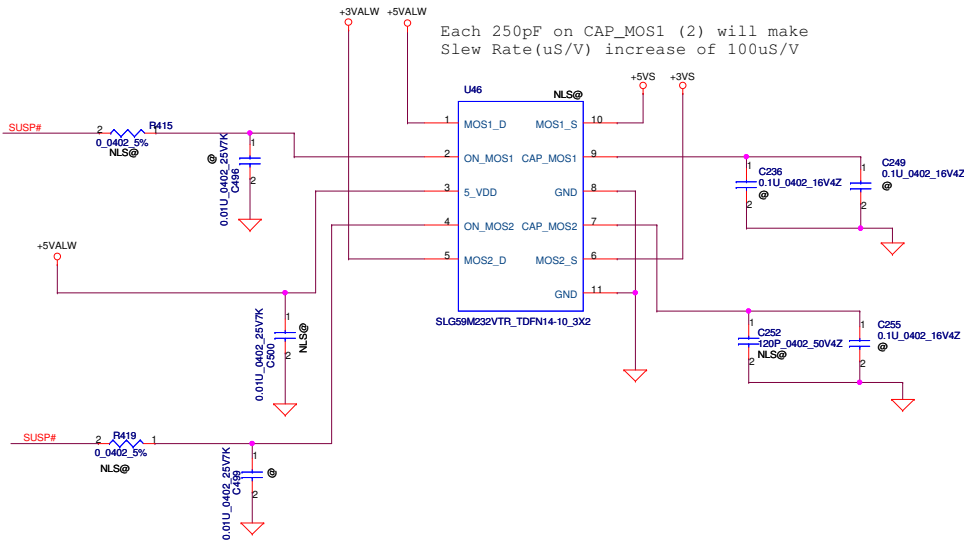
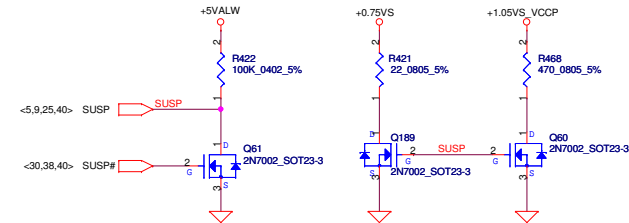
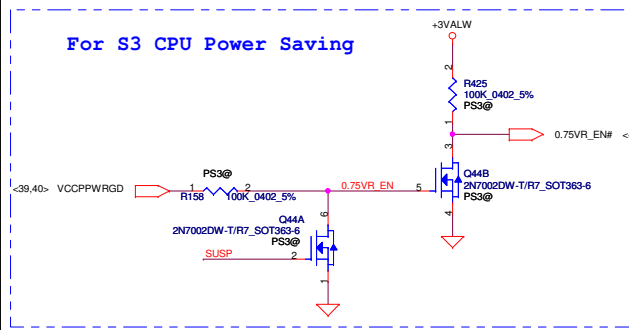
+1.5V to +1.5VS



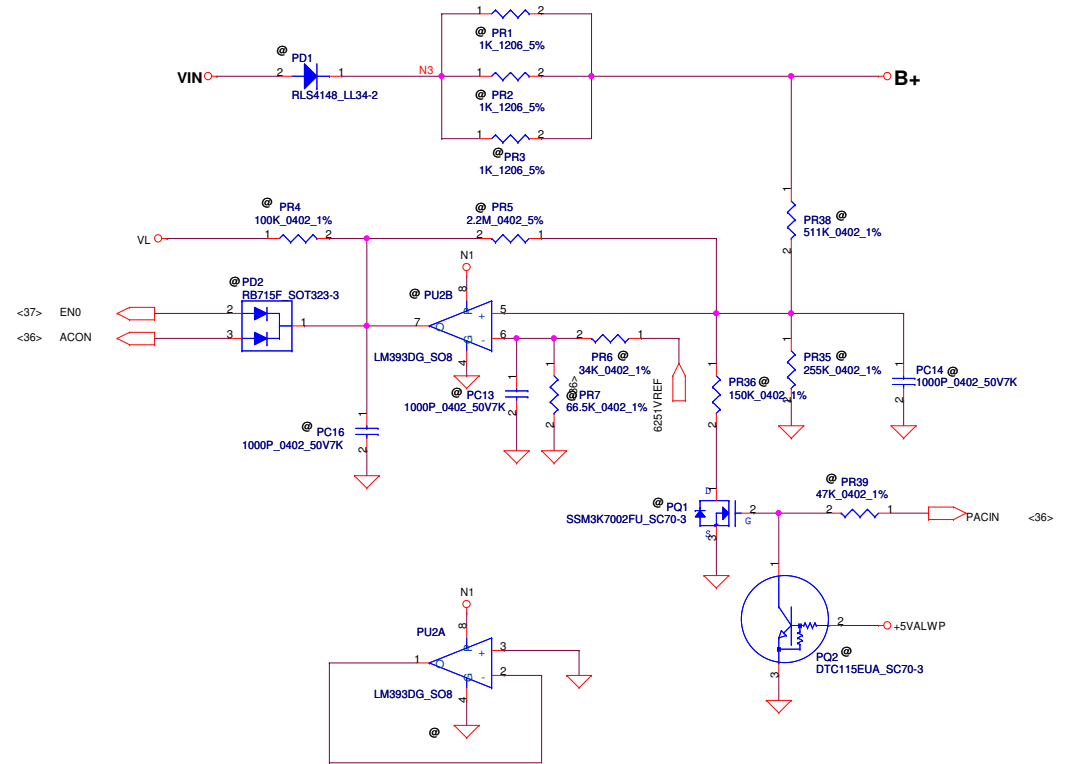
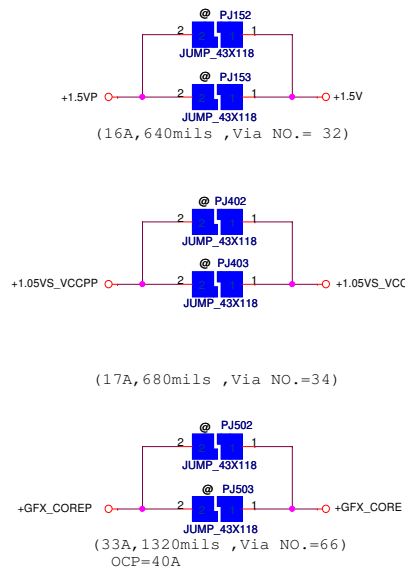
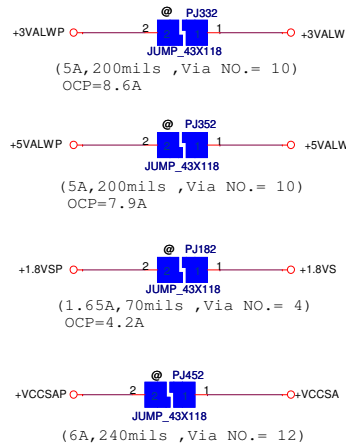
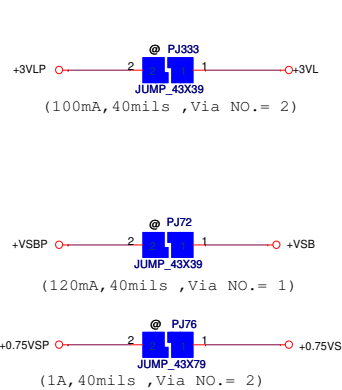
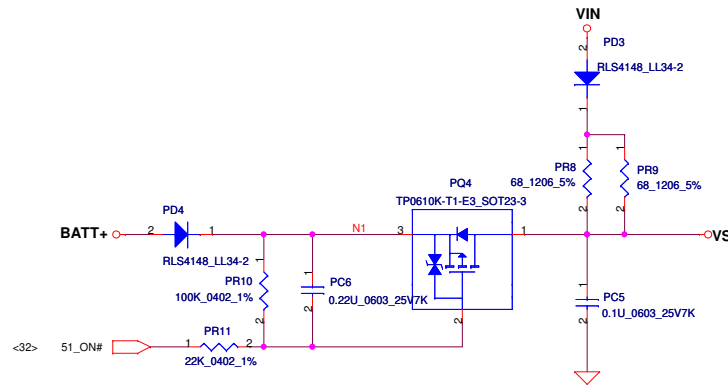
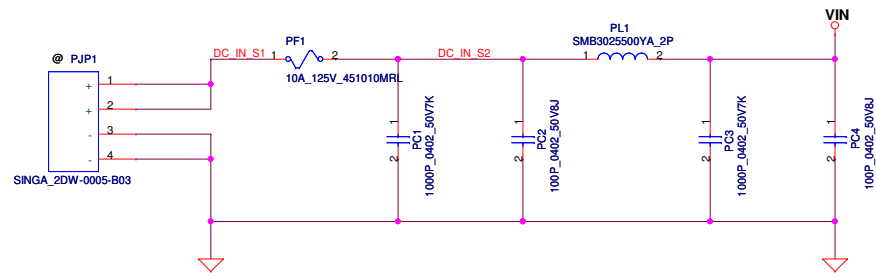
+5VS TO +5VS_ODD



For S3 CPU Power Saving



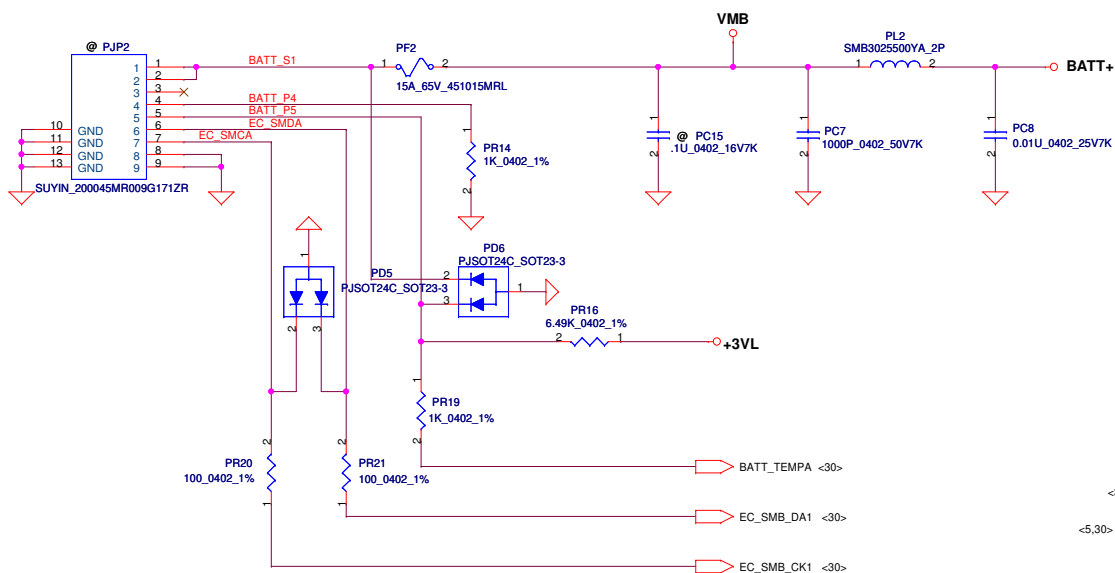
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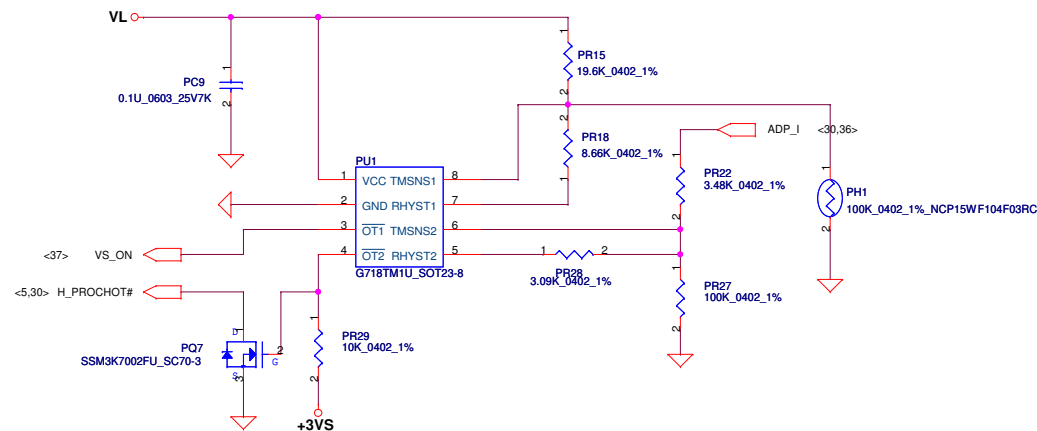
ACIN			
	Precharge detector		
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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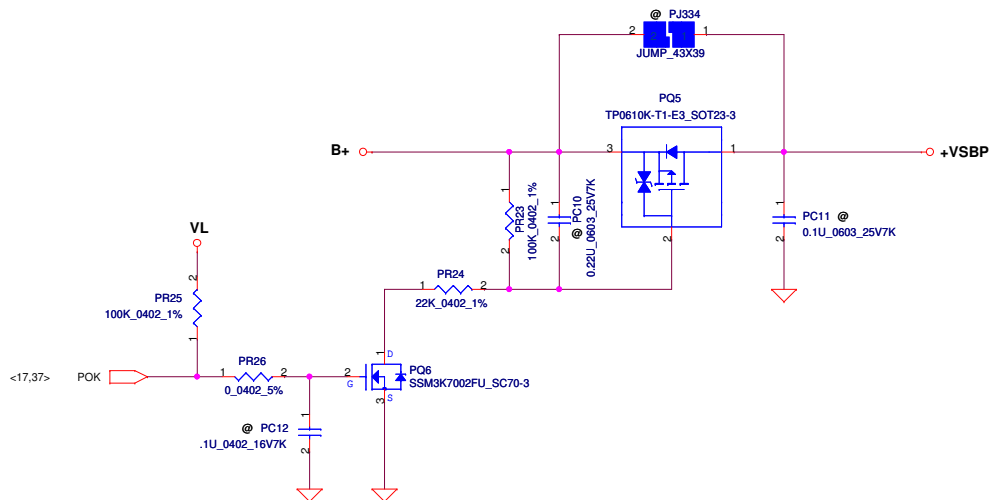
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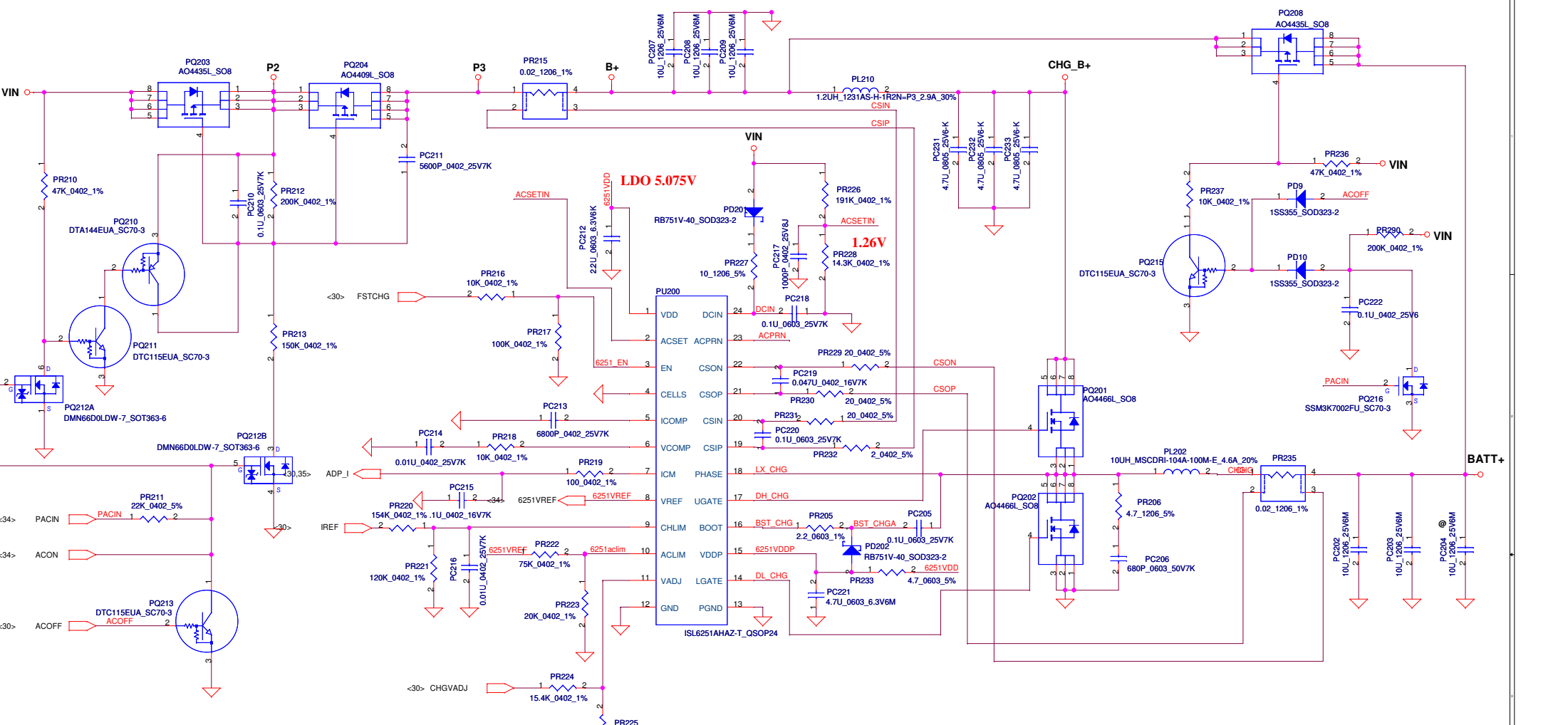


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V

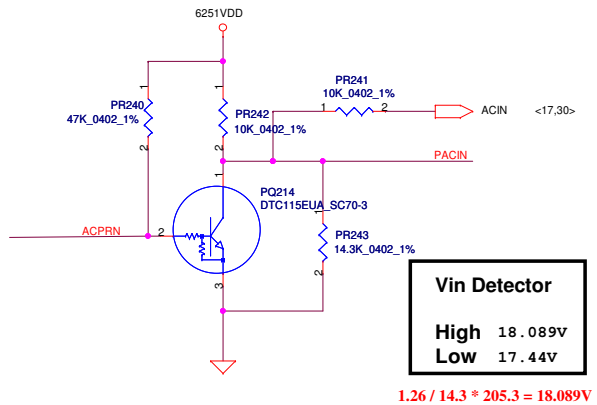




CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

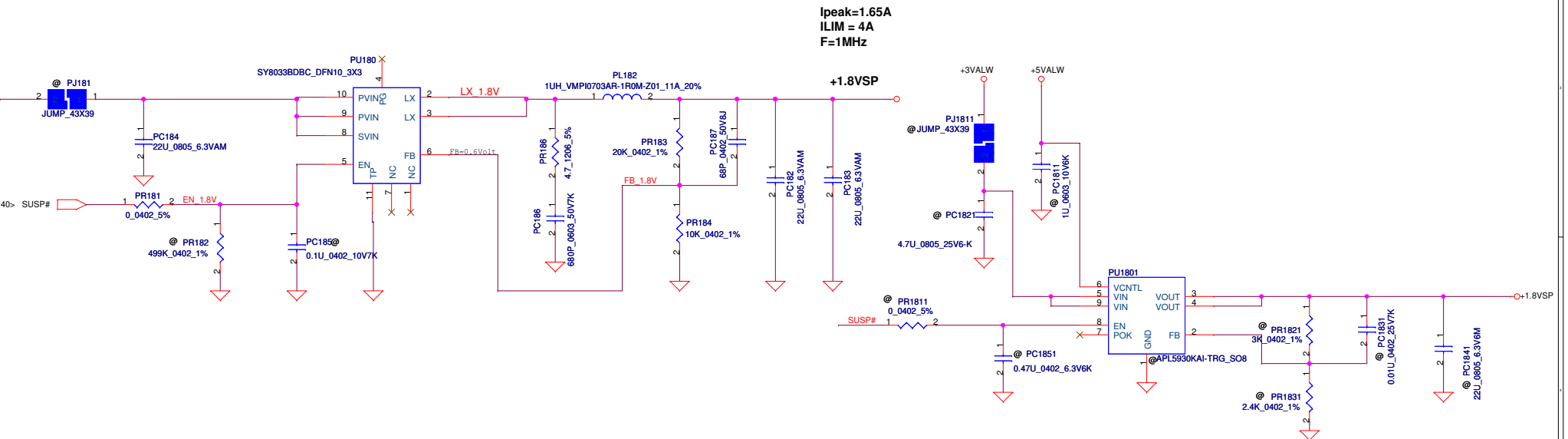
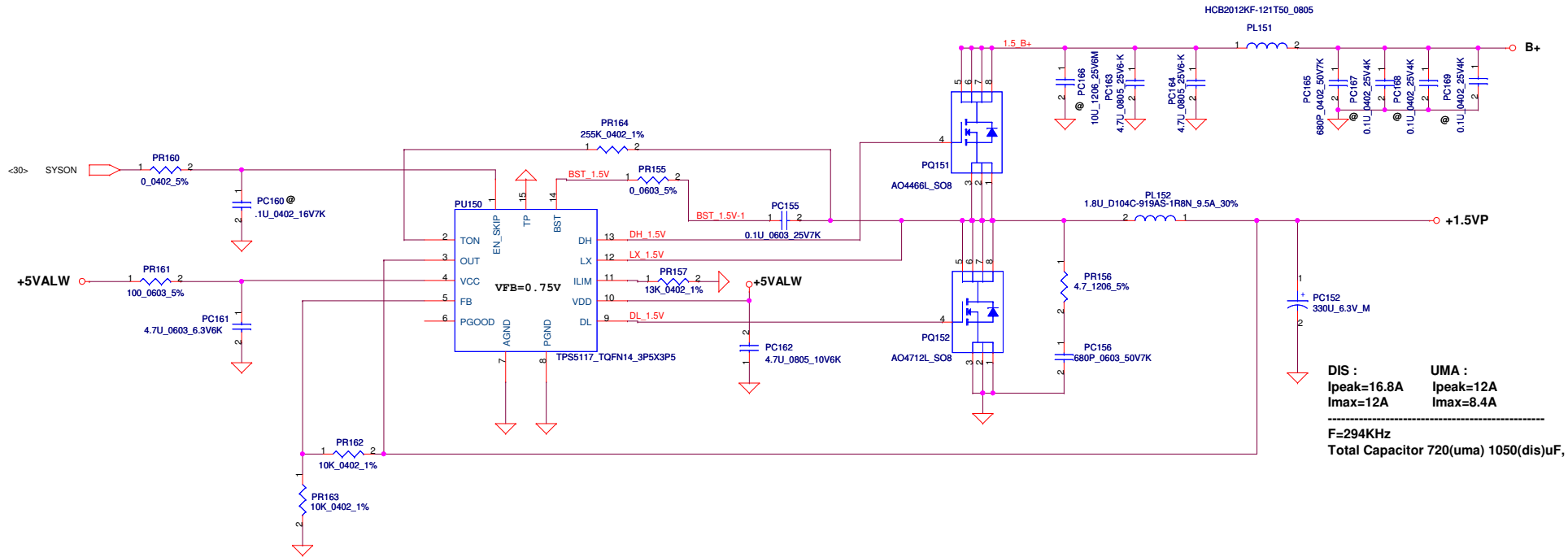
CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode	
Iada=0~3.42A (65W)	CP= 92%*Iada; CP=3.147A
VacLim=1.08V (65W)	PR222=75k PR223=20k PR215=0.02
Iada=0~3.947A (75W)	CP= 92%*Iada; CP=3.63A
VacLim=0.736V (75W)	PR222=24k PR223=20k PR215=0.02

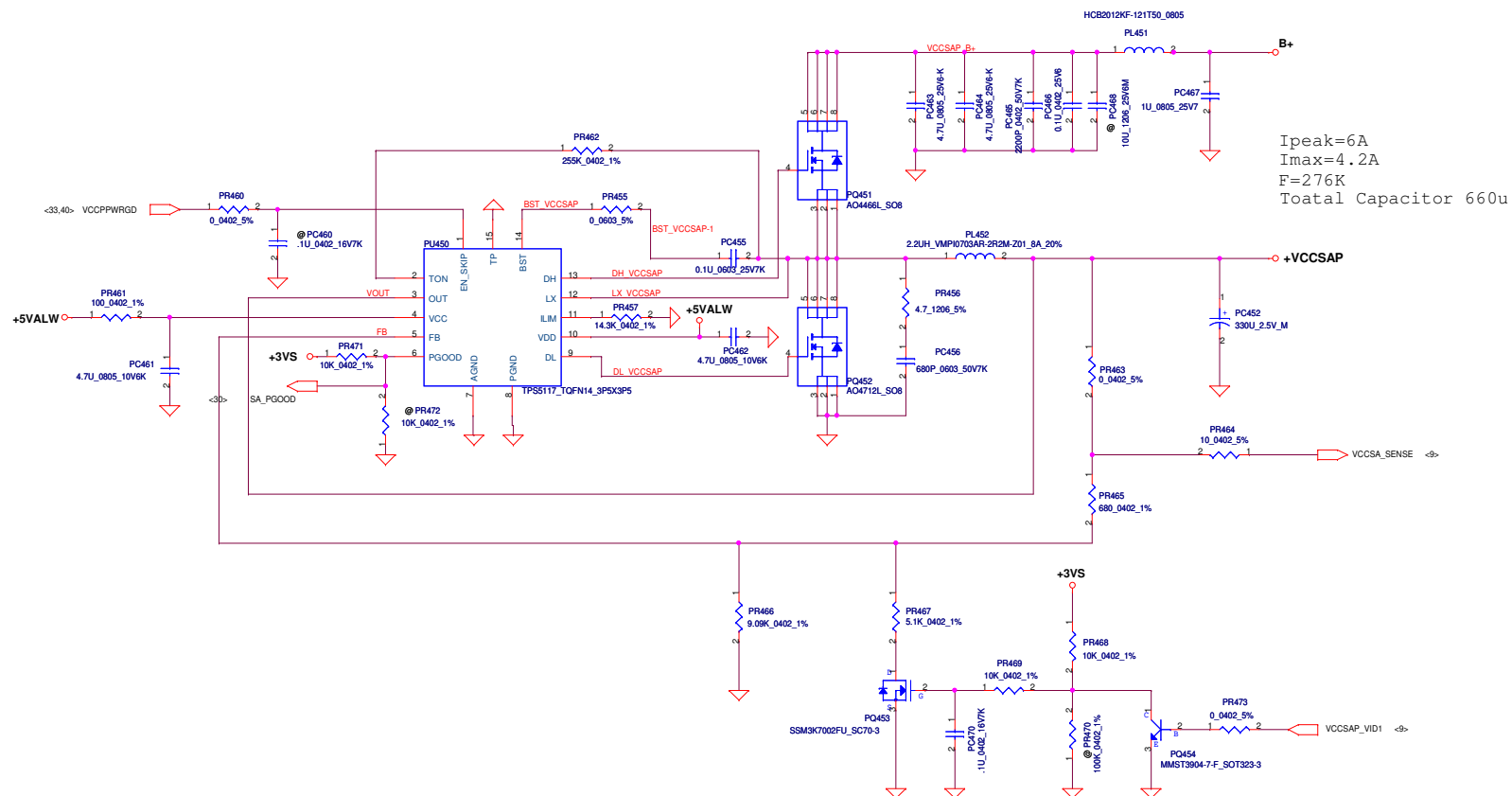


$1.26 / 14.3 * 205.3 = 18.089V$

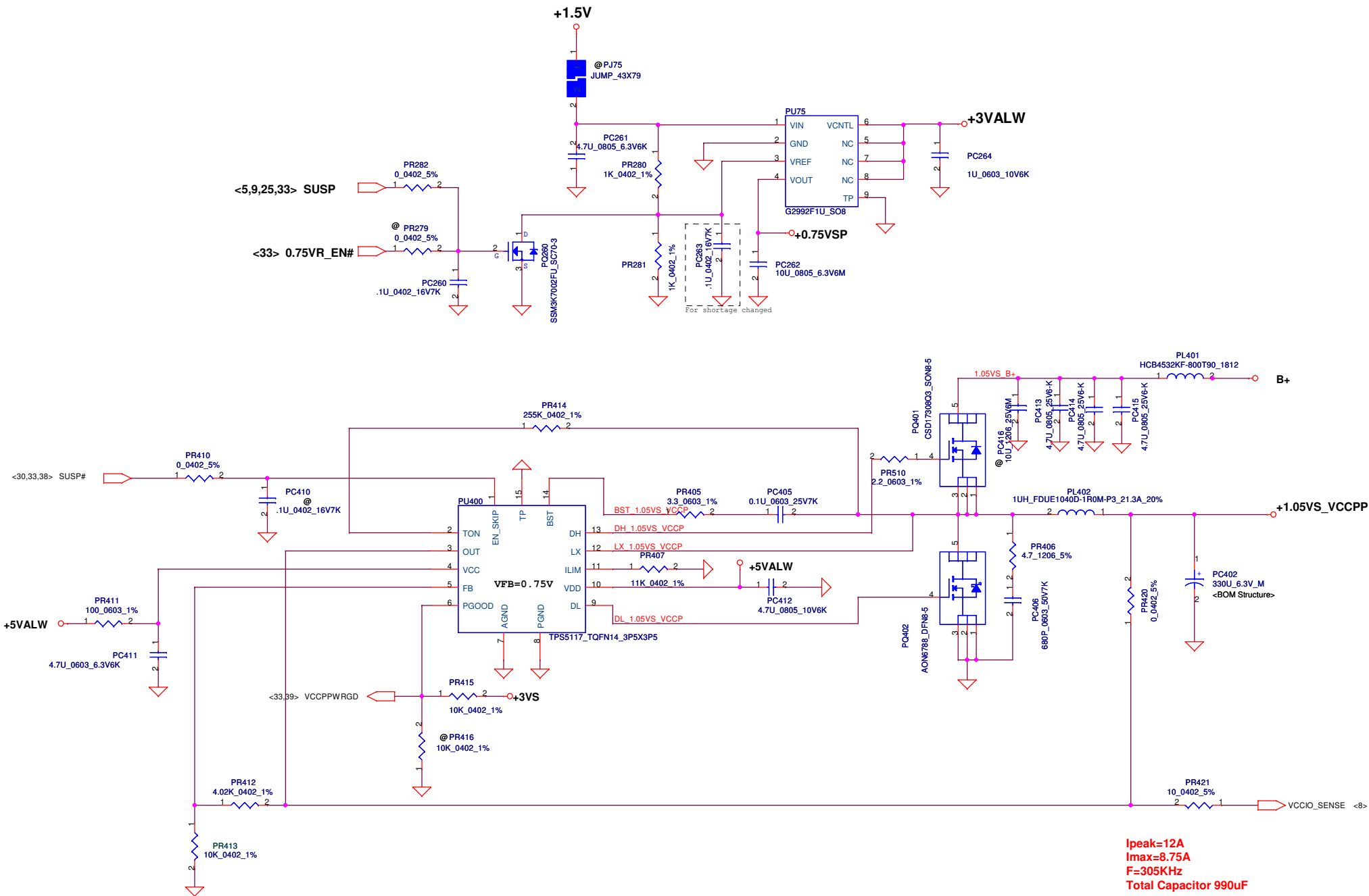
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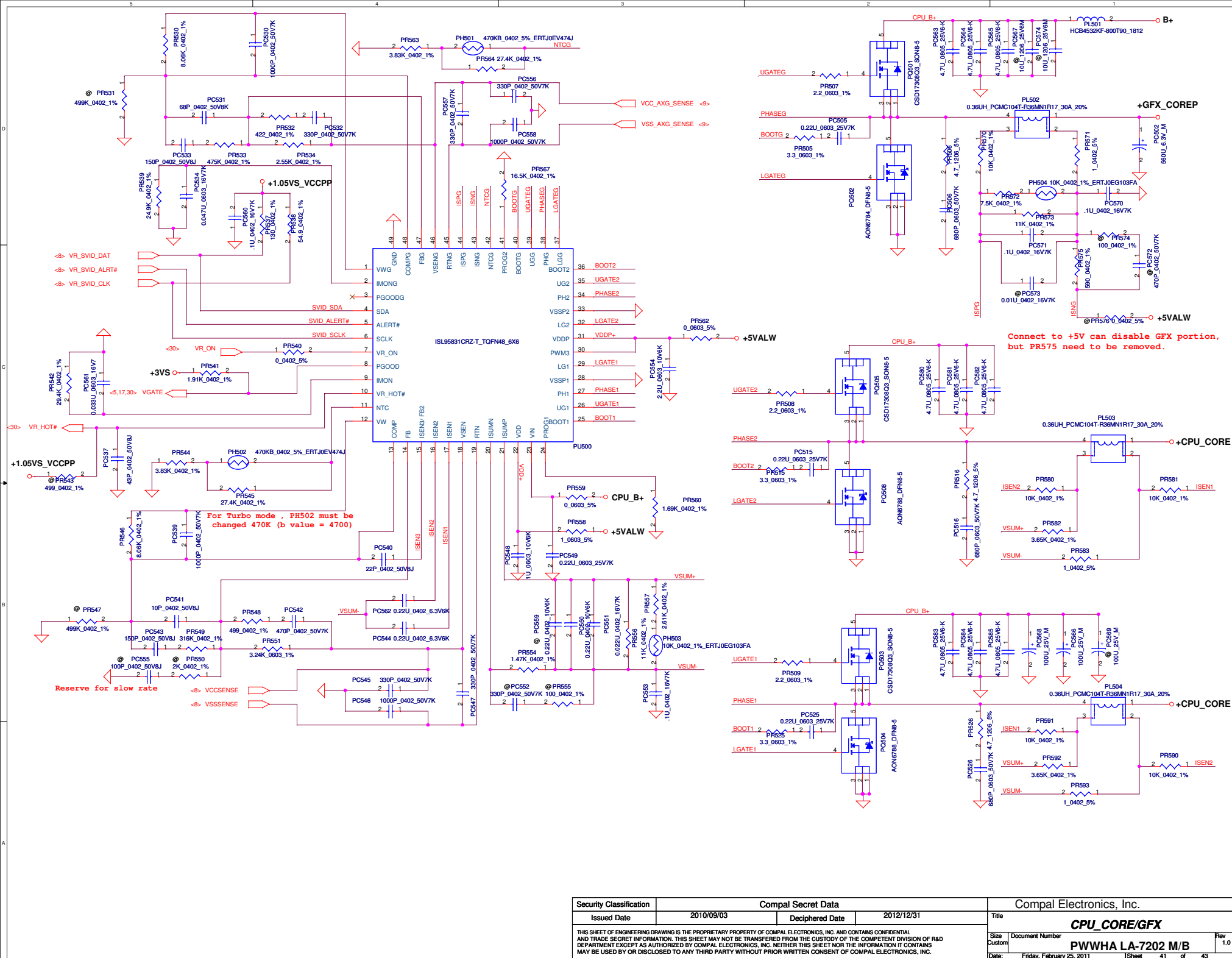
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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VID1	+VCCSAP
1	0.8V
0	0.9V



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PAGE	MODIFICATION LIST	PURPOSE
2010/12/31 (PVT) P36 Charger	Change PQ203,PQ208 to AO4435L	Cost down
2010/12/31 (PVT) P36 Charger	add PQ207,PQ208,PQ209 10u	EMI command
2010/12/31 (PVT) P36 Charger	add snubber PR206,PC206	EMI command
2010/12/31 (PVT) P36 Charger	change boost to 2.2 ohm PR205	EMI command
2010/12/31 (PVT) P35 +3VALW/+5VALW	add snubber PR336,PC336,PR356,PC336	EMI command
2010/12/31 (PVT) P37 +1.5VP/+1.8VSP	add snubber PR156,PC156	EMI command
2010/12/31 (PVT) P37 +1.5VP/+1.8VSP	add PC165 for MEI	EMI command
2010/12/31 (PVT) P37 +VCCSA	add snubber PR456,PC456	EMI command
2010/12/31 (PVT) P37 +VCCSA	change output capacitor PC452 to OS-con	cost down
2010/12/31 (PVT) P37 +VCCSA	change choke PL452 to molding	cost down
2010/12/31 (PVT) P38 +1.05VS/+0.75	add snubber PC406 PR406	EMI command
2010/12/31 (PVT) P38 +1.05VS/+0.75	change 0.75V enable PR279 tp PR282	HW command
2010/12/31 (PVT) P39 +CPU_CORE	change PC549,PC515,PC525,PC 505 to correct rating	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PL502,PL503,PL504 to DCR 5%	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PC568 PC 566 to 5.8mmm capacitor	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PL551 for load line adjust	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PR560 for program temperture	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PC502,PC531,PC532 for burn-in shun down	design change

Title <Title>		
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HW PIR (Product Improve Record)

PWWHA LA-7202P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0

GERBER-OUT DATE: 2011/02/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	01/24	05	modify FAN with BTO item PWM and RPM	For HW BTO item
2)	01/24	05	modify RPM FAN connector pin define	Request from thermal team
3)	02/14	30	co-lay KB9012	For BTO item
4)	02/15	24	Add C450	For ESD request

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