

## LCD Monitor Technical Training

### \* Model

; Analog input L chassis LCD monitor

- L1510SL
- L1710SL
- L1810SL
- L1910SL
- L1511SL
- L1515SL
- L1715SL
- L1516S
- L1716SL
- L1520BL
- L1720BL

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- 2) Analog Signal Input block**
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- 4) Scaler Block**
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### **2. LIPS block operation description**

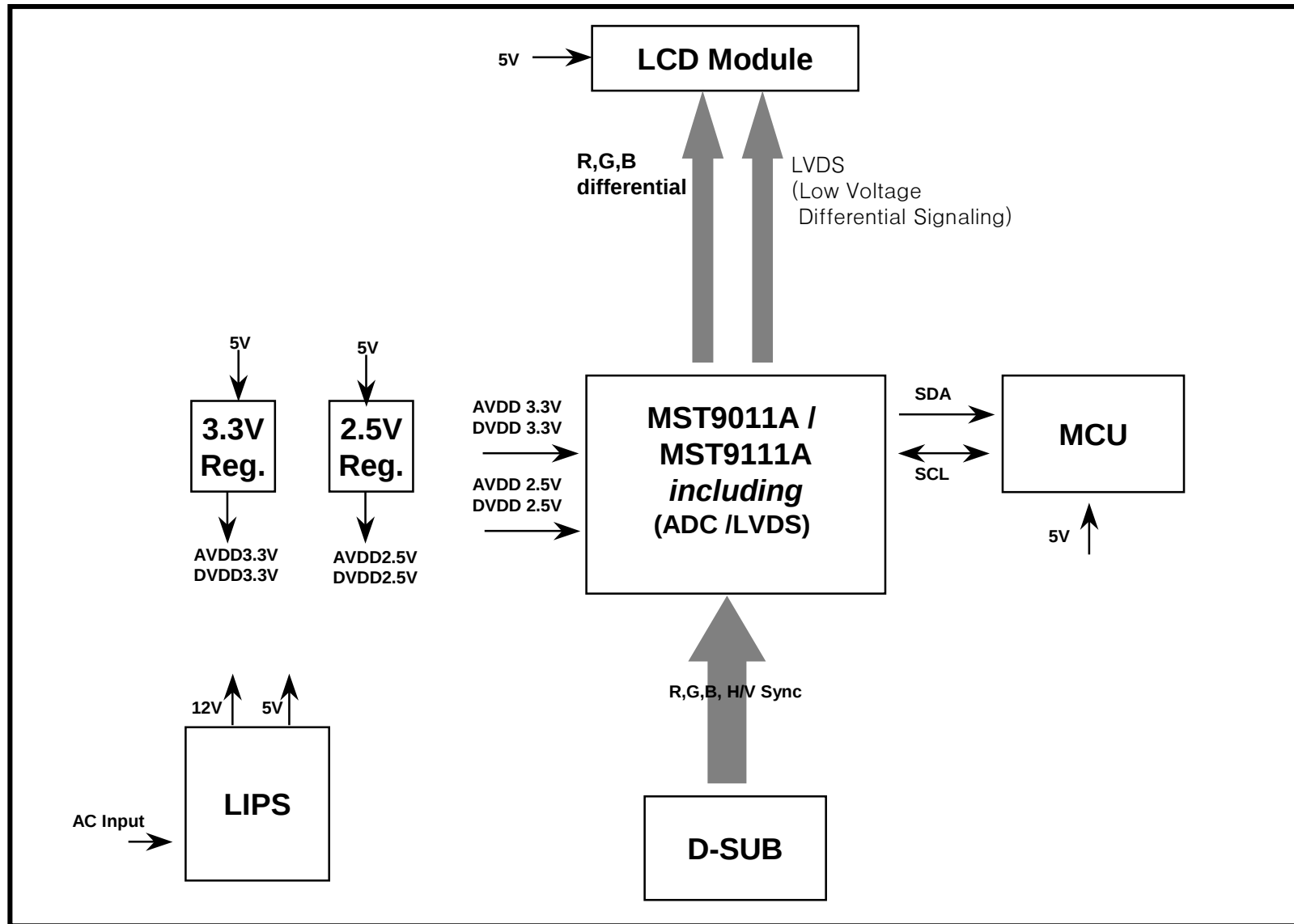
- 1) Block diagram**
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# 1. I/F Circuit operation Description

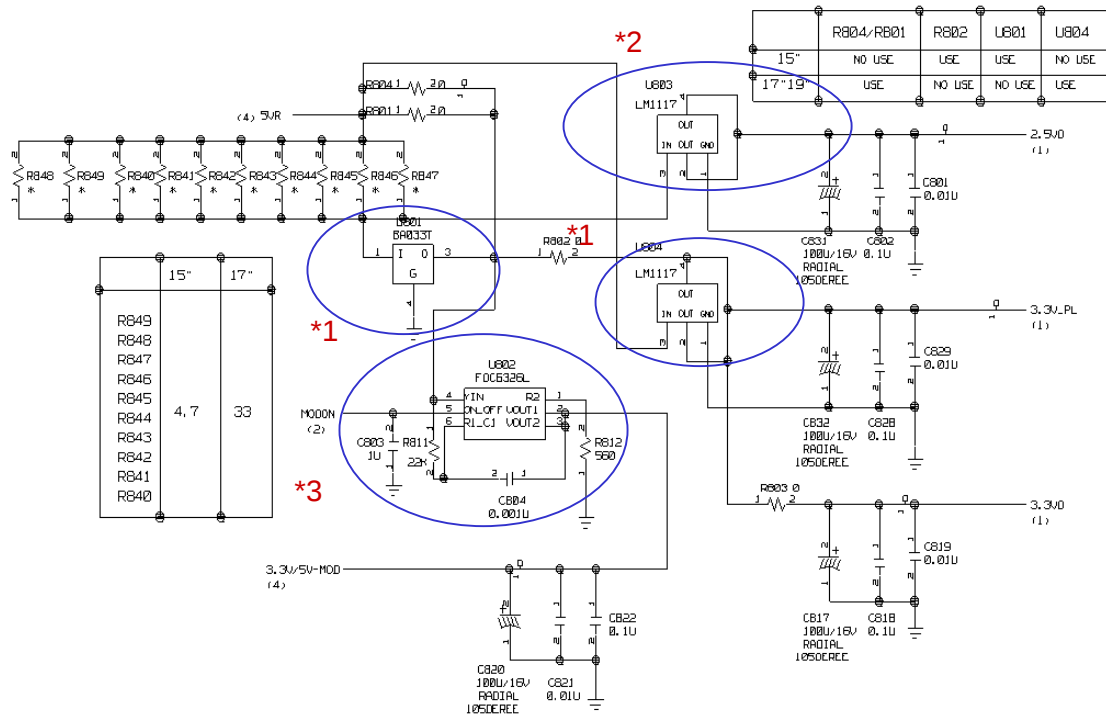
## 1.1. Block diagram





# 1. I/F Circuit operation Description

## 1.3. Supply Voltage regulation block



This is a supply voltage regulation block.

This block consist of 3.3V regulator, 2.5V regulator, panel Vcc voltage switching circuit.

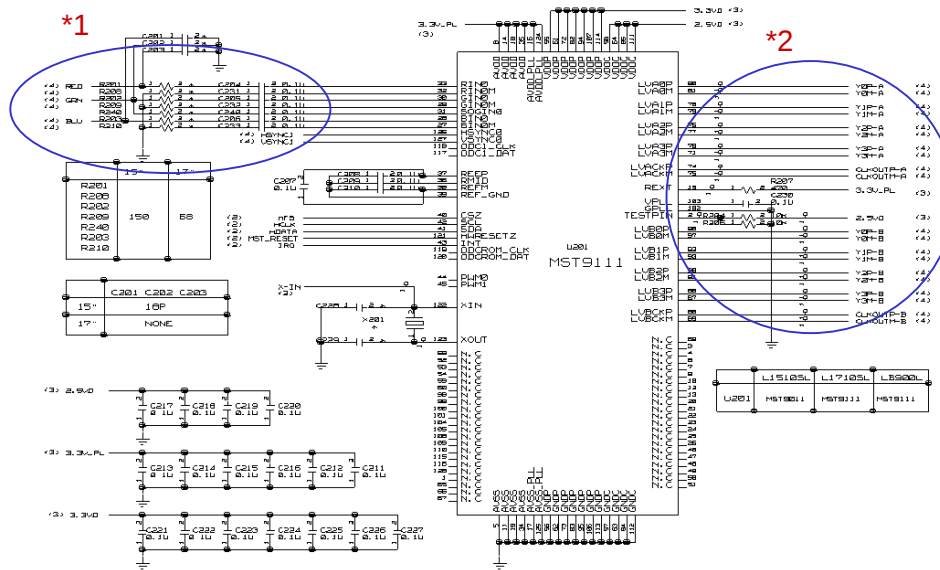
\*1) This is a voltage regulation circuit for 3.3V output.

\*2) This is a voltage regulation circuit for 2.5V output.

\*3) This is voltage FET switching circuit which is for panel Vcc power sequence.

# 1. I/F Circuit operation Description

## 1.4. Scaler block



### MST9011 (15" ), MST 9111(17",18",19")

1. Manufacturer : M star
2. Fully integrated ADC , PLL and scaler, LVDS,
3. Input sampling rate :
  - MST9011 : 85MHz
  - MST9111 : 135Mhz
4. Input Format :
  - MST9011 : Analog RGB up to XGA (1024 \* 768 @75Hz)
  - MST9111 : Analog RGB up to SXGA (1280 \* 1024 @75Hz)
5. Output Format : 8 or 6-bit panels  
One (15") or Two(17",19") pixel output format

\* Input and output signal

\*1) Analog Input block

- R,G,B input ,
- H-sync,V-sync,
- DDC line (D-SDA,D-SCL)

\*2) Output block

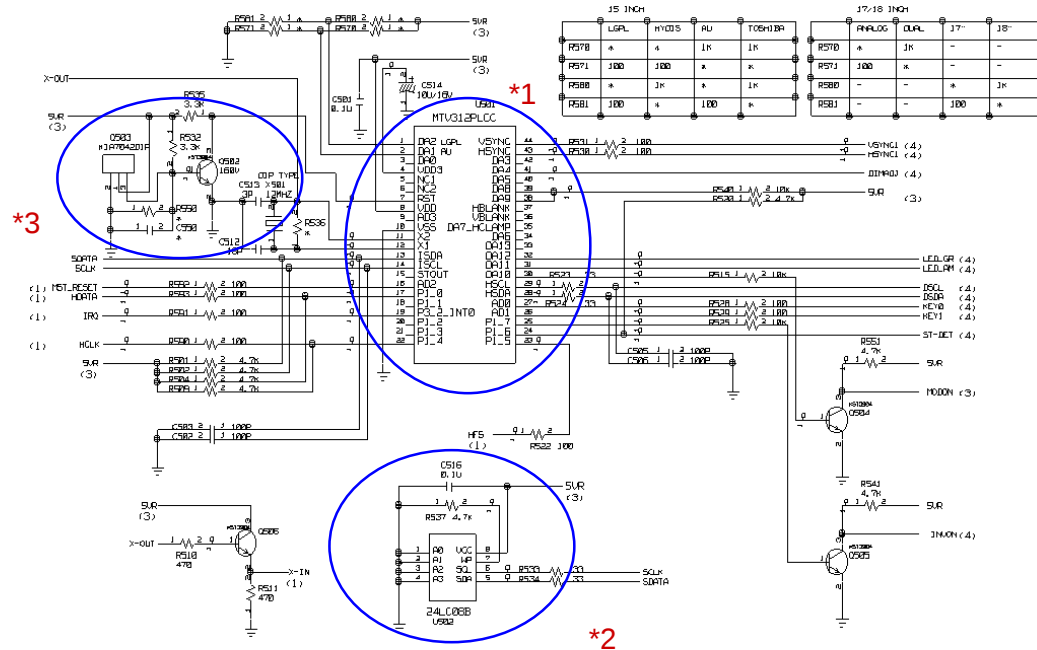
- LVDS output (5 channel) including Clock

This Scaler amplifies the level of video signal for the digital conversion and converts from the analog video signal to the digital video signal using a pixel clock and outputs 8-bit R, G, B signal to LVDS transmitter.

The range of the pixel clock is from 25MHz to 135MHz .

# 1.I/F Circuit operation Description

## 1.5. micro-controller block



This block consists of u-controller, EEPROM IC which stores control data, and Reset IC

### \*1) U-controller

The u-controller distinguishes polarity and frequency of the H/V sync which are supplied from signal cable. And u-controller control “Inverter on”, “LCD power on”, “Lamp current Adjust” and communication with scaler.

### \*2) EEPROM

The controlled data of each modes is stored in EEPROM.

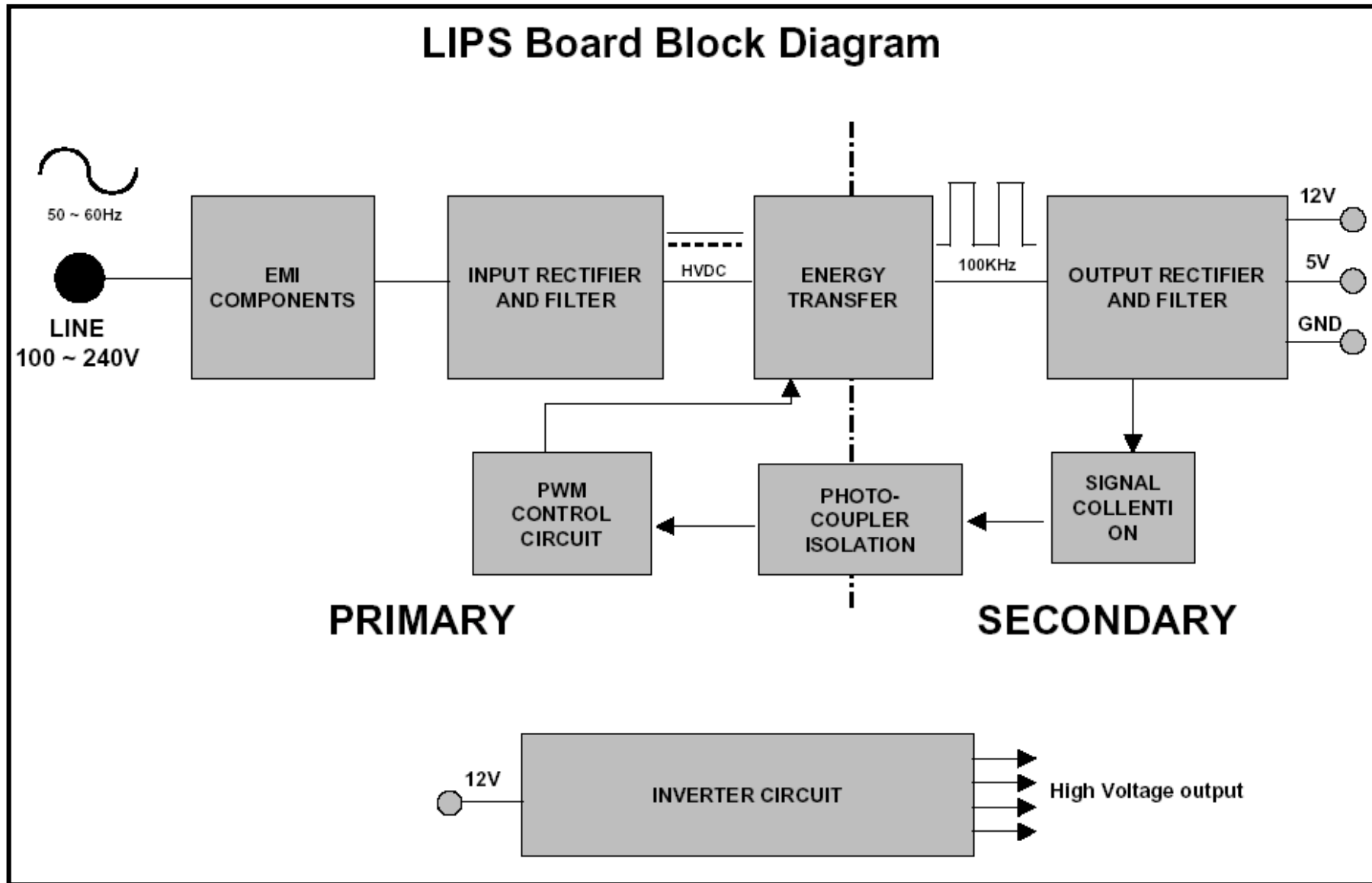
### \*3) Reset block

The reset of the u-controller is active “High”

KIA7042 reset IC's output is low until 5V come to be over 4.2V so that u-controller can have stable reset operation.

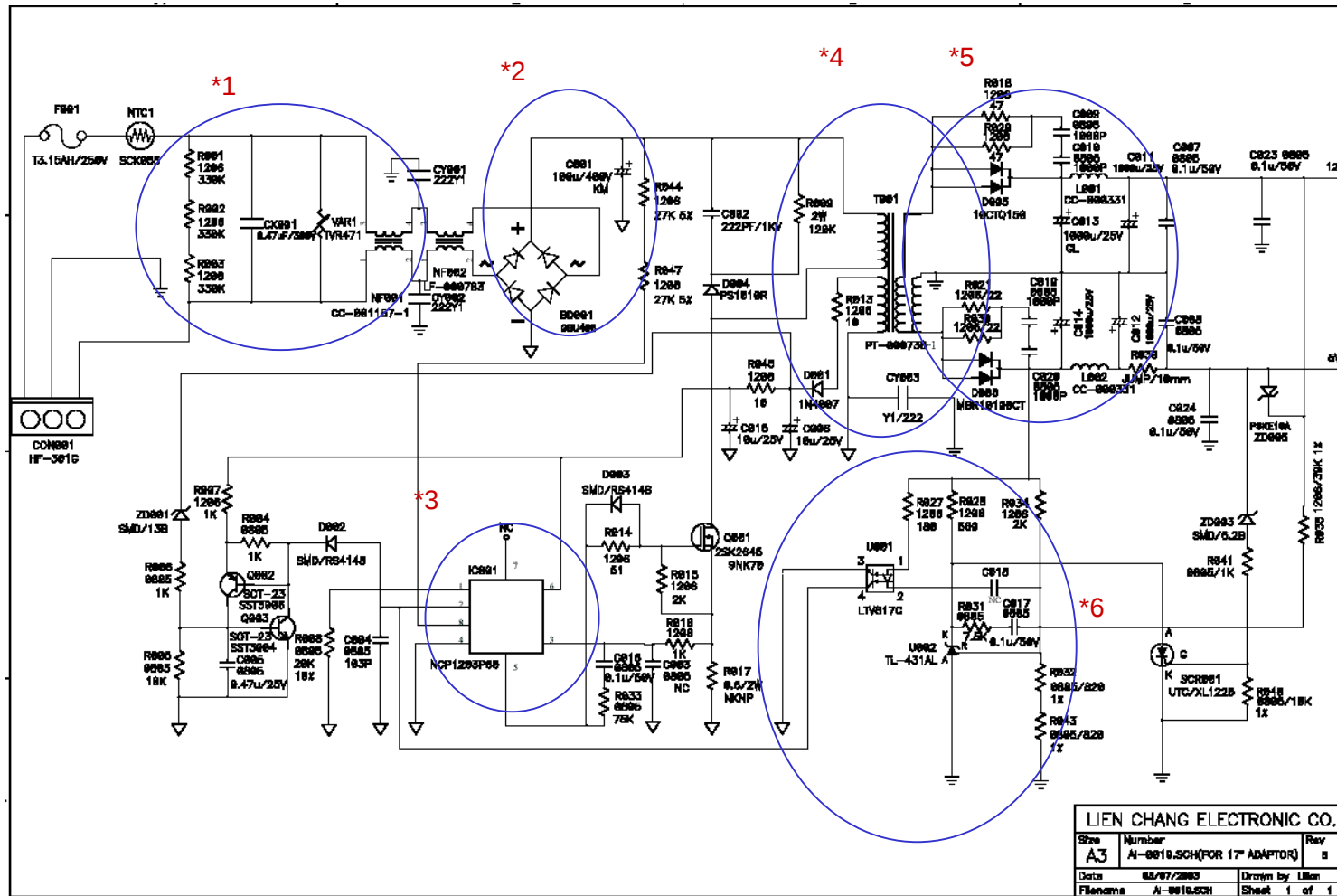
## 2. LIPS block operation description

### 2.1. Block diagram



## 2.LIPS block operation description

### 2.2. SMPS Block



## 2.LIPS block operation description

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### 2.2. SMPS Block

This block is SMPS block.

\*1) EMI component

This block construct Low pass filter for EMI reduction.

\*2) Input rectifier and smoothing filter

This block change AC input voltage to high DC voltage.

\*3) PWM control circuit

Control PWM oscillator frequency and drive switching MOSFET.

\*4) Energy transfer Transformer

Change high voltage on primary side to low voltage on secondary side and meet the output voltage spec.

\*5) Output rectifier and filter

- Through rectifier diode, get the DC voltage 12V,5V .
- Construct filter to get more approach DC voltage.

\*6) Feedback circuit

Construct feedback circuit to control U801 wavy duty.



## 2.LIPS block operation description

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### 2.3. Inverter Block

This block is Inverter block.

\*1) Reset circuit

This block is for voltage detecting. When input 5V is less than 5VDC, U106 KIA7042 will shut down U103(OZ960). U103 (OZ960) will be reset if the voltage is recovered 5VDC.

\*2) PWM controller

U103 (OZ960) is the PWM output controller to drive CCFL .

\*3) Drive network

Dual MOSFET for switch direct network to drive transformer.

\*4) Feedback and OVP circuit.

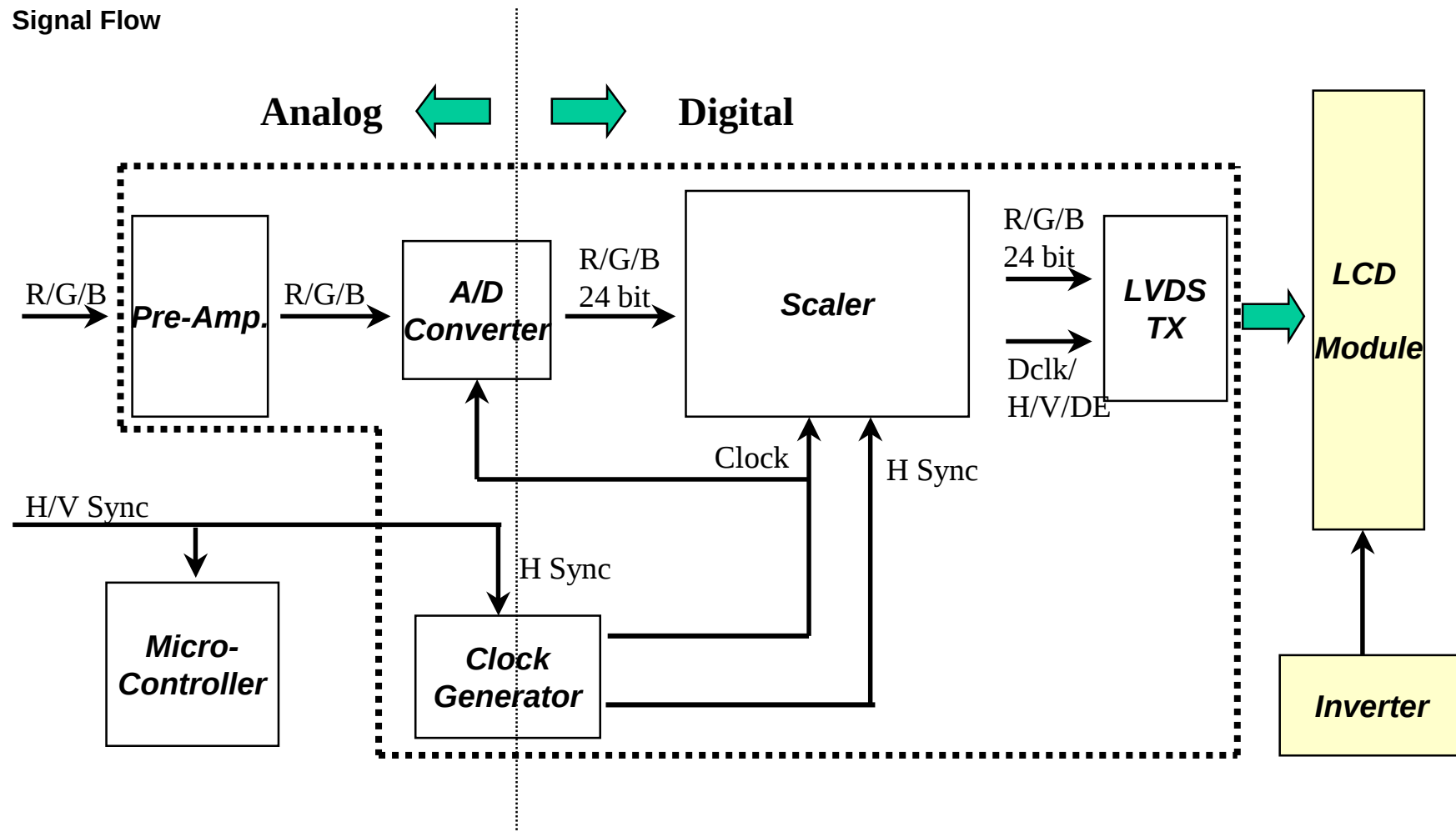
Detect kick off voltage from transformer and transfer this feedback voltage to pin 2 of U103.

If the feedback voltage is over 2V, U103 (OZ960) will be shut down.

### Operation principle of LCD Monitor

- 1) LCD Monitor Block diagram
- 2) Video signal Timing
- 3) Analog to Digital Converter
- 4) ADC Calibration
- 5) Pixel sampling
- 6) Output TTL Timing
- 7) LVDS
- 8) Power sequence for panel

Signal Flow



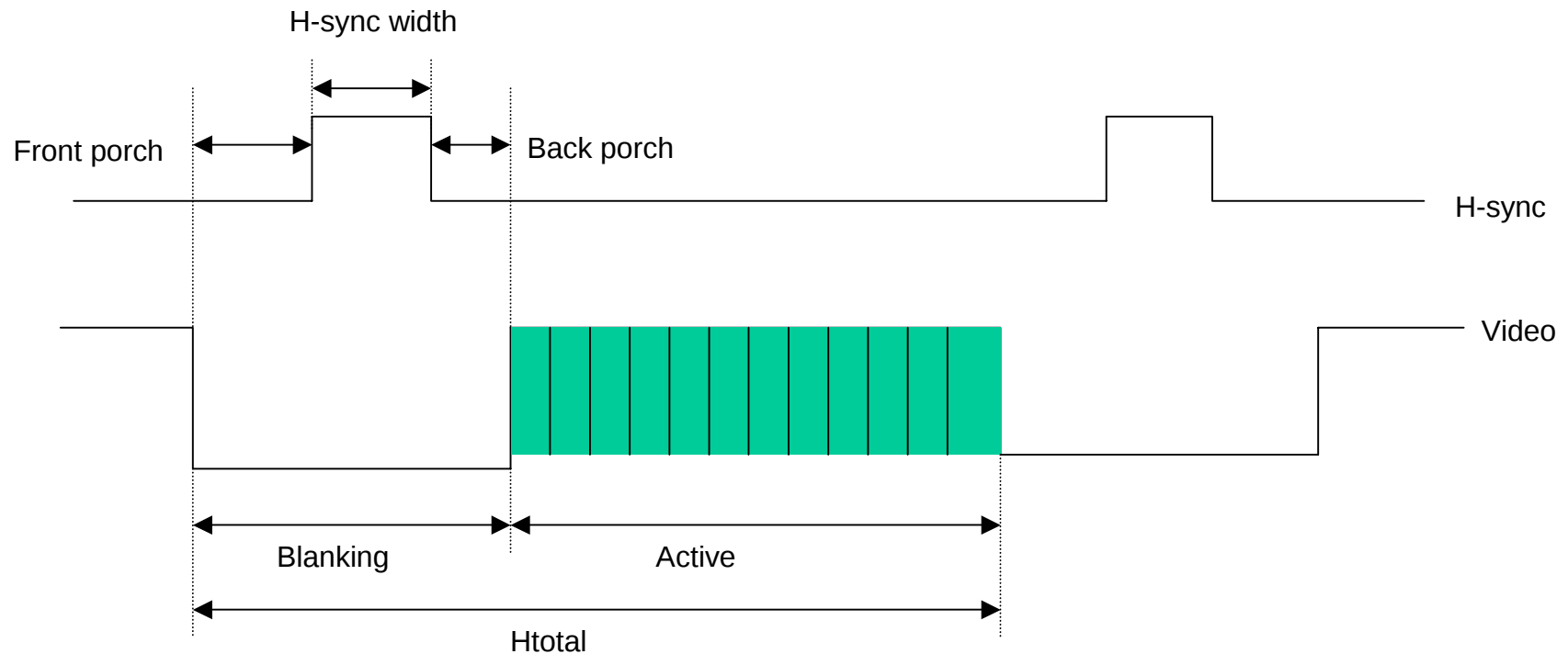
### 2.1. Timing formula

-  **$Dclk \text{ (Mhz)} = Htotal * Vtotal * Vsync(\text{Refresh Rate})$**

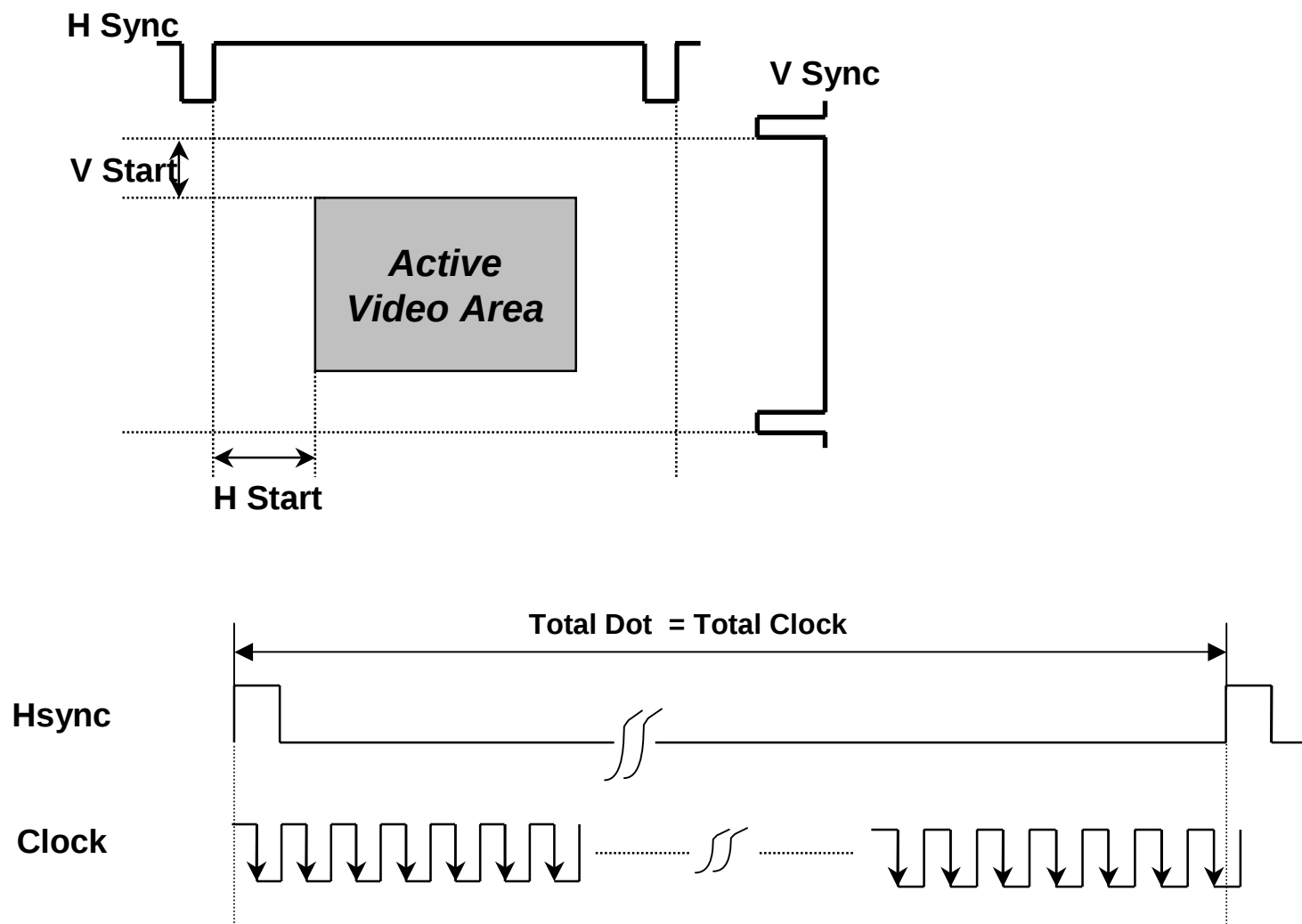
-  $Dclk = 1 / T_{pixel} = Htotal * Hsync$

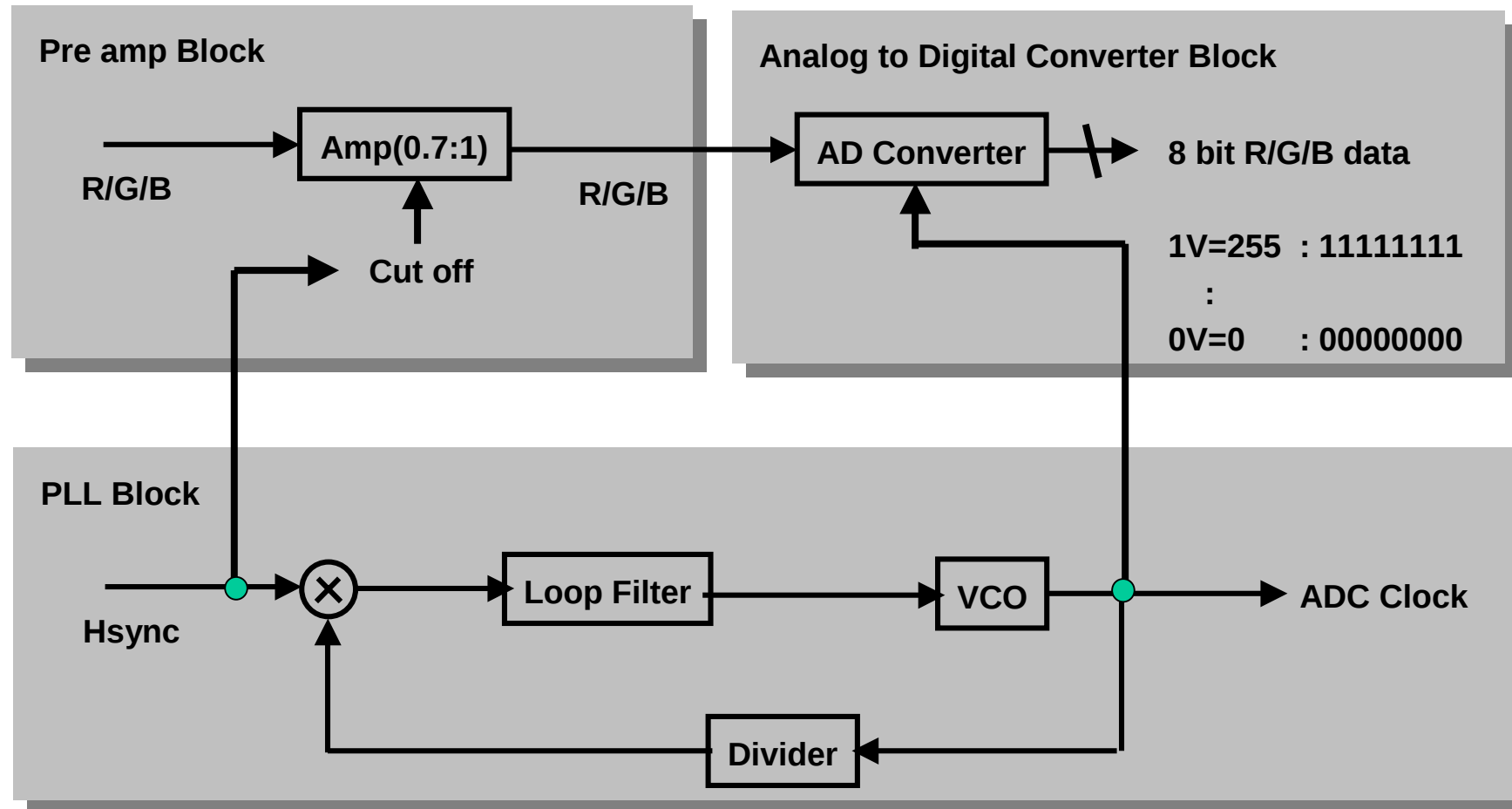
-  $Hsync = Vtotal * Vsync$

$Vsync = \text{Refresh Rate}$   
 $Hsync = \text{Horizontal Frequency}$   
 $Dclk = \text{Pixel clock}$



### 2.2. Timing configuration on Display





### 4.1. ADC Calibration Procedure

Each channel of the ADC must be calibrated before it can be used.

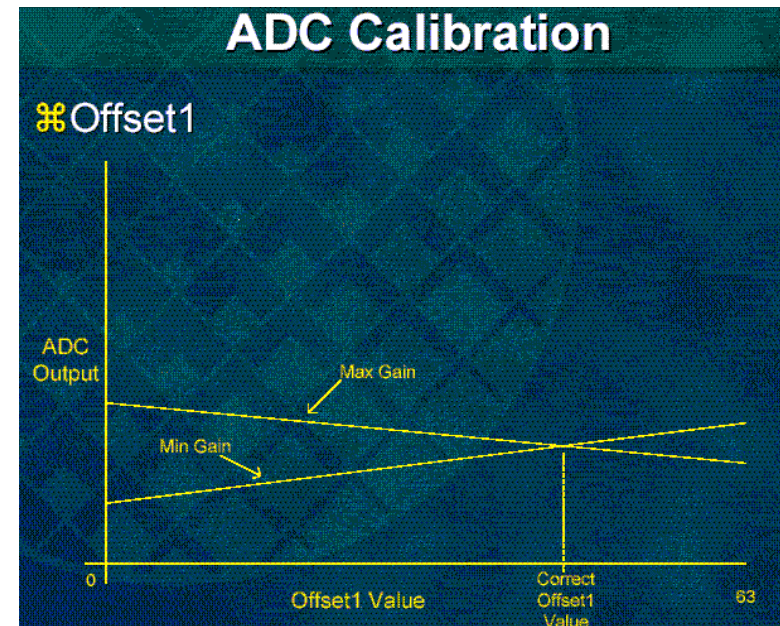
1. OFFSET1 is used to remove DC bias offsets in the ADC path.
2. OFFSET2 is used to trim the ADC to the black level characteristics of the RGB source.
3. GAIN is used to align the full scale voltage swing of the external source to the maximum input of the ADC.

OFFSET and GAIN calibration should be done with the real video source source, while capturing a full scale input.

Calibration is performed through firmware routines.

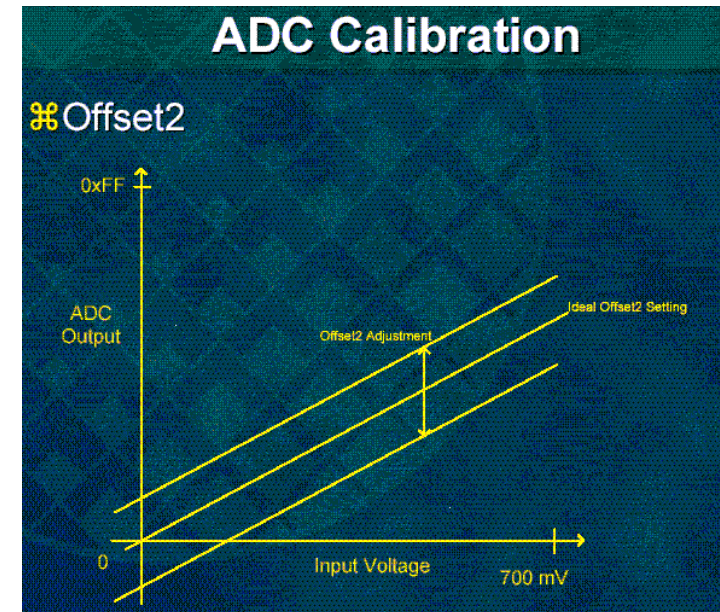
### 4.2. Offset1 Calibration

- \* Offset1
  - : Compensate for internal DC offset of the input stage of the on-chip track and Hold.
- \* To compensate the chip to chip variation .  
Therefore, the requirement is to perform only once (at Factory).
- Procedure is :
  - Set video input voltage for 0.0V.
  - set gain to minimum ; read ADC outputs
  - Set gain to maximum; read ADC outputs
  - Adjust offset 1 until ADC outputs at minimum and maximum are the same (within +/- tolerance)



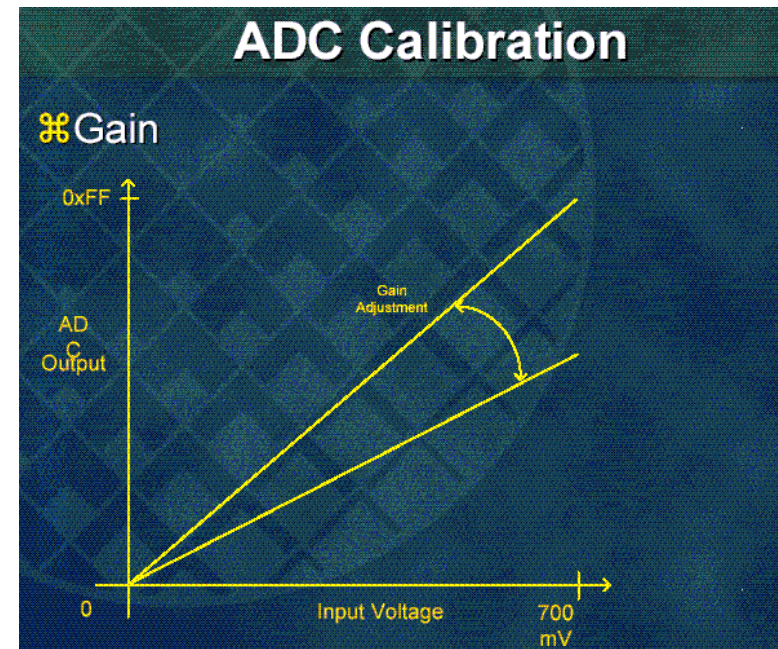
### 4.3. Offset2 Calibration

- \* Offset2
  - : Compensate for internal DC offset of the 2nd stage of the on-chip track and Hold.
- \* When used with offset1, make the overall ADC offset equal to zero and independent of the ADC gain setting.
- \* Ideally performed using actual analog input with full range values from graphics source.
- Procedure is :
  - Set video input voltage for 0.0V.
  - Decrease Offset2 to first instance where ADC underflow flags are set



### 4.4. Gain Calibration

- \* Gain
  - : Used to adjust full range input to produce full –swing ADC codes (from 00h to FFh)
- \* sometime, called auto color; auto white level; auto balance
- \* Require a full range input source to be performed correctly
- Procedure is :
  - Set video input voltage for 0.73V (or 0.7V for some model).
  - Increase gain to first instance where ADC 0verflow flags are set

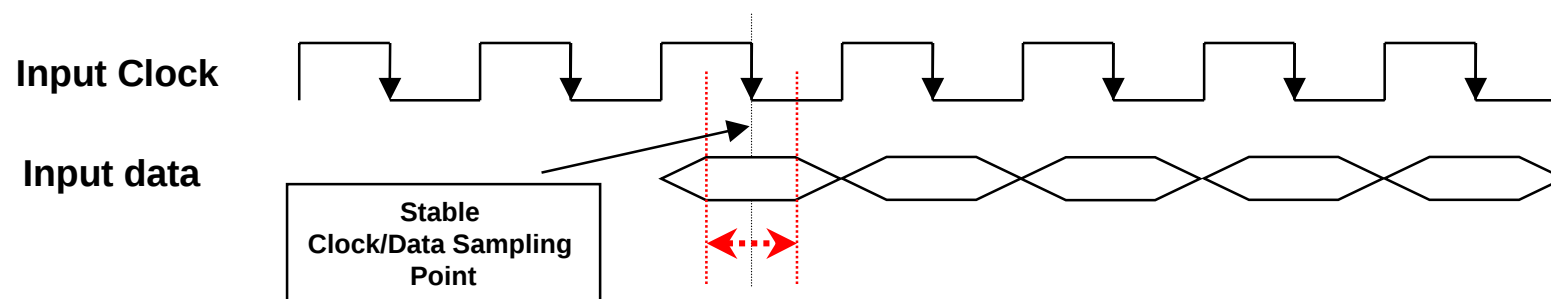
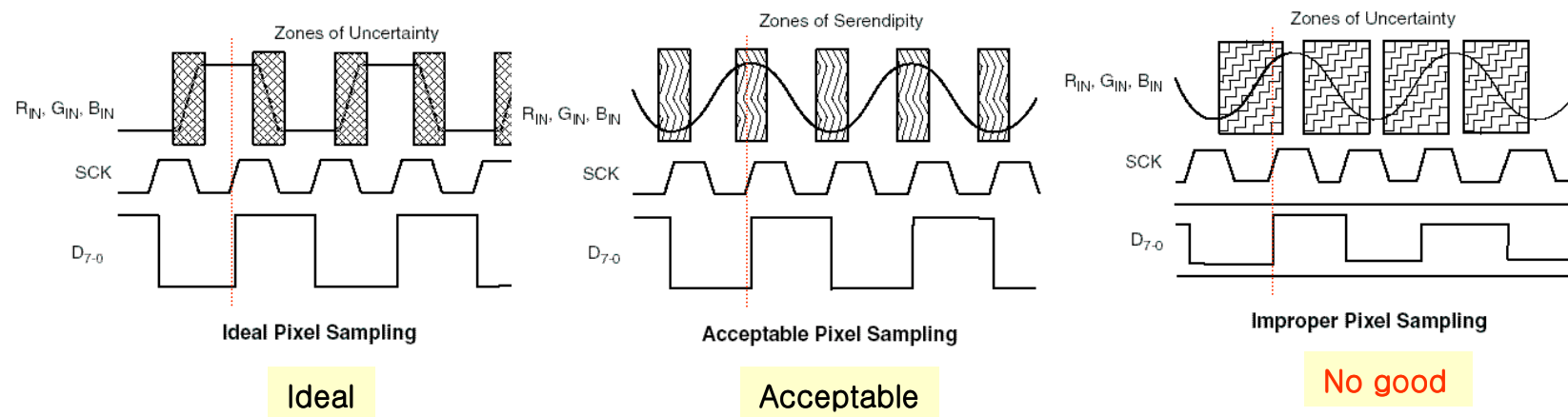


### 4.5. Effect of incorrect ADC calibration

- \* If ADC calibration is performed incorrectly, then following various artifacts might be happened.
  - Saturated “White”
    - ➔ different shades close to peak white value can’t be differentiated.
  - “Unblack” black
    - ➔ different shades of black close to black floor can’t be differentiated or black doesn’t black enough.
  - Reduced apparent contrast

## 5. Pixel sampling

### 5.1. Pixel sampling Point



### 5.2. How to find best pixel sampling point

- ★ Sum of pixel difference

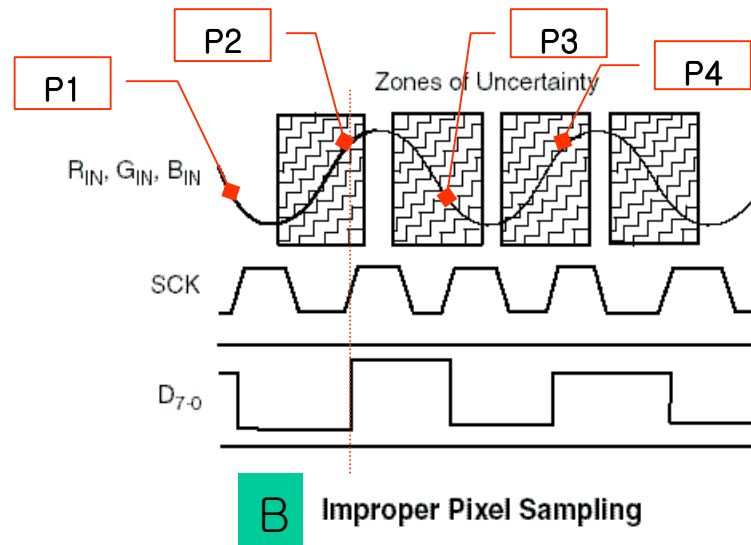
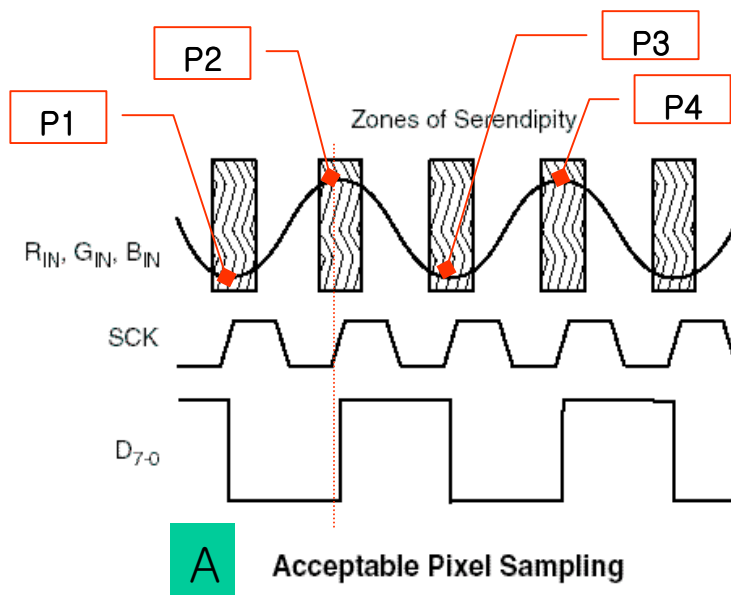
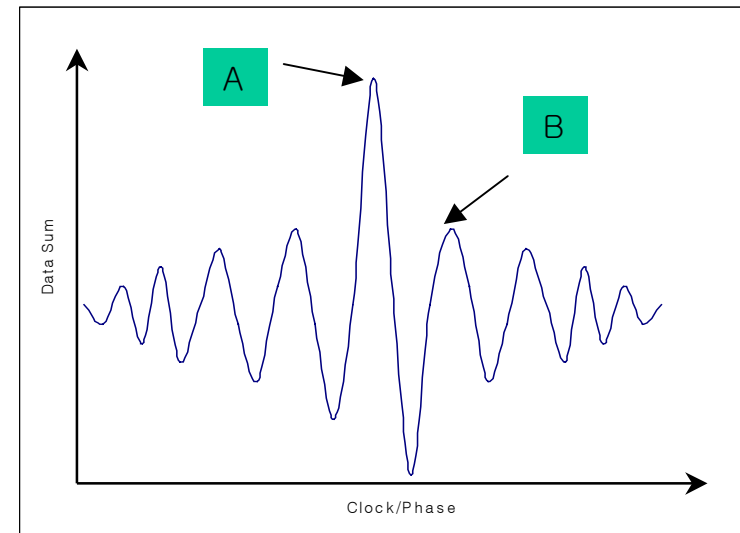
: For auto phase adjustment,

“sum of pixel difference” method is used.

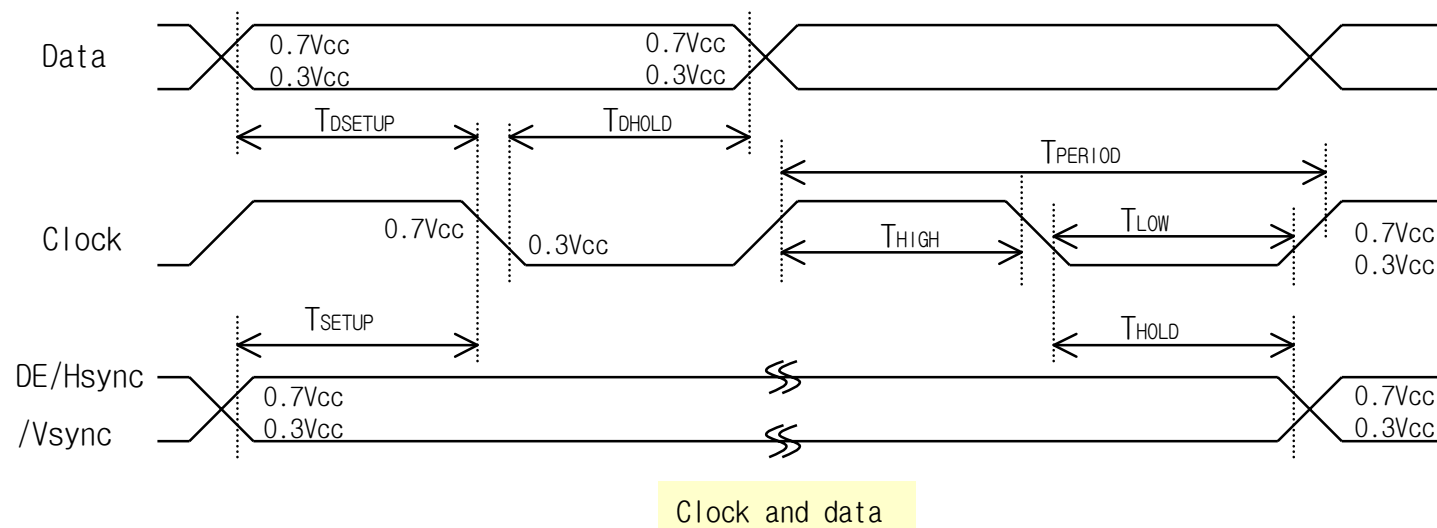
The pixel sum is highest at best phase point.

$$\text{PHASE} = \sum (P_N - P_{N-1})$$

- ★ To find best phase point is done by firmware routine.

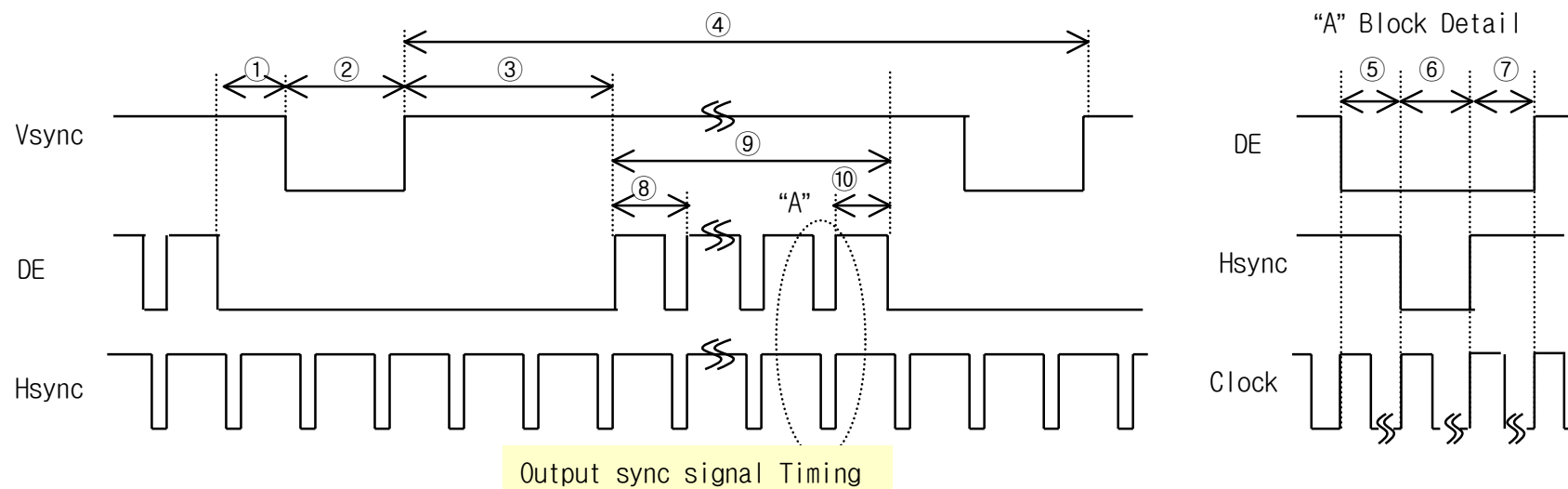


## (1) Detail timing description between Clock and Data (Falling Latch)



- ① Data Setup ( $T_{DSETUP}$ ) : Data setup time before Falling Edge of Clock.
- ② Data Hold ( $T_{DHOLD}$ ) : Data Hold up time after Falling Edge of Clock.
- ③ DE/Hsync/Vsync Setup ( $T_{SETUP}$ ) : DE/Hsync/Vsync setup time before Falling Edge of Clock.
- ④ DE/Hsync/Vsync Hold ( $T_{HOLD}$ ) : DE/Hsync/Vsync Hold up time after Falling Edge of Clock.

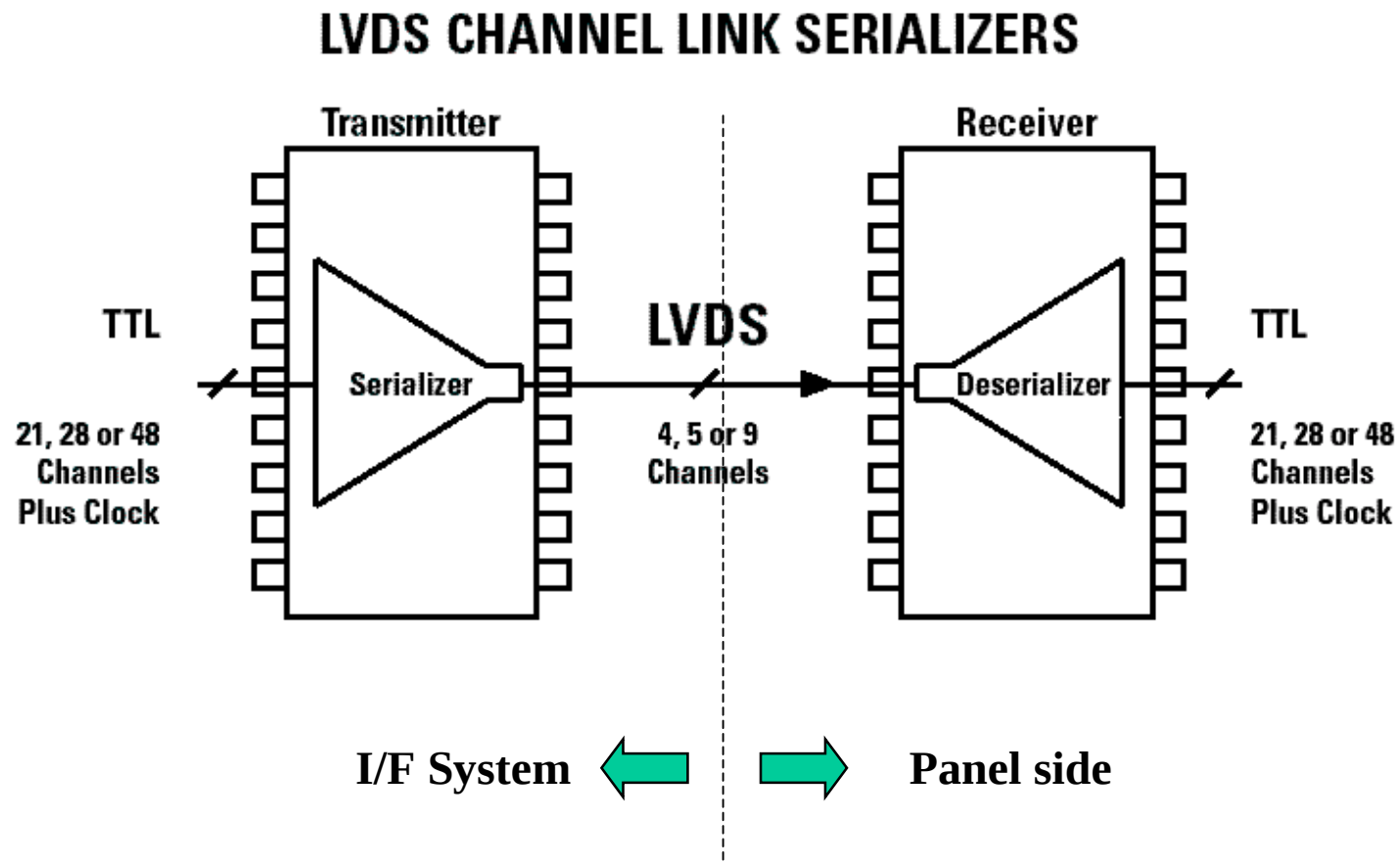
### (2) Output TTL Signal description (measured at Panel side)



- ① Vertical Front Porch
- ② Vertical Sync Width
- ③ Vertical Back Porch
- ④ Vertical Total : Active Line + Vertical Bank Porch + Vertical Front Porch
- ⑤ Horizontal Front Porch
- ⑥ Horizontal Sync Width
- ⑦ Horizontal Back Porch
- ⑧ Horizontal Total : Active Pixel + Horizontal Back Porch + Horizontal Front Porch
- ⑨ Active Line : Active Line Data
- ⑩ Active Data : Active Pixel Data

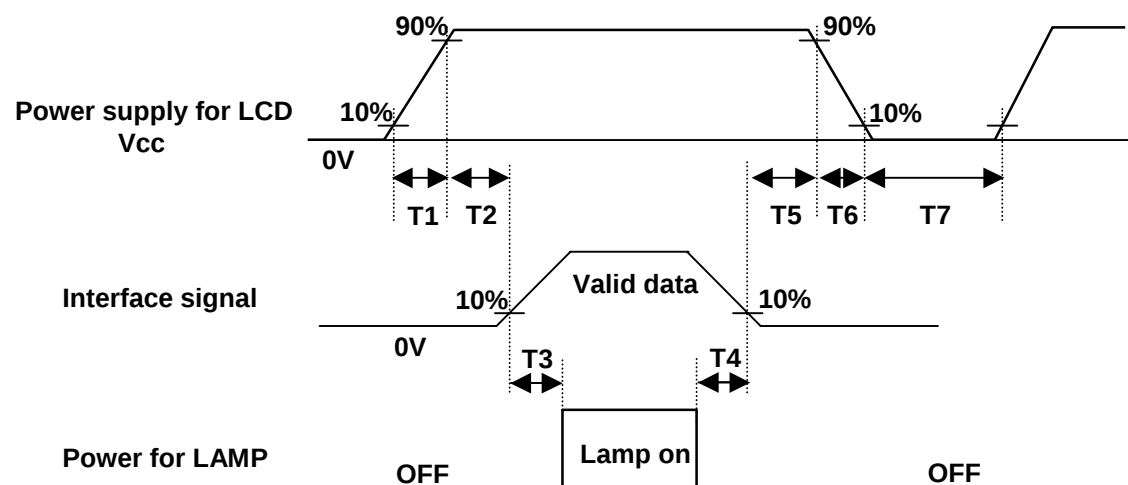
### 7.1.LVDS (Low voltage differential signaling)

; Convert TTL signal to Low voltage differential signal.



## 8. Power sequence for Panel

## Appendix



| Parameter | Values |      |      | Units |
|-----------|--------|------|------|-------|
|           | Min.   | Typ. | Max. |       |
| T 1       | —      | —    | 10   | ms    |
| T 2       | 0.01   | —    | 50   | ms    |
| T 3       | 200    | —    | —    | ms    |
| T 4       | 200    | —    | —    | ms    |
| T 5       | 0.01   | —    | 50   | ms    |
| T 6       | -      | —    | 10   | ms    |
| T 7       | 1      | —    | —    | s     |

- Notes :
1. Please avoid floating state of interface signal at invalid period.
  2. When the interface signal is invalid, be sure to pull down the power supply for LCD  $V_{CC}$  to 0V.  
Invalid signal with Vcc for a long period of time, causes permanent damage to LCD panel.
  3. Lamp power must be turn on after power supply for LCD and interface signals are valid.