

■ Terminal Function of ICs

• IC701 (AN8835SBE1) Servo Amplifier

Pin No.	Mark	I/O	Function
1	PDA	I	PD signal input
2	PDB	I	PD signal input
3	VCC	I	Power supply connection
4	LPD	I	Laser PD connection
5	LD	O	Power out for LD driving
6	RF	O	RF signal output
7	RFIN	I	RF signal input
8	CAGC	I	AGC loop filter connection
9	ARF	O	RF-AGC output
10	CSBRT	I	Capacitor for detection connection
11	CEA	I	Capacitor connection for HPF amplifier
12	BDO	O	BDO output ("H" : drop out)
13	LDON	I	LD APC input ("H" : ON, "L" : OFF)
14	GND	—	Ground connection

Pin No.	Mark	I/O	Function
15	/RFDET	O	NRFDET output ("L" : detection)
16	CROSS	O	CROSS output (Track cross signal output)
17	OFTR	O	Off-track output("L" : ON track, "H" : OFF track)
18	VDET	O	VDET output("H" : Vibration detected)
19	ENV	O	RF envelope detection
20	TEBPF	I	Vibration detection signal input
21	CCRS	I	Capacitor for LPF connection
22	TE	O	Tracking error signal output
23	FE	O	Focus error signal output
24	TBAL	I	Tracking balance signal input
25	FBAL	I	Focus balance signal input
26	VREF	O	Reference voltage output
27	PDE	I	PD signal input
28	PDF	I	PD signal input

• IC703 (AN8389SE1) Focus coil / Tracking coil / Traverse motor / Spindle motor driver

Pin No.	Mark	I/O	Function
1	VCC	I	Power supply terminal
2	VREF	I	Reference voltage input
3	IN4	I	Motor driver (4) input
4	IN3	I	Motor driver (3) input
5	GND	—	Ground connection
6	NC	—	Ground connection
7	NRESET	I	Reset input
8	GND	—	Ground connection
9	IN2	I	Motor driver (2) input
10	PC2	I	PC2 (power cut) input
11	IN1	I	Motor driver (1) input
12	PC1	I	PC1 (power cut) input (Not used, open)

Pin No.	Mark	I/O	Function
13	PVCC1	I	Power supply (1) for driver
14	PGND1	—	Ground connection (1) for driver
15	D1—	O	Motor driver (1) reverse-action output
16	D1+	O	Motor driver (1) forward-action output
17	D2—	O	Motor driver (2) reverse-action output
18	D2+	O	Motor driver (2) forward-action output
19	D3—	O	Motor driver (3) reverse-action output
20	D3+	O	Motor driver (3) forward-action output
21	D4—	O	Motor driver (4) reverse-action output
22	D4+	O	Motor driver (4) forward-action output
23	PGND2	—	Ground connection (2) for driver
24	PVCC2	I	Power supply (2) for driver

• IC702 (MN662741RPA) Servo processor / Digital signal processor / Digital filter / D/A converter

Pin No.	Mark	I/O	Function
1	BCLK	O	Serial bit clock terminal (Not used, open)
2	LRCK	O	L/R discriminating signal (Not used, open)
3	SRDATA	O	Serial data (Not used, open)
4	DVDD1	I	Power supply (digital circuit) terminal
5	DVSS1	—	GND (digital circuit) terminal
6	TX	O	Digital audio interface signal
7	MCLK	I	Microprocessor command clock signal
8	MDATA	I	Microprocessor command data signal
9	MLD	I	Microprocessor command load signal
10	SENSE	O	Sense signal output (OFT, FESL, MAGEND, NAJEND, POSAD, SFG)
11	/FLOCK	O	Optical servo condition (focus) ("L" : lead-in)
12	/TLOCK	O	Optical servo condition (tracking) ("L" : lead-in)
13	BLKCK	O	Sub-code block clock (f=75Hz)
14	SQCK	I	External clock signal input for sub-code Q register.
15	SUBQ	O	Sub-code Q code output
16	DMUTE	I	Muting input ("H" : mute)
17	STAT	O	Status signal output (CRC, CUE, CLVS, TTSTVP, FCLV, SQCK)
18	/RST	I	Reset input
19	SMCK	O	1/2-divided clock signal of crystal oscillating at MSEL = "H" (fSMCK=8.4672MHz) 1/4-divided clock signal of crystal oscillating at MSEL = "L" (fSMCK=4.2336MHz)
20	PMCK	O	1/192-divided clock signal of crystal oscillating (fPMCK=88.2kHz) (Not used, open)
21	TRV	O	Traverse servo control output
22	TVD	O	Traverse drive signal output
23	PC	O	Spindle motor ON signal output ("L" : ON)
24	ECM	O	Spindle motor drive signal output (forced mode output)
25	ECS	O	Spindle motor drive signal output (servo error signal output)
26	KICK	O	Kick pulse output
27	TRD	O	Tracking drive output
28	FOD	O	Focus drive output
29	VREF	I	D/A (drive) output (TVD, ECS, TRD, FOD, FBAL, TBAL) Reference voltage input.
30	FBAL	O	Focus balance adjustment output (Not used, open)
31	TBAL	O	Tracking balance adjustment output
32	FE	I	Focus error signal input (analog input)
33	TE	I	Tracking error signal input (analog input)
34	RFENV	I	RF envelope signal input
35	VDET	I	Vibration detection signal input ("H" : detection)

Pin No.	Mark	I/O	Function
36	OFT	I	Off-track signal input ("H" : off track)
37	TRCRS	I	Track cross signal input
38	/RFDET	I	RF detection signal input ("L" : detection)
39	BDO	I	Dropout signal input ("H" : Dropout)
40	LDON	O	Laser on signal output ("H" : ON)
41	TES	O	Tracking error shunt signal output ("H" : shunt)
42	PLAY	O	Play signal out ("H" : PLAY)
43	WVEL	O	Double speed status signal output ("H" : DS)
44	ARF	I	RF signal input
45	IREF	I	Reference current input
46	DRF	I	DSL bias (Not used, open)
47	DSLIF	I/O	DSL loop filter
48	PLLIF	I/O	PLL loop filter
49	VCOF	I/O	VCO loop filter (Not used, open)
50	AVDD2	I	Power supply input (for analog circuit)
51	AVSS2	—	GND (for analog circuit)
52	EFM	O	EFM signal output (Not used, open)
53	PCK	O	PLL extraction clock output (Not used, open) (fPCK=4.321 MHz during normal playback)
54	PDO	O	Phase comparison signal of EFM and PCK signals (Not used, open)
55	SUBC	O	Sub-code serial data output (Not used, open)
56	SBCK	I	Sub-code frame clock signal output (fCLDCK=7.35kHz during normal playback)
57	VSS	—	GND
58	X1	I	Crystal oscillating circuit input (f=16.9344MHz)
59	X2	O	Crystal oscillating circuit output (f=16.9344MHz)
60	VDD	I	Power supply input (for oscillating circuit)
61	BYTCK	O	Byte clock output (Not used, open)
62	/CLDCK	O	Clock input for sub-code serial data (Not used, open)
63	FCLK	O	Crystal frame clock signal output (fCLK=7.35kHz, double=14.7kHz)
64	PFLAG	O	Interpolation flag output ("H" : interpolation) (Not used, open)
65	FLAG	O	Flag output (Not used, open)
66	CLVS	O	Spindle servo phase synchronizing signal output ("H" : CLV, "L" : rough servo) (Not used, open)
67	CRC	O	Sub-code CRC checked output ("H" : OK, "L" : NG) (Not used, open)
68	DEMPH	O	De-emphasis ON signal output ("H" : ON) (Not used, open)
69	RESY	O	Frame resynchronizing signal output (Not used, open)
70	/RST2	I	Reset input through MASH circuit ("L" : Reset)
71	/TEST	I	Test input

Pin No.	Mark	I/O	Function
72	AVDD1	I	Power supply input (for analog circuit)
73	OUTL	O	Left channel audio signal output
74	AVSS1	—	GND
75	OUTR	O	Right channel audio signal output
76	RSEL	I	RF signal polarity assignment input (at "H" level, RSEL="H", at "L" level, RSEL="L")
77	CSEL	I	Crystal oscillating frequency designation input

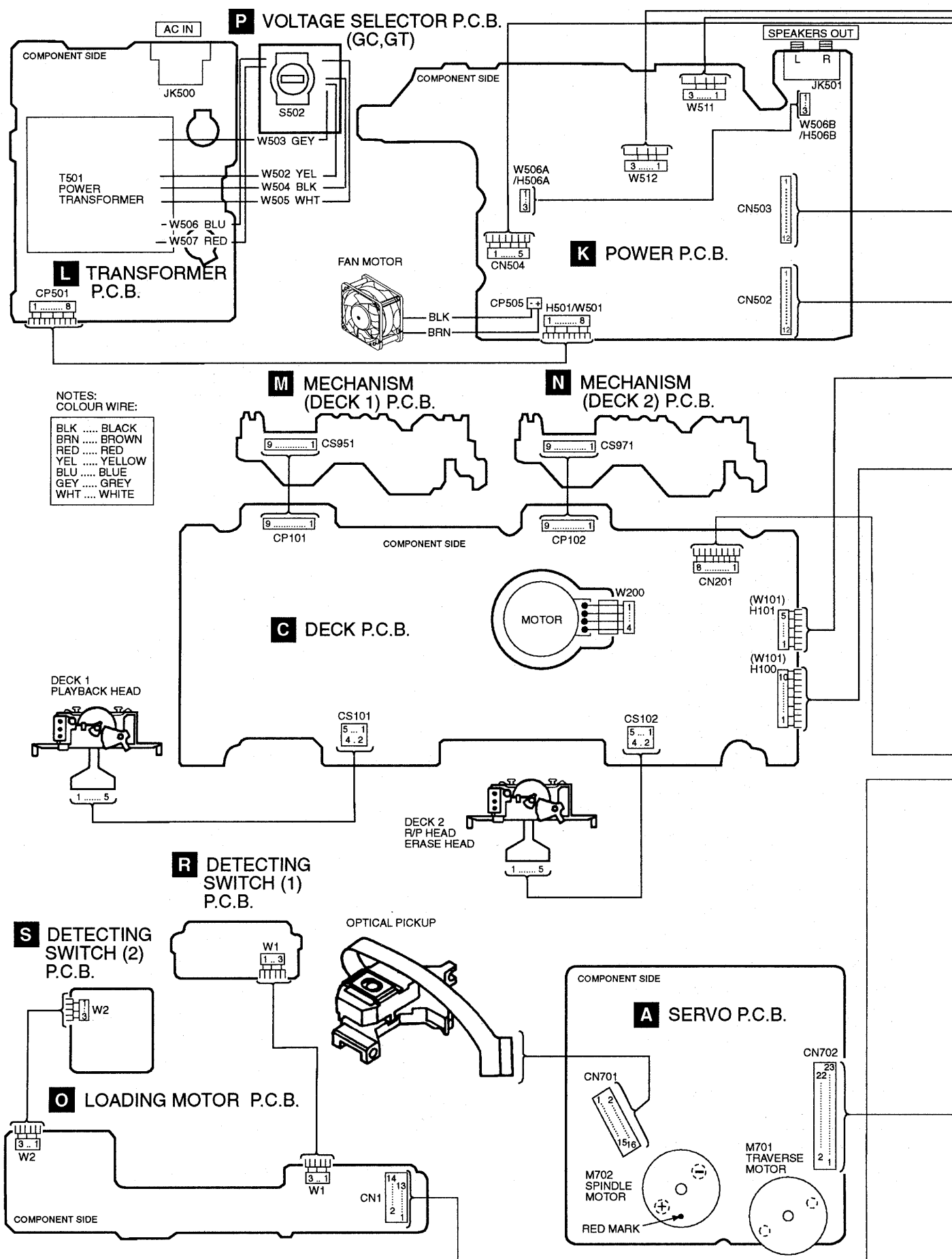
Pin No.	Mark	I/O	Function
			"L" : 16.9344MHz "H" : 33.8688MHz
78	PSEL	I	Test input (normally "L") (Not used, open)
79	MSEL	I	Output mode switching of SUBQ terminal ("H" : Q code buffer mode)
80	SSEL	I	Output frequency switching for SMCK terminal "H" : SMCK=8.4672MHz "L" : MCK=4.2336MHz (Not used, open)

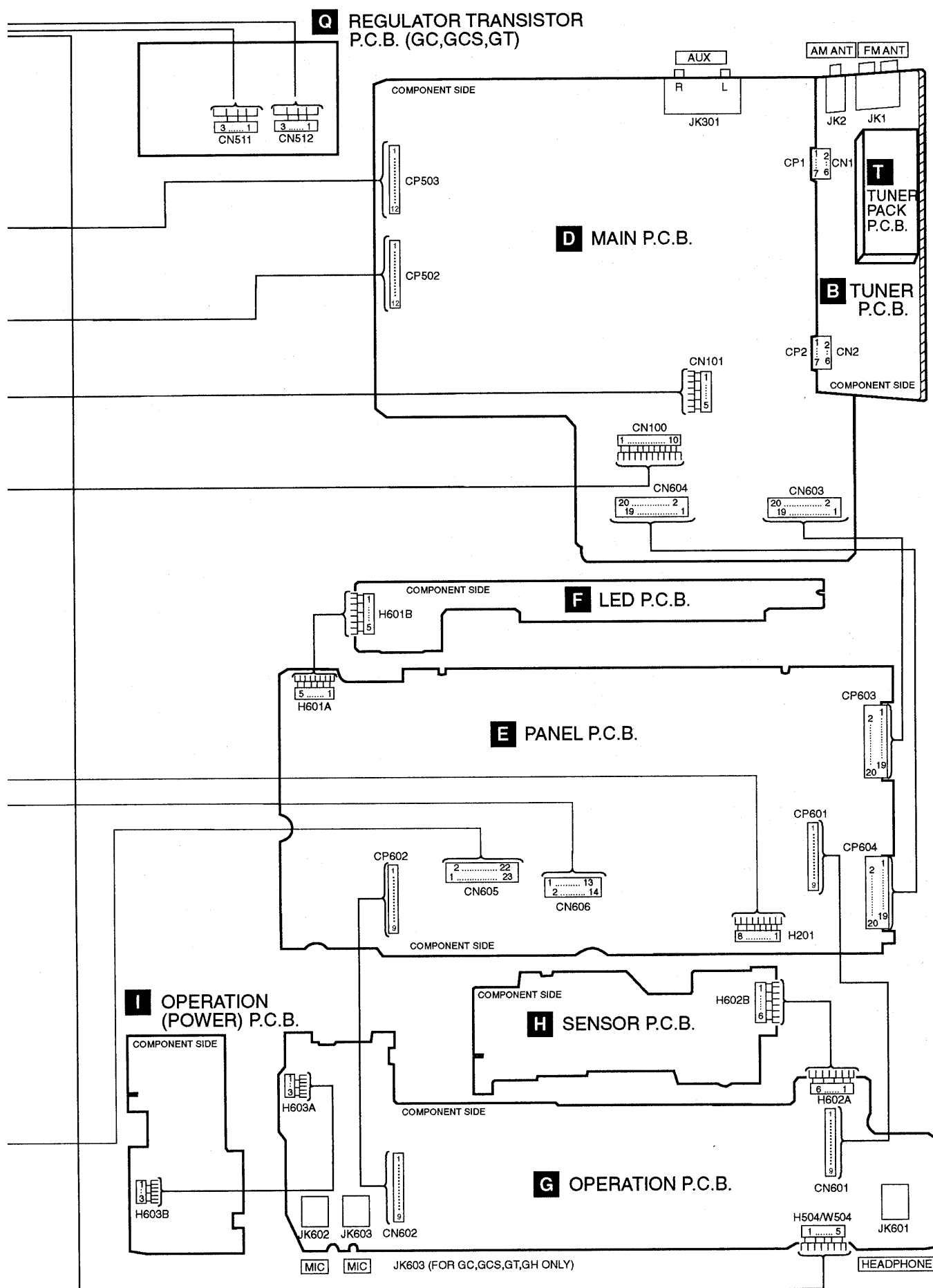
• IC601 (M38197MA136F) System Microprocessor

Pin No.	Mark	I/O	Function
1	DECK 2	I	Mecha condition input(PLAY, FF/RW, MOTOR)
2	DECK 1	I	Mecha condition input(PLAY, FF/RW, MOTOR)
3	TPS	I	TPS input
4	CRT	—	CR timer
5	KEY 4	I	Key 4 input
6	KEY 3	I	Key 3 input
7	KEY 2	I	Key 2 input
8	KEY 1	I	Key 1 input
9	SER 1	O	LED drive clock output
10	VOL OUT	O	Volume control DA output
11	SER 2	O	LED drive data output
12	SER 3	O	LED drive data output
13	SER 4	O	Key control clock output
14	SER 5	O	Key control strobe output
15	SPEANA INPUT	I	Spectrum analyser input
16	CHG SW1	I	CD changer SW input (STK_SW, TUP_SW)
17	CHG SW2	I	CD changer SW input (DR0_SW, PLY_SW, TN0_SW)
18	CDRST	I	CD reset input
19	STATUS	I	CD signal processor status input
20	SQCK	O	CD subcode clock output
21	NC	—	No connection
22	SUBQ	I	CD subcode data input
23	TLOCK	I	CD tracking lock input
24	FLOCK	I	CD focus lock input
25	SENSE	I	CD servo processor sense input
26	MLD/ PLLCE	O	CD command load output
27	MDATA/ PLLDATA	O	CD command data output
28	MCLK/ PLLCLK	O	CD command clock output
29	RESTSW	I	CD REST detect SW input
30	BLKCK	I	CD block clock input

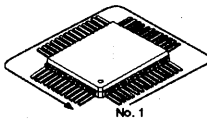
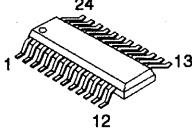
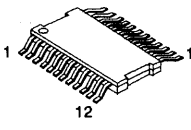
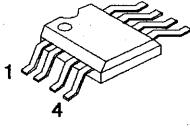
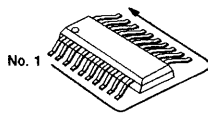
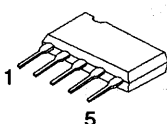
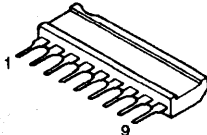
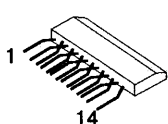
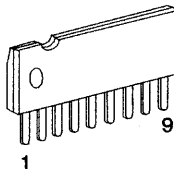
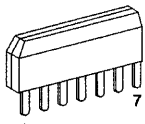
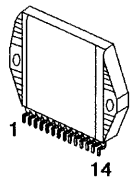
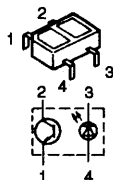
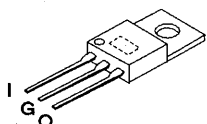
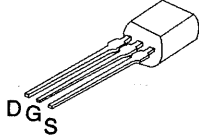
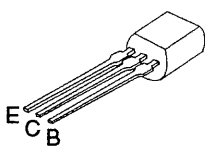
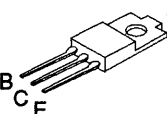
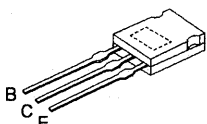
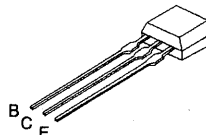
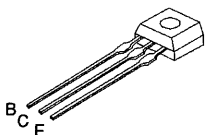
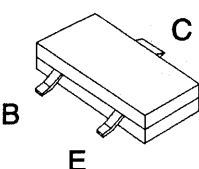
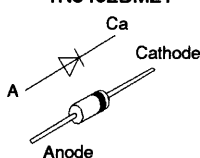
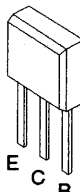
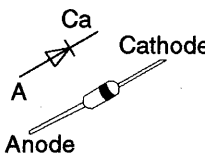
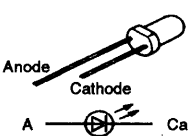
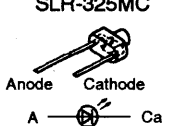
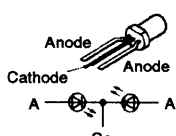
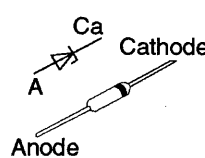
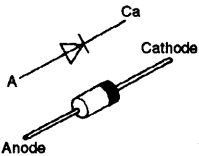
Pin No.	Mark	I/O	Function
31	RMT	I	Remote control signal input
32	DCDET	I	DC detect input
33	P.CONT	O	Power control output
34	/HALT	I	AC failure detect input
35	/RESET	I	RESET input
36	XCIN	I	X'tal oscillator (f = 32.768 kHz sub clock)
37	XCOU	O	X'tal oscillator (f = 32.768 kHz sub clock)
38	XIN	I	X'tal oscillator (f = 6.0 MHz Main clock)
39	XOUT	O	X'tal oscillator (f = 6.0 MHz Main clock)
40	VSS	—	Ground (0V)
41	MBP1	O	MPU beat proof output 1
42	MBP2	O	MPU beat proof output 2
43	CDGMUTE	—	No connection
44	/CDGRESET	—	No connection
45	CD DMUTE	O	CD digital mute output
46	SPE CONT A	—	No connection
47	SPE CONT B	—	No connection
48	SPE CONT C	—	No connection
49-52	GRD16-GRD13	—	No connection
53	GRD12	O	FL digit (grid) drive signal output
54-55	GRD11-GRD10	—	No connection
56-64	GRD9-GRD1	O	FL digit (grid) drive signal output
65-88	AND1-AND24	O	FL segment (anode) drive output
89	JOG A	I	Jog dial signal input A
90	JOG B	I	Jog dial signal input B
91	VCC	I	Power supply (+5V)
92	REGION IN	I	Area setting terminal
93	MKCLK	O	Cassette deck control clock signal output
94	MKDATA	O	Cassette deck control data output
95	SD IN	I	Tuner signal DET input
96	STEREO IN	I	Tuner stereo DET input
97	DO IN	I	Tuner PLL if data input
98	VP	I	Power input (-30V)
99	VSS	—	Ground (0V)
100	VREF	I	Reference for A-D

Wiring Connection Diagram

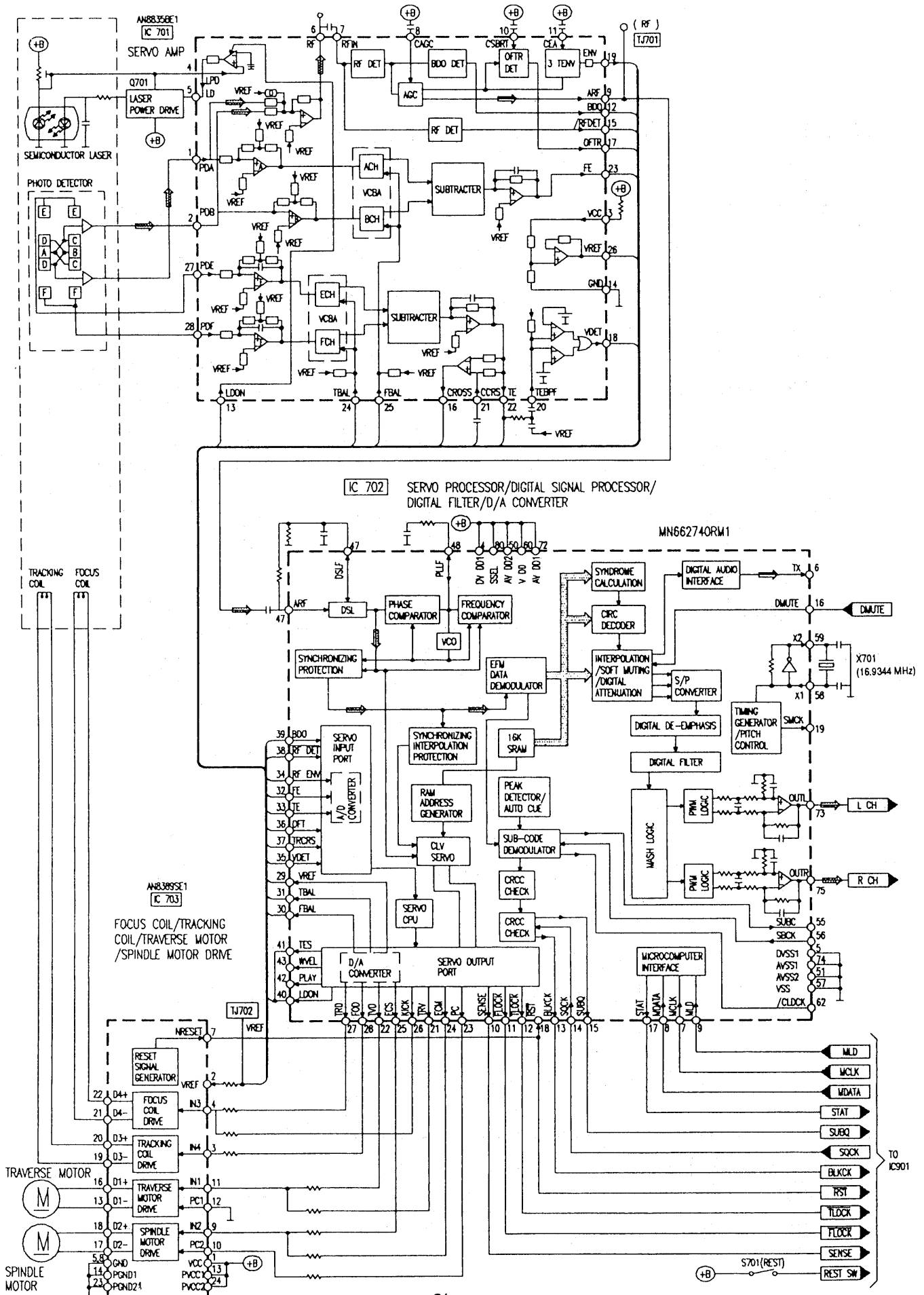


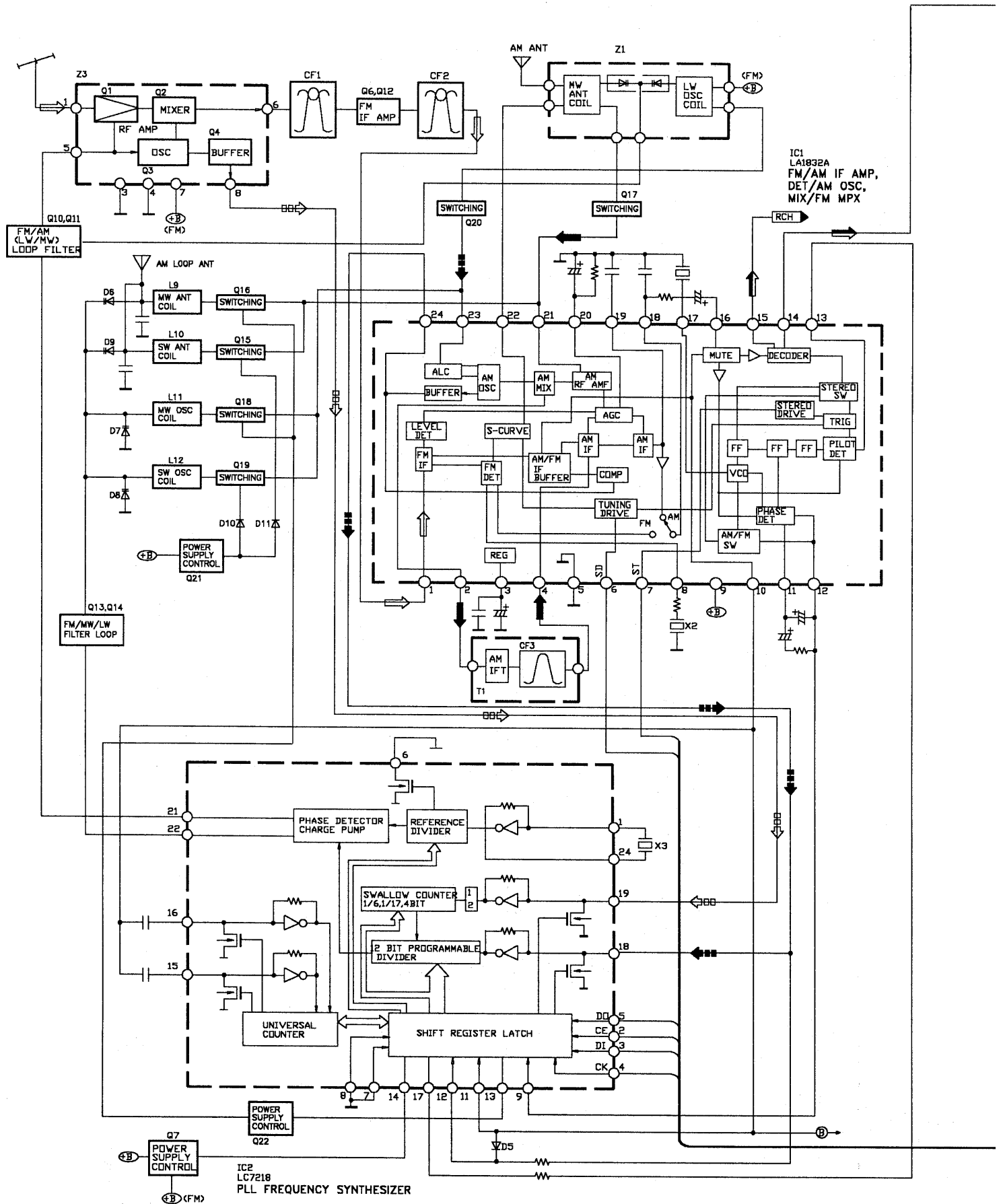


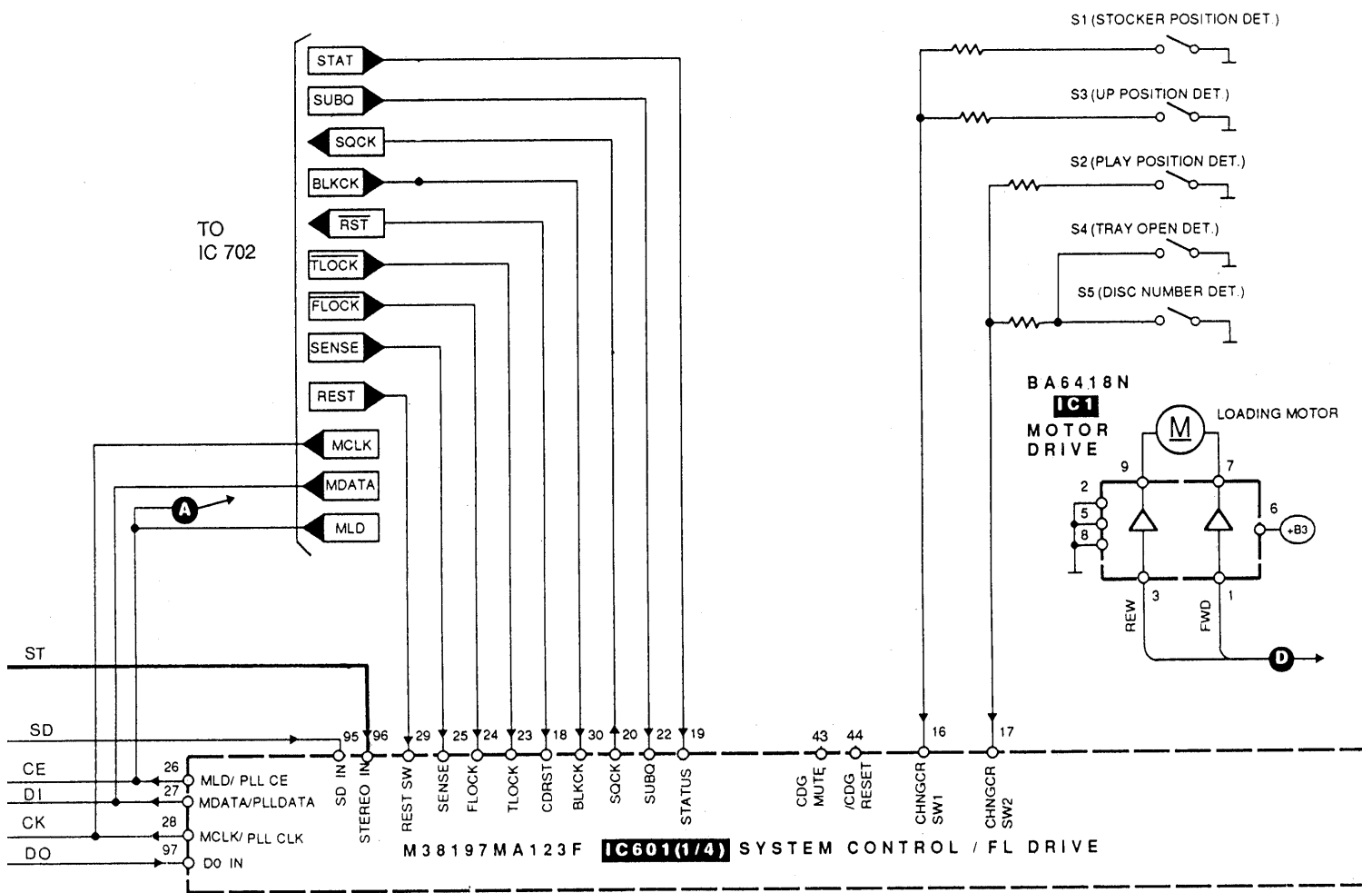
■ Terminal Guide of ICs, Transistors and Diodes

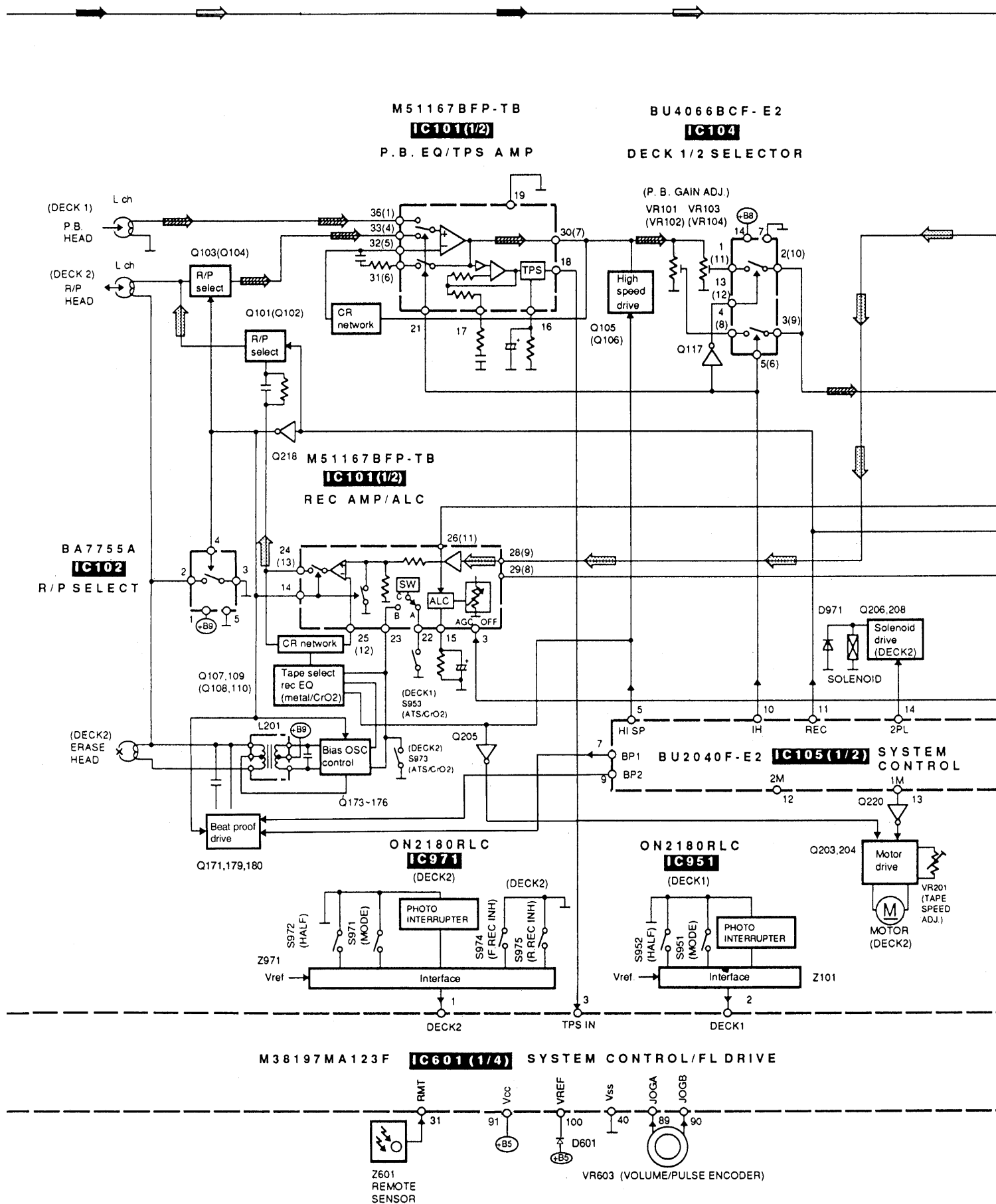
M38197MA136F(100P) MN662741RPA(80P) 	LA1832A LC7218 	AN8389SE1 	BA4558FDXE2 	AN8835SBE1 (28P) BU2040F-E2 (16P) BU2090F-E2 (16P) BU4052BCF-E2 (16P) BU4066BCF-E2 (14P) CXA1102M-T4 (16P) M51167BFP-E1 (36P) M62422FPE1 (42P) 	
BA7755A 	DAP803 	M51131L-702 	BA6418N 	TA2011S 	RSN3502 
ON2180RLC 	LM2940T5M 	2SJ164QRTA 	2SK301QTA 	2SB621ARTA 2SB621RTA 2SC2001KTA 2SD1302STA 2SD965RTA 	
2SB1185E 2SD1762E 	2SD2037ETA 	2SA933SSTA 2SC1740SLNET 2SC1740SSTA RVTDTA143XST 		2SC2785FETA 2SC2785FTA 2SC2787LTA 2SD1020HTA BA1A4ZTA BA1F4MTA BA1L3ZTA BN1L3NTA 	
2SB709S 	1D3E 1N5402BM21 	2SC2784FTA 2SD1450STA BA1L4MTA BA1L4ZTA BN1A4MTA 		1SS254TA 1SS291TA MA165TA MA167TA MA700ATA RVD1SS133TA 	
SLR325DCT31 	SLR342DCTB7 SLR342MCTB7 SLR-325MC 	SPR505MDTT 	MTZJ11CTA MTZJ12BTA MTZJ13ATA MTZJ15BTA MTZJ15CTA MTZJ20BTA MTZJ33CTA MTZJ3R6BTA		MTZJ4R7BTA MTZJ5R1CTA MTZJ5R6BTA MTZJ6R8BTA MTZJ6R8CTA MTZJ7R5CTA MTZJ8R2BTA MTZJ9R1ATA 
RL1N4003N02 					

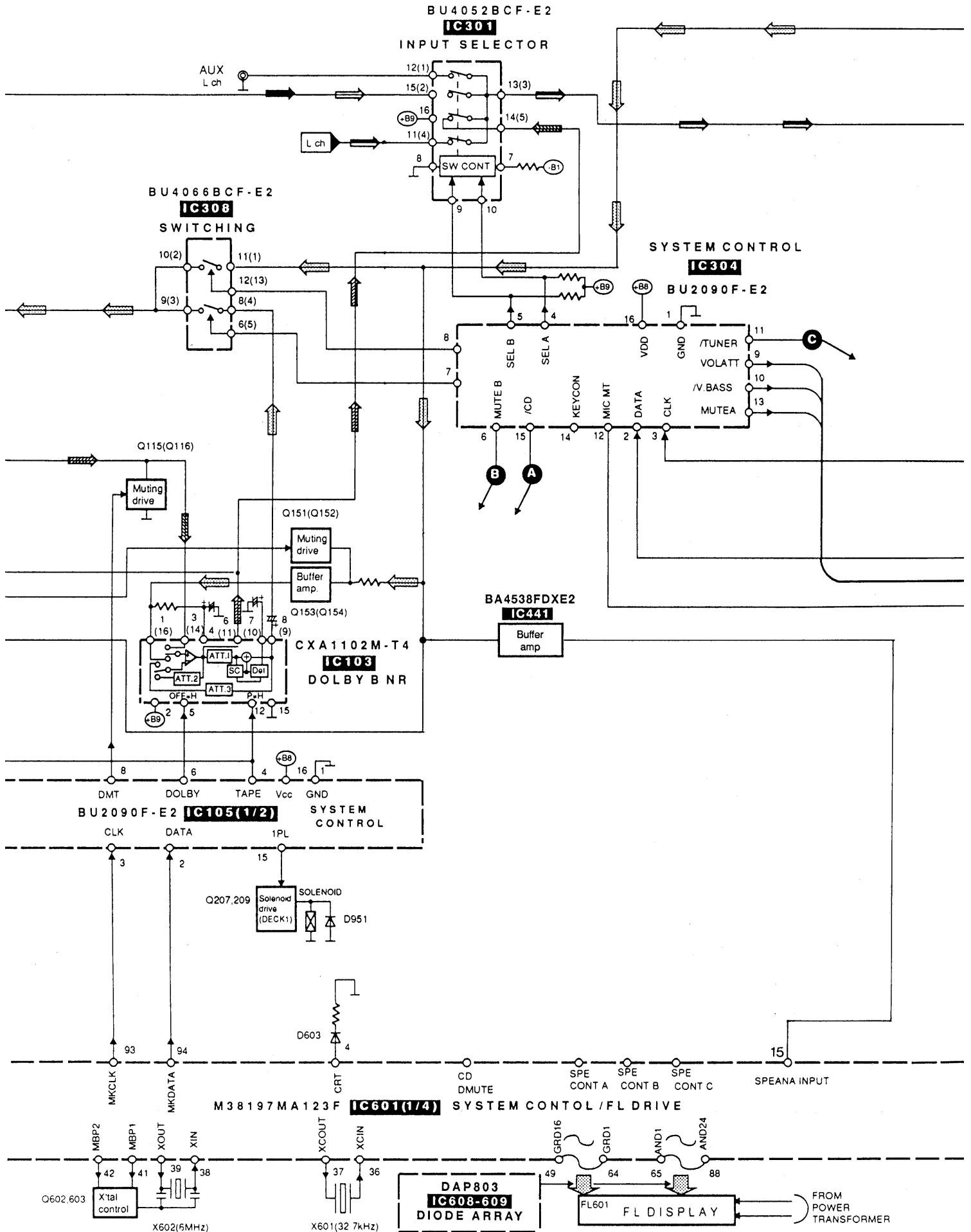
Block Diagram

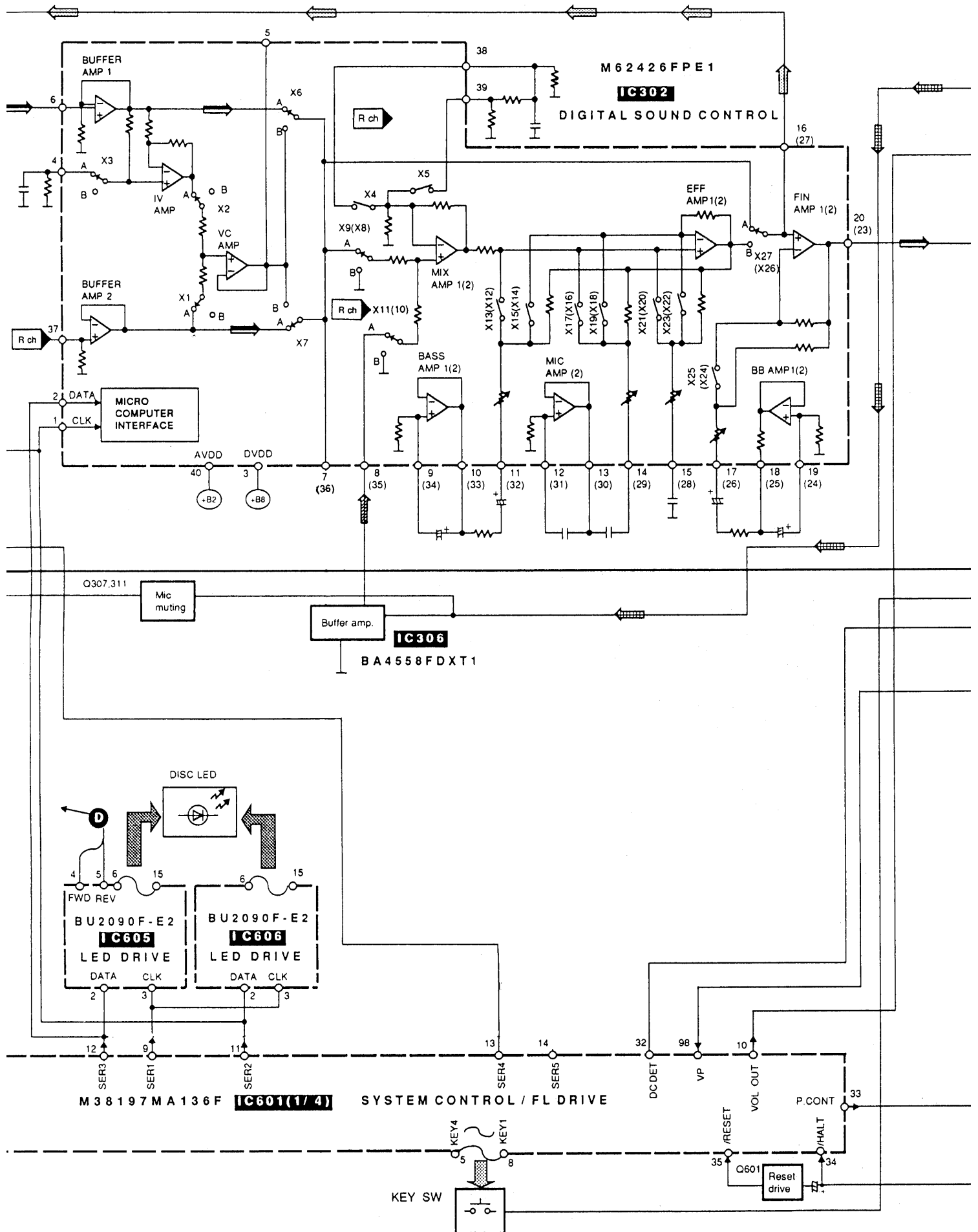


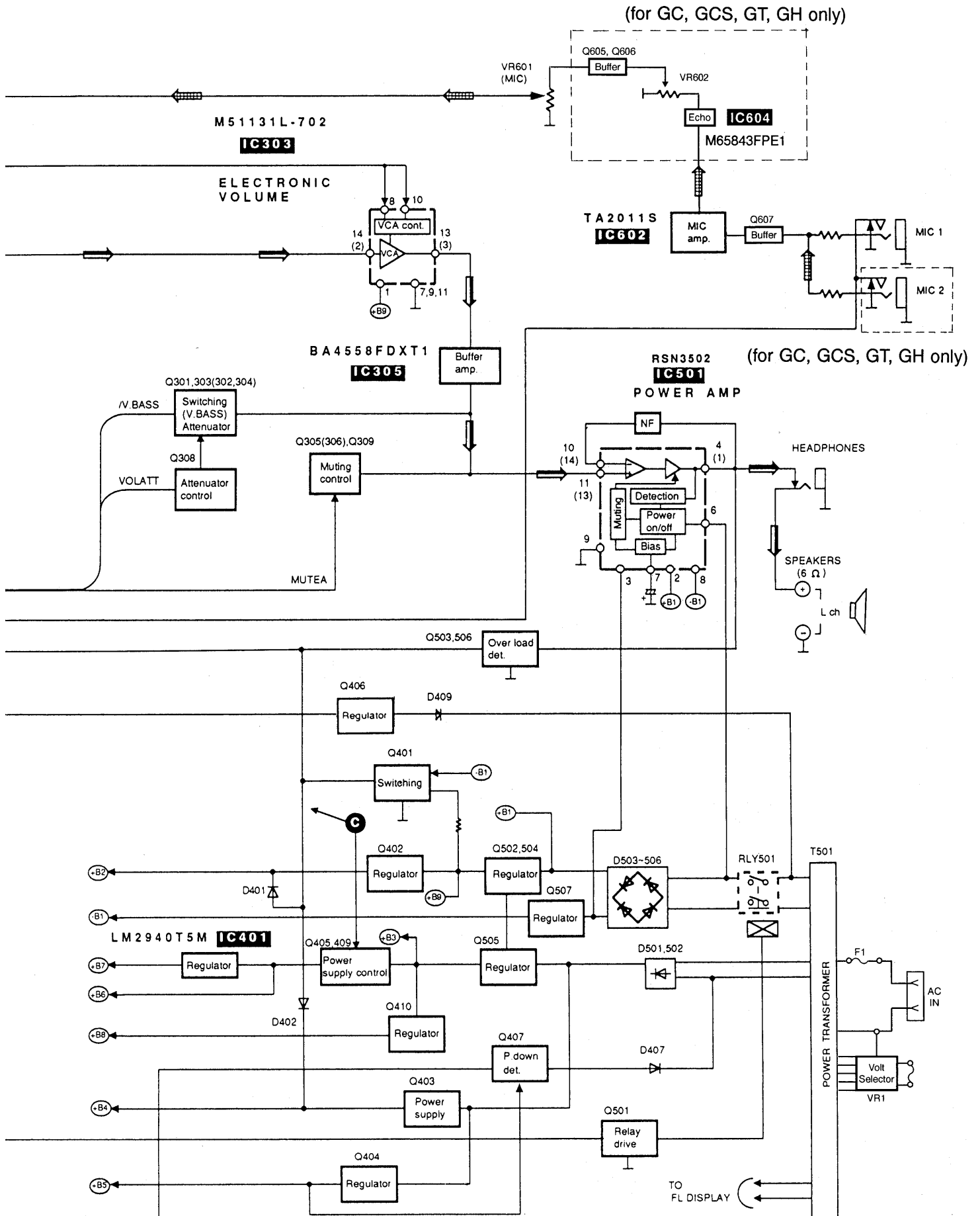






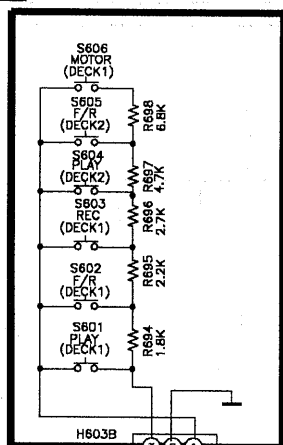




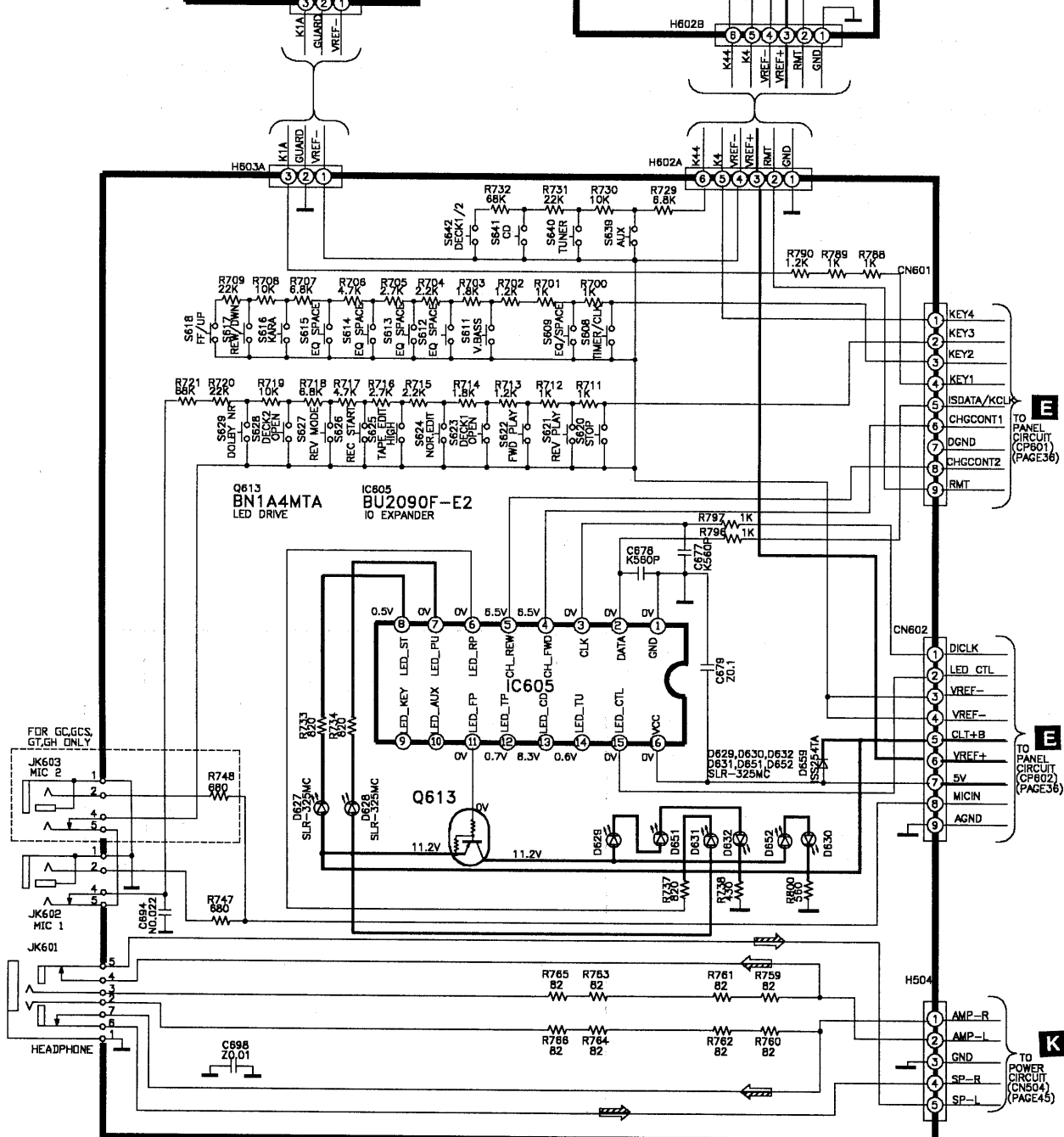
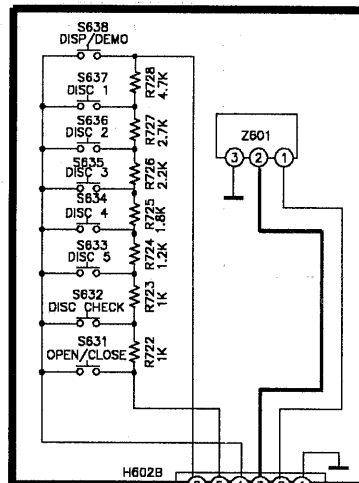


NOTE: FM SIGNAL LINE AM SIGNAL LINE CD SIGNAL LINE RECORDING SIGNAL LINE
 FM OSC SIGNAL LINE AM OSC SIGNAL LINE C D G SIGNAL LINE PLAYBACK SIGNAL LINE
 MIC SIGNAL

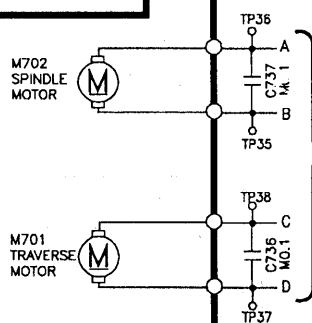
OPERATION (POWER) CIRCUIT



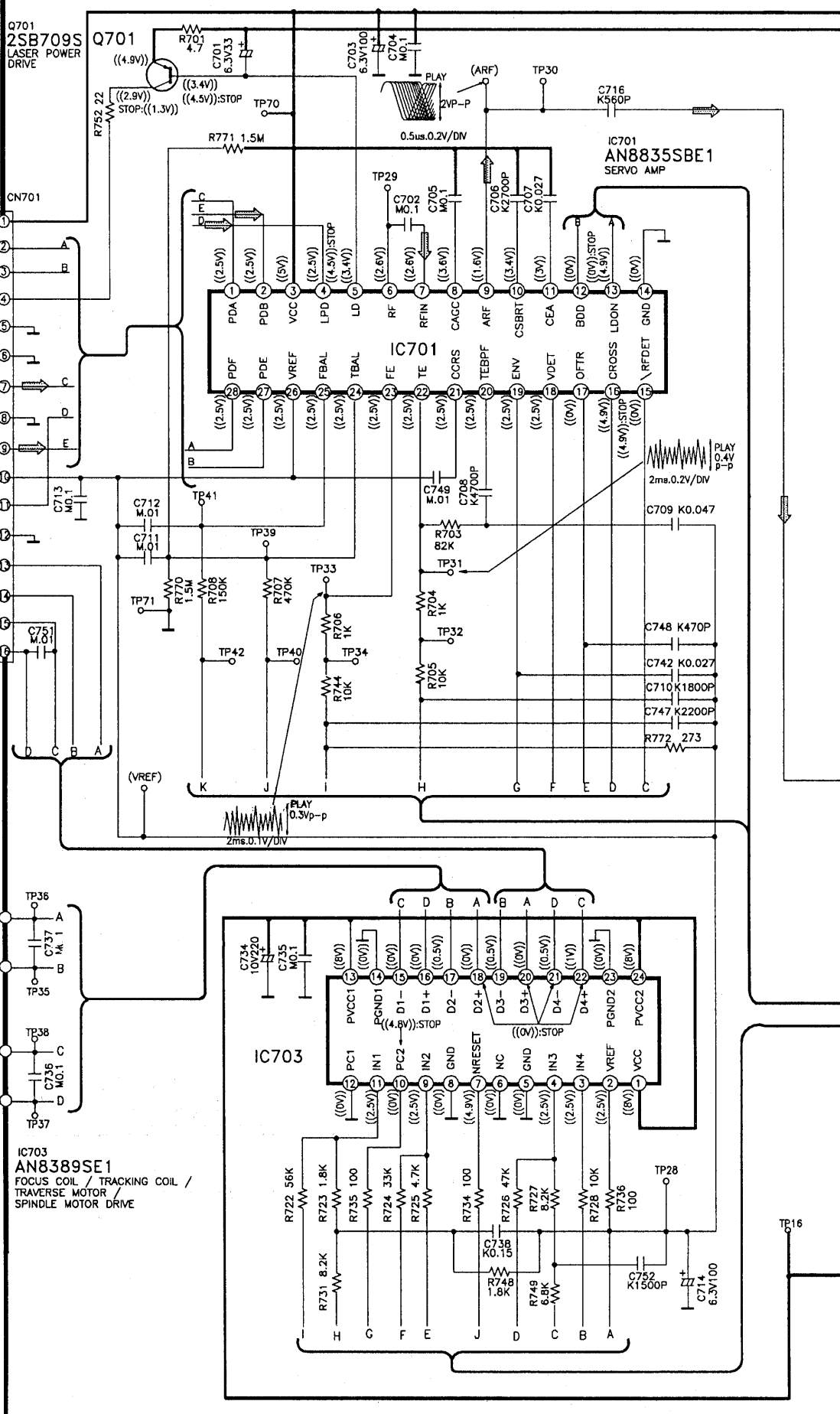
H SENSOR CIRCUIT

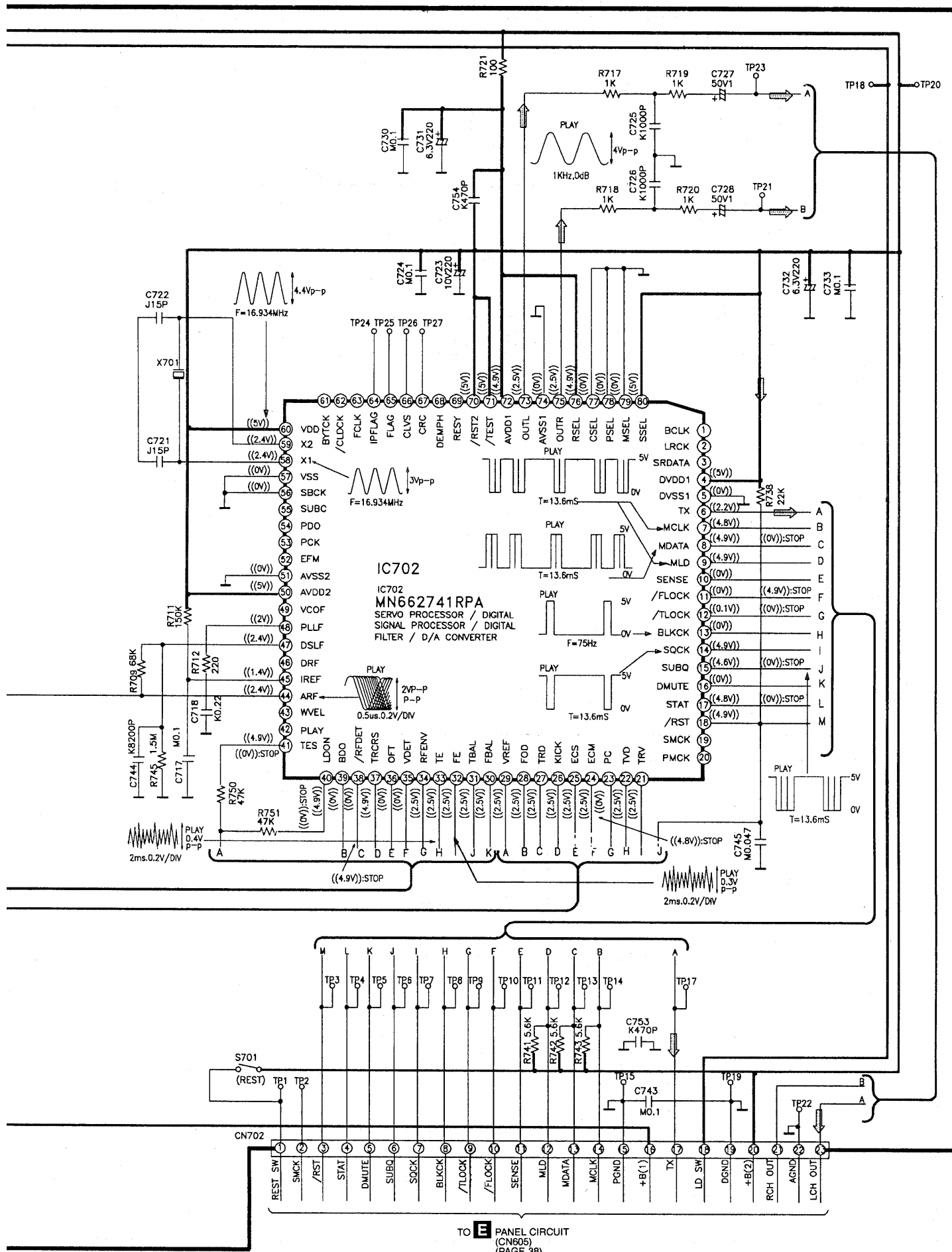


G OPERATION CIRCUIT

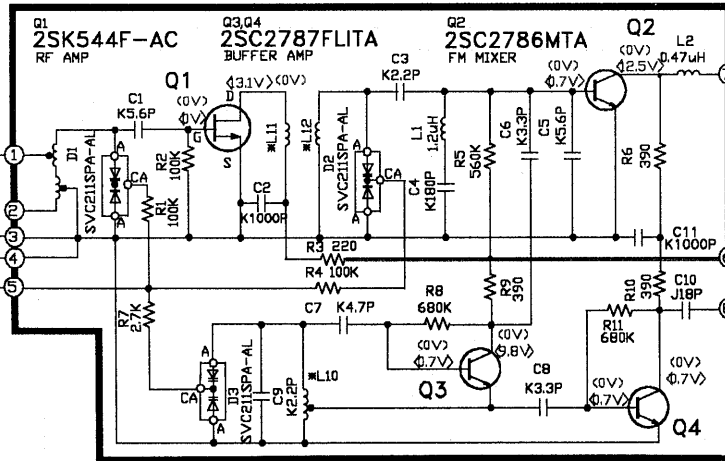
[illegible]

Q701
2SB709S
LASER POWER
DRIVE

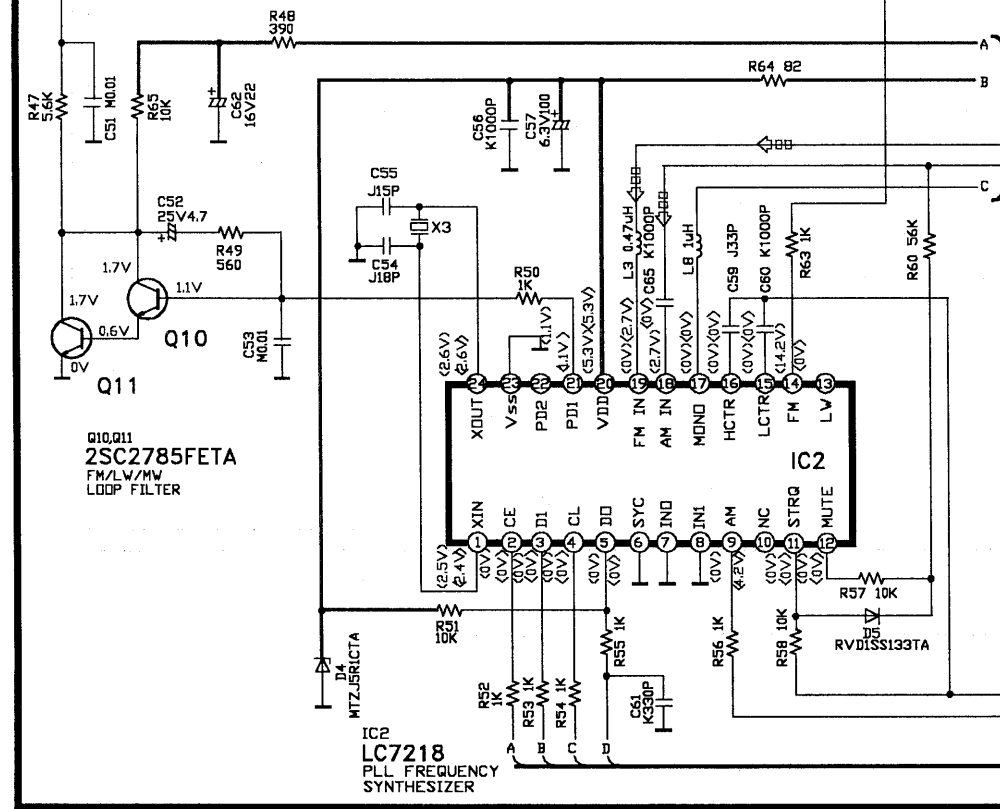
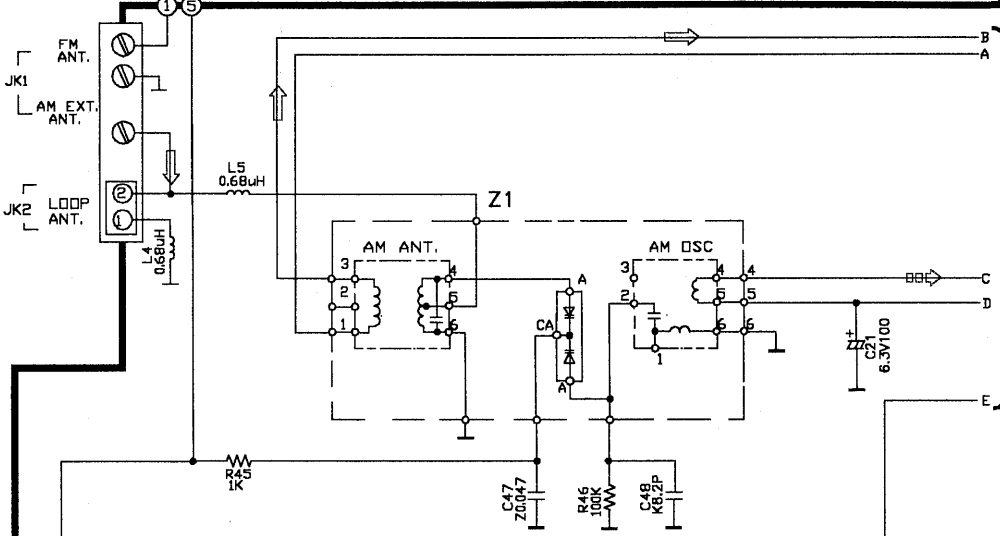


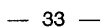


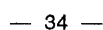
T TUNER PACK CIRCUIT

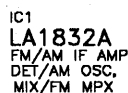


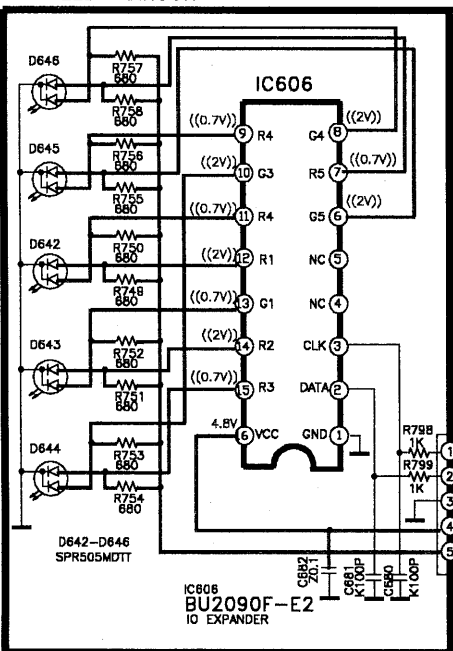
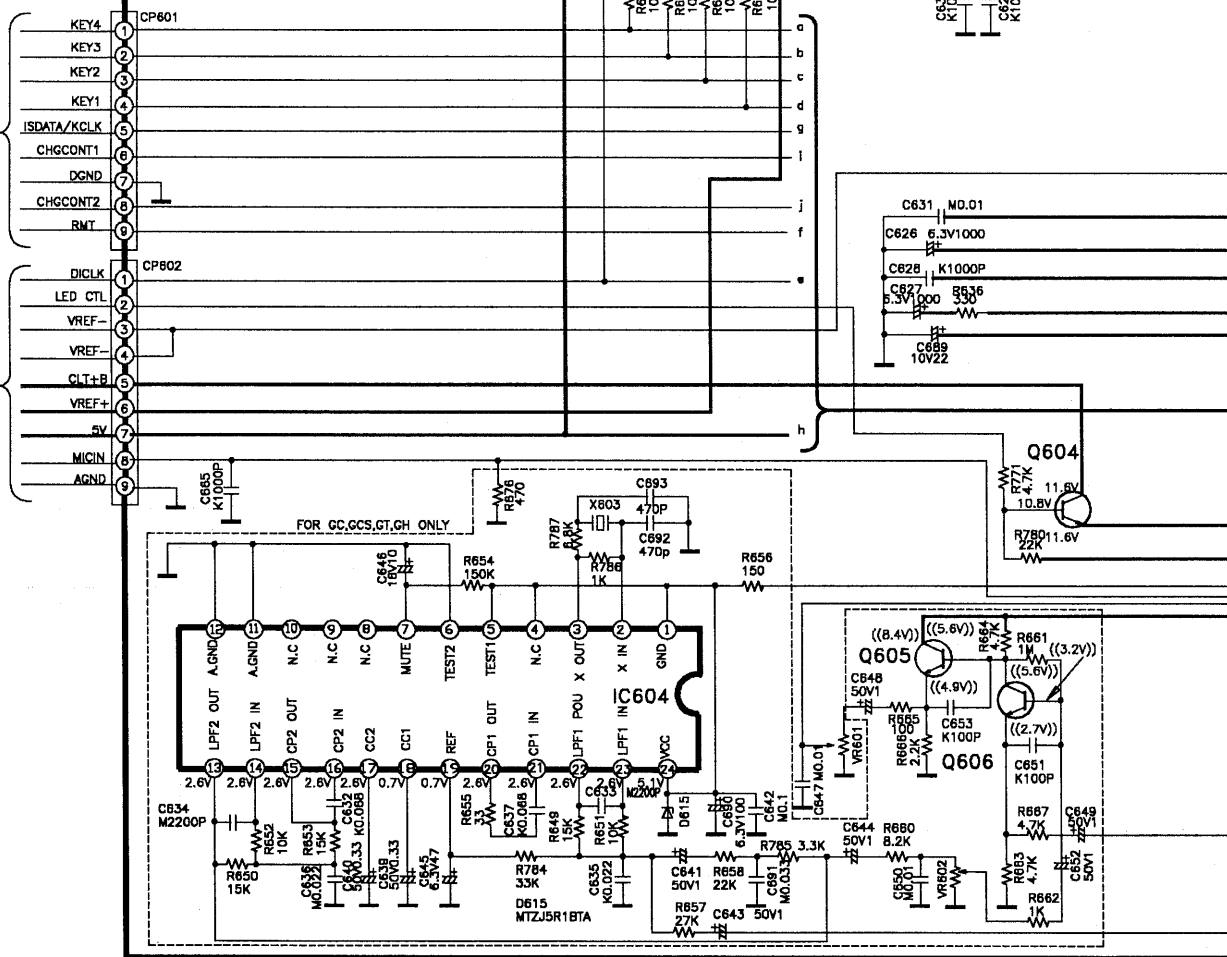
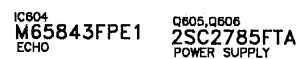
B TUNER CIRCUIT FOR GN, GH area









F**E**

Q612
2SC2785FTA
SYSTEM DRIVE AND FL CONTROL

FL601

D611-D614
MA1677A

IC601
M38197MA136F
SYSTEM DRIVE AND FL CONTROL

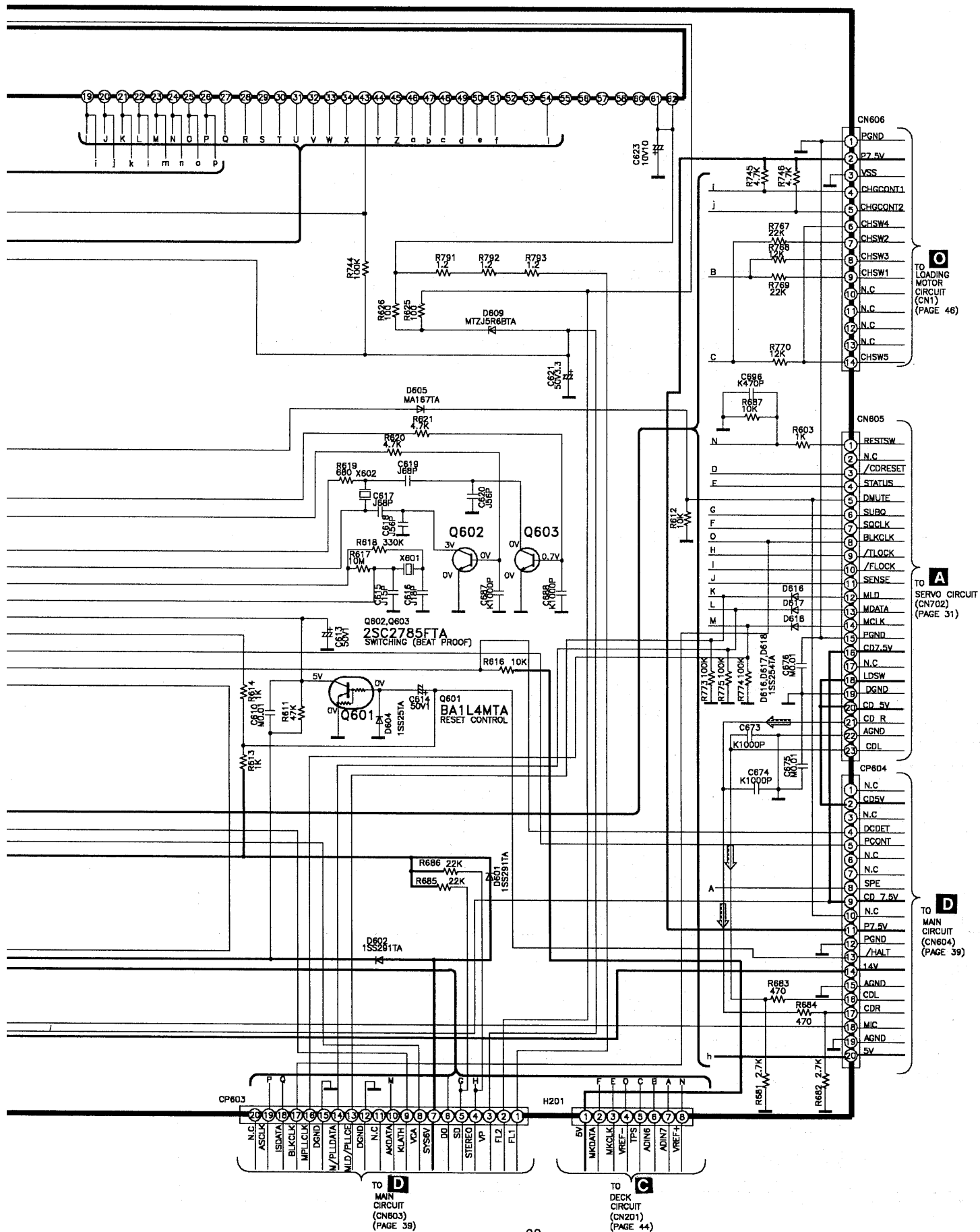
IC602
TA2011S
SYSTEM DRIVE AND FL CONTROL

Q604
2SB621RTA
POWER SUPPLY

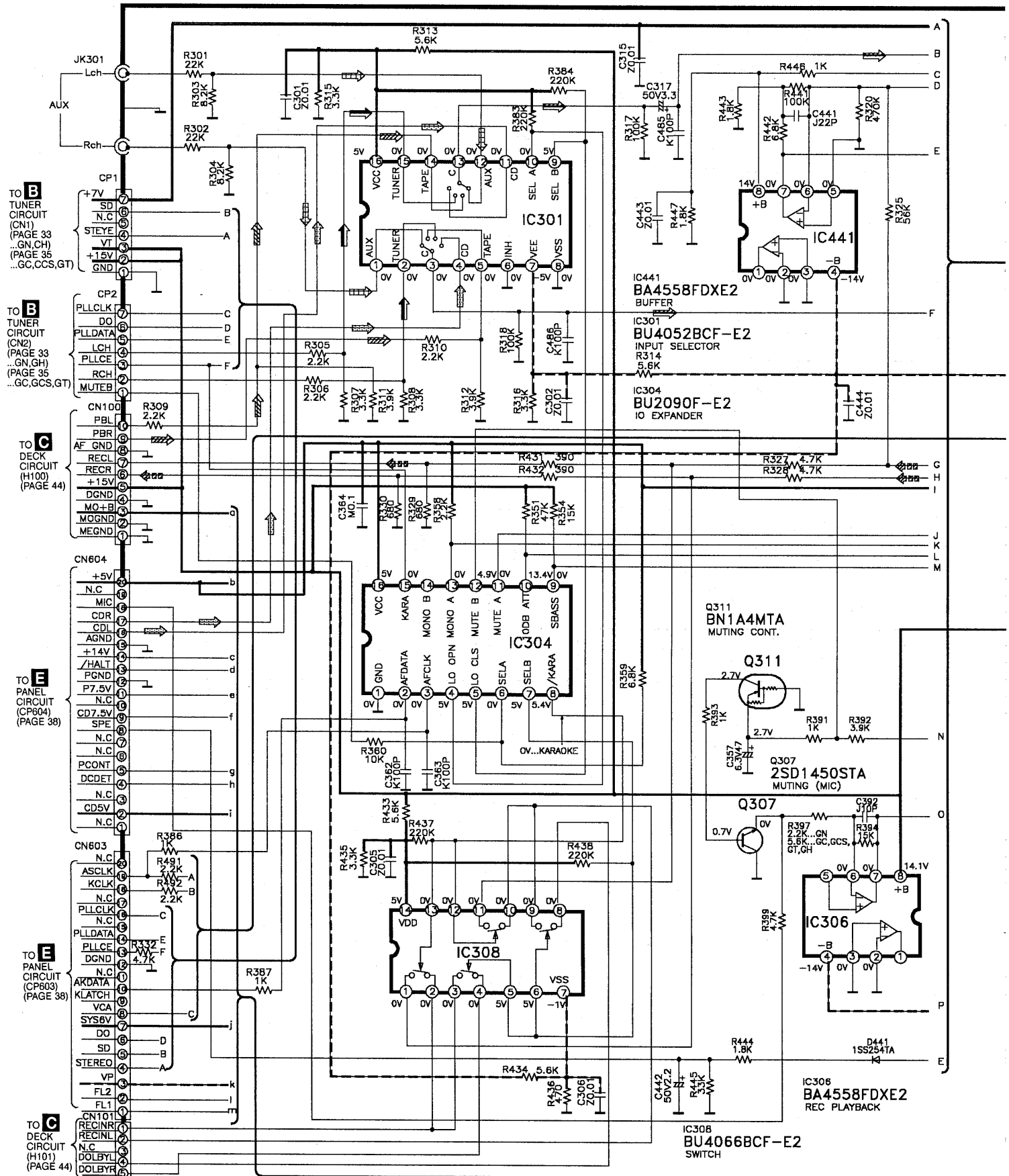
FOR GC,GCS,GT,GH ONLY

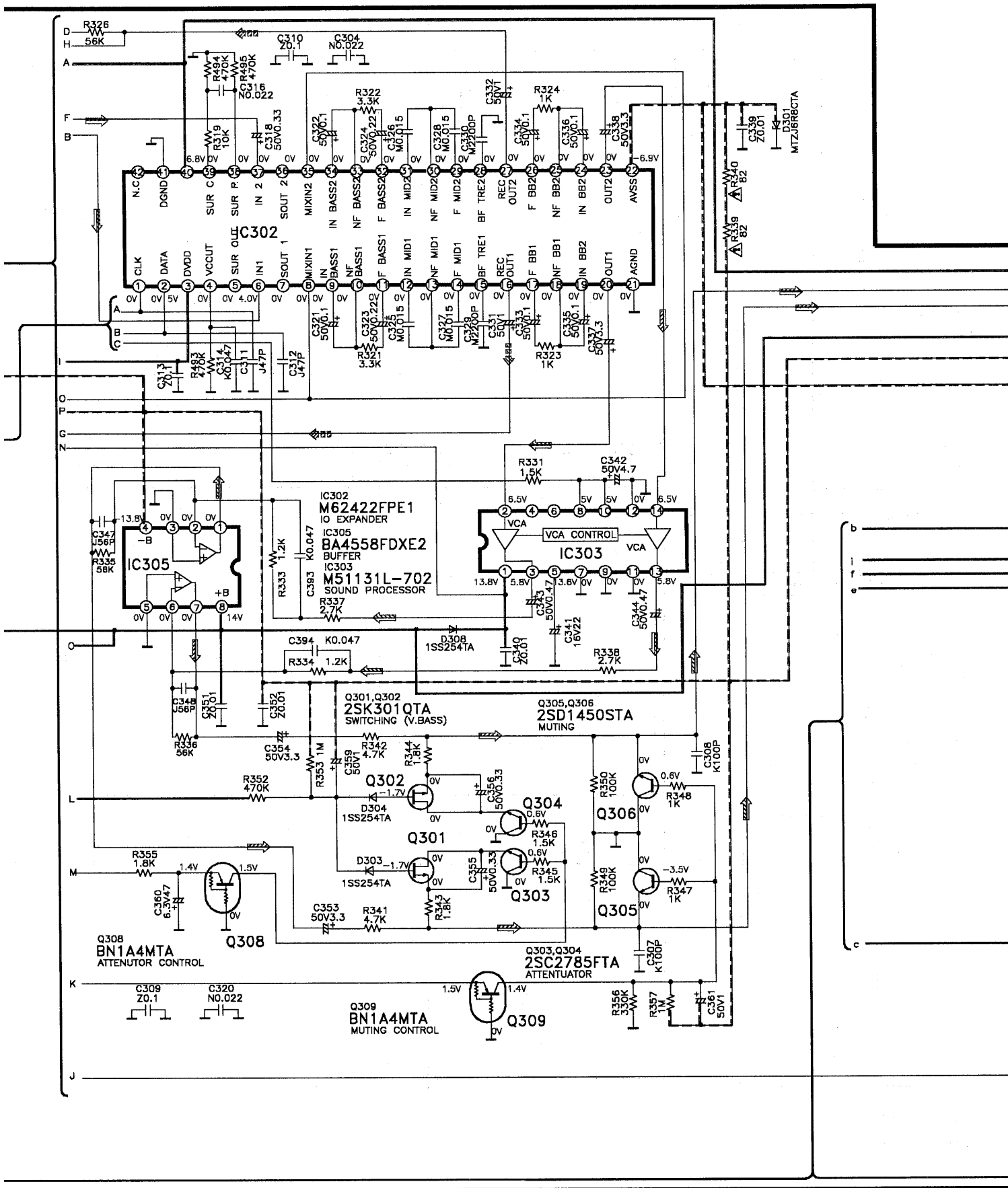
Q607
2SC2785FTA
POWER SUPPLY

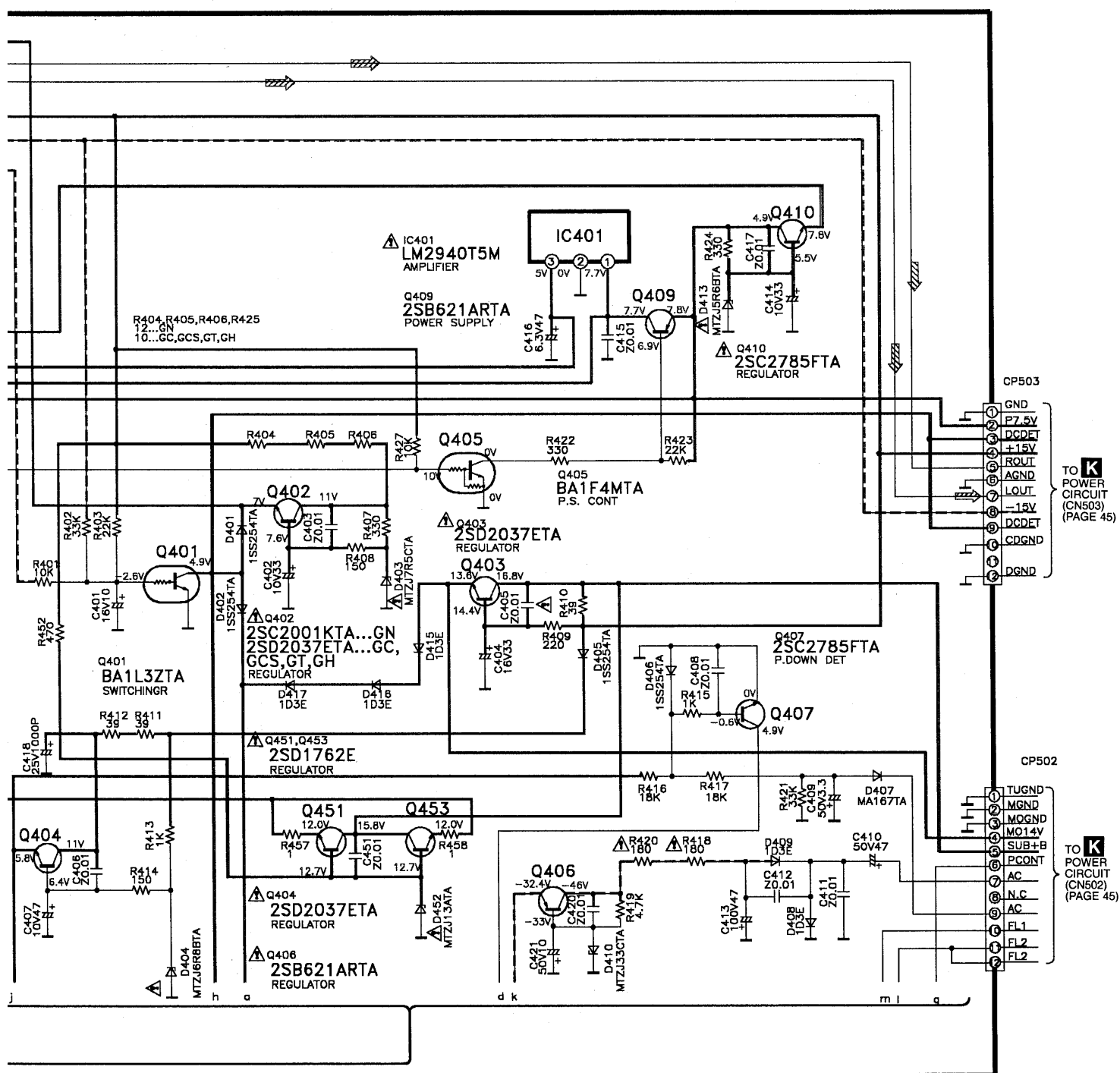
R669
150...GN
820...GC,GCS,GT,GH
R671
470...GN
4.7K...GC,GCS,GT,GH

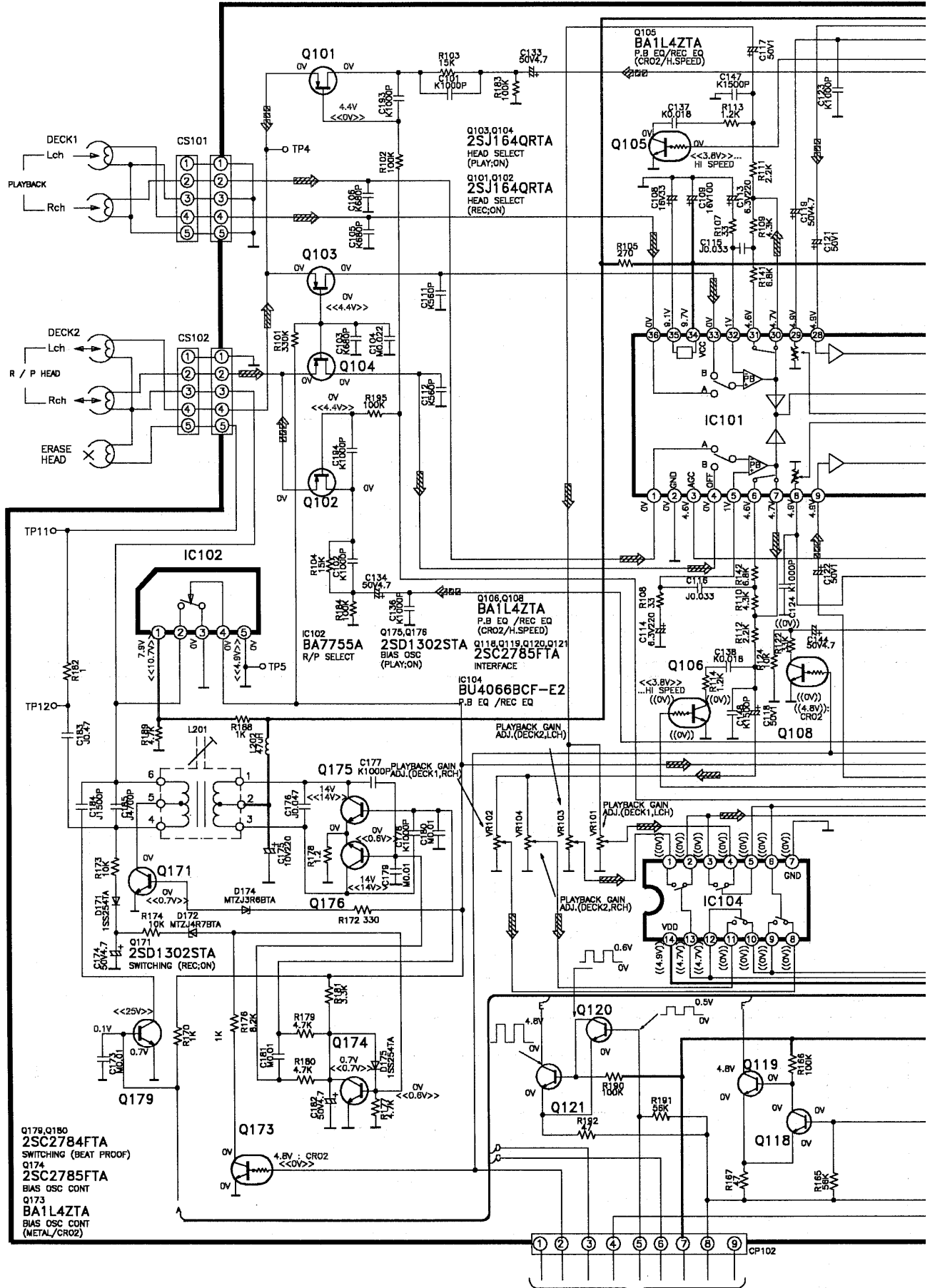


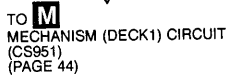
D MAIN CIRCUIT

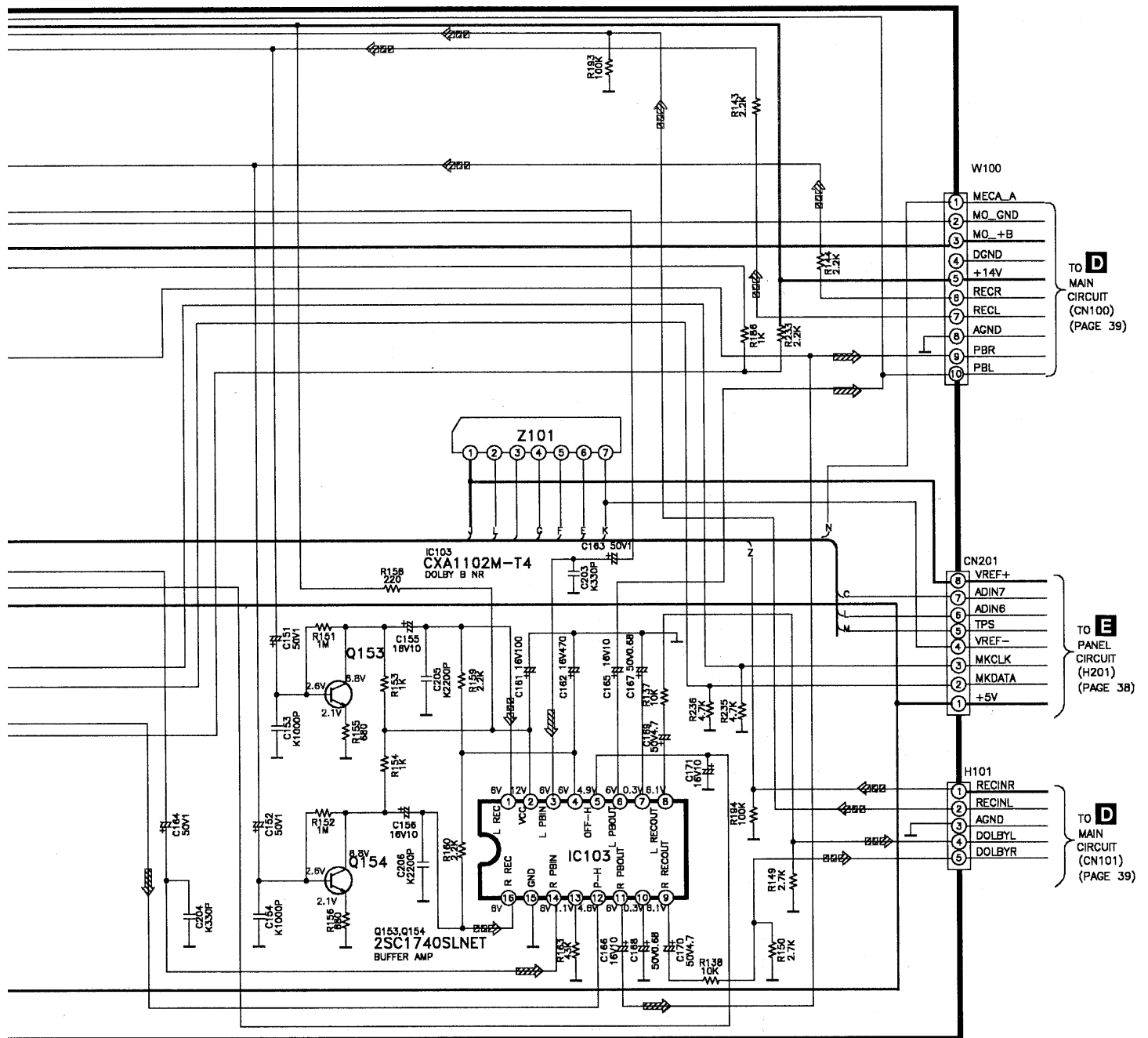




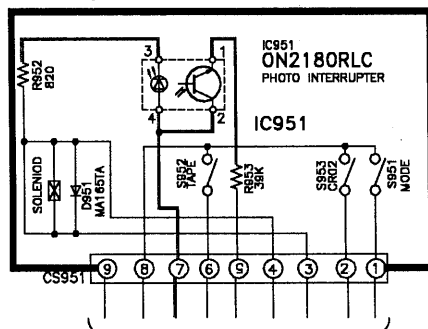


 DECK CIRCUIT


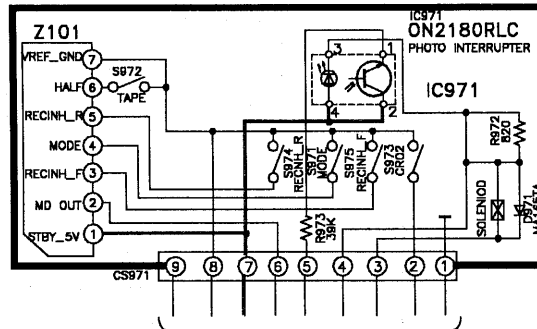




M MECHANISM (DECK 1) CIRCUIT



N MECHANISM (DECK 2) CIRCUIT

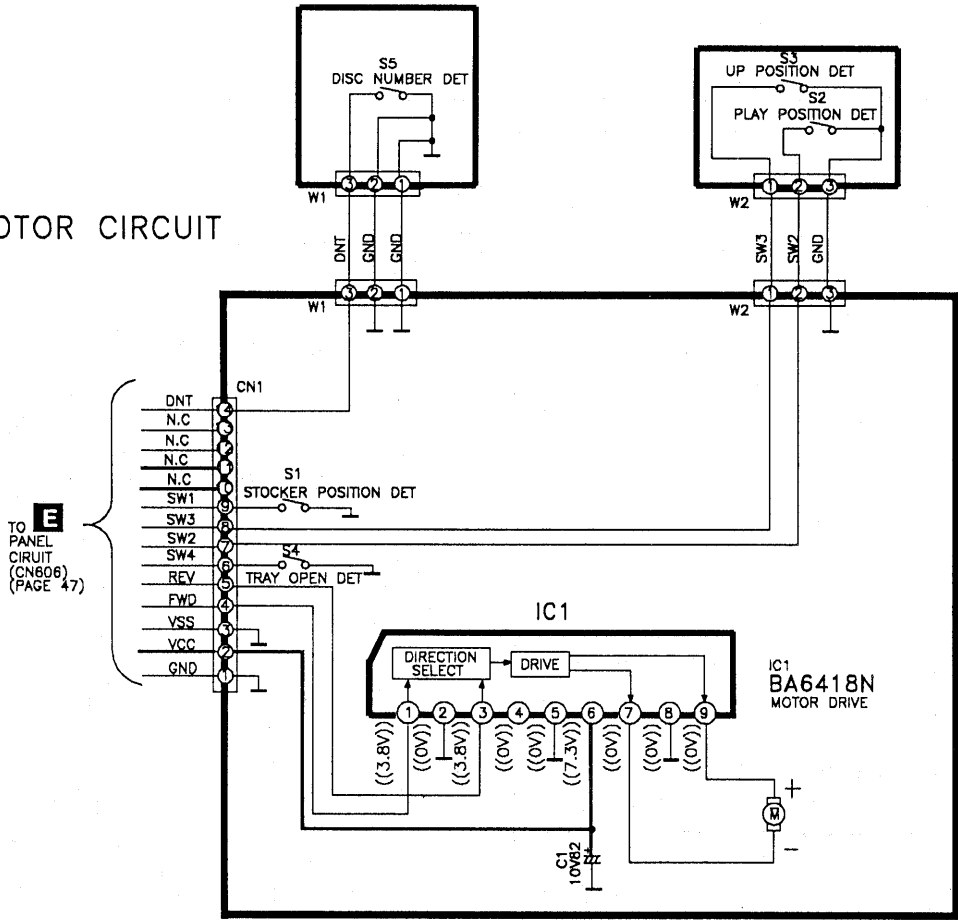




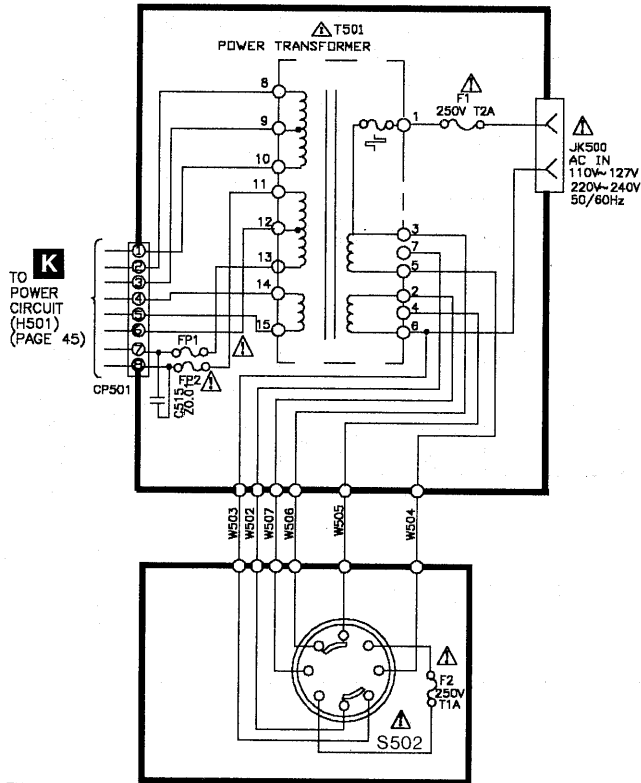
R DETECTING SWITCH (1) CIRCUIT

S DETECTING SWITCH (2) CIRCUIT

O LOADING MOTOR CIRCUIT



L TRANSFORMER CIRCUIT FOR GC & GT



P VOLTAGE SELECTOR CIRCUIT FOR GC & GT