



SERVICE MANUAL



ABS549DU
DM1009

CONTENTS

1. PRECAUTIONS	2
1-1 SAFETY PRECAUTIONS	2
1-2 SERVICING PRECAUTIONS	3
1-2-1 General Servicing Precautions	3
1-2-2 Insulation Checking Procedure	4
1-3 ESD PRECAUTIONS	4
2. REFERENCE INFORMATION	5
2-1 COMPONENT DESCRIPTIONS	5
2-1-1 DVD SONY HM-313 PUH	5
2-1-2 DVD Processor Chip MTK1389D	7
2-1-3 Serial EEPROM, 2K (256 x 8) (24C02) or 16 K (2048 x 8) (24C16)	19
2-1-4: Boot Sector Flash Memory 1M X 8 Bit / 512K X 16 Bit A29L800	20
2-1-5 2 Banks x 512K x 16 Bit Synchronous DRAM HY57V161610E	24
3. PRODUCT SPECIFICATIONS	28
4. UPGRADING SYSTEM AND CHANGING THE REGION CODE	29
5. OPERATING INSTRUCTION	30
MAINTENANCE & TROUBLESHOOTING	30
6. Problems and Solutions	31
7. TROUBLESHOOTING	32
8. RESOLVE DIAGRAM	33
9. BLOCK DIAGRAM	34
10. CIRCUIT DIAGRAMS	35
11. WIRING DIAGRAM:	49

1. PRECAUTIONS

1-1 Safety Precautions

1) Before returning an instrument to the customer, always make a safety check of the entire instrument, including, but not limited to, the following items:

(1) Be sure that no built-in protective devices are defective or have been defeated during servicing.

(1) Protective shields are provided to protect both the technician and the customer. Correctly replace all missing protective shields, including any remove for servicing convenience.

(2) When reinstalling the chassis and/or other assembly in the cabinet, be sure to put back in place all protective devices, including, but not limited to, nonmetallic control knobs, insulating fish papers, adjustment and compartment covers/shields, and isolation resistor/capacitor networks. Do not operate this instrument or permit it to be operated without all protective devices correctly installed and functioning.

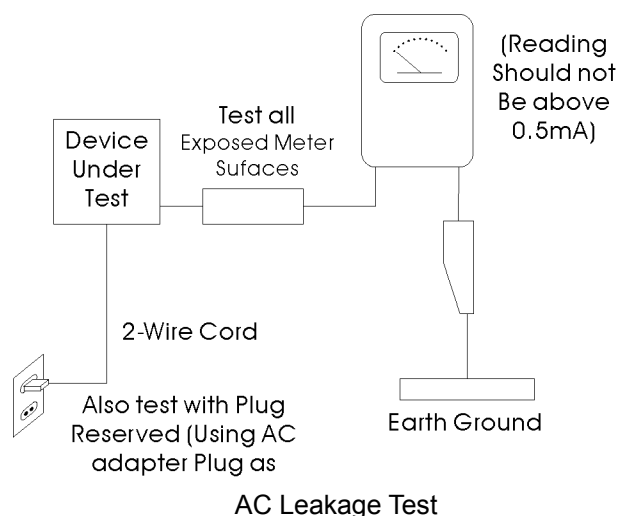
(2) Be sure that there are no cabinet opening through which adults or children might be able to insert their fingers and contact a hazardous voltage. Such openings include, but are not limited to, excessively wide cabinet ventilation slots, and an improperly fitted and/or incorrectly secured cabinet back cover.

(3) Leakage Current Hot Check-With the instrument completely reassembled, plug the AC line cord directly into a 120V AC outlet. (Do not use an isolation transformer during this test.) Use a leakage current tester or a metering system that complies with American National Standards institute (ANSI) C101.1 Leakage.

Current for Appliances and underwriters Laboratories (UL) 1270 (40.7). With the instrument's AC switch first in the ON position and then in the OFF position, measure from a known earth ground (metal water pipe, conduit, etc.) to all exposed metal parts of the instrument (antennas, handle brackets, metal cabinets, screwheads, metallic overlays, control shafts, etc.), especially and exposed metal parts that offer an electrical return path to the chassis.

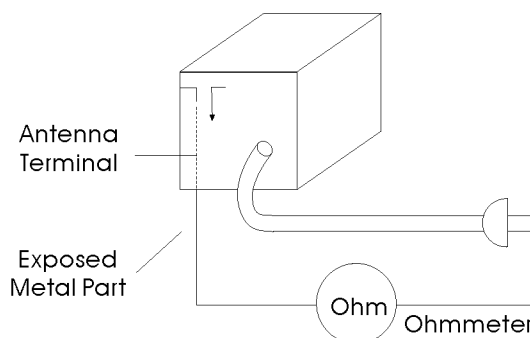
Any current measured must not exceed 0.5mA.

Reverse the instrument power cord plug in the outlet and repeat the test.



Any measurements not within the limits specified herein indicate a potential shock hazard that must be eliminated before returning the instrument to the customer.

(4) Insulation Resistance Test Cold Check-(1) Unplug the power supply cord and connect a jumper wire between the two prongs of the plug. (2) Turn on the power switch of the instrument. (3) Measure the resistance with an ohmmeter between the jumpered AC plug and all exposed metallic cabinet parts on the instrument, such as screwheads, antenna, control shafts, handle brackets, etc. When an exposed metallic part has a return path to the chassis, the reading should be between 1 and 5.2 megohm. When there is no return path to the chassis, the reading must be infinite. If the reading is not within the limits specified, there is the possibility of a shock hazard, and the instrument must be re-pared and rechecked before it is returned to the customer.



- 2) Read and comply with all caution and safety related notes non or inside the cabinet, or on the chassis.
- 3) Design Alteration Warning-Do not alter or add to the mechanical or electrical design of this instrument. Design alterations and additions, including but not limited to, circuit modifications and the addition of items such as auxiliary audio output connections, might alter the safety characteristics of this instrument and create a hazard to the user. Any design alterations or additions will make you, the service, responsible for personal injury or property damage resulting there from.
- 4) Observe original lead dress. Take extra care to assure correct lead dress in the following areas:
 - (1) near sharp edges, (2) near thermally hot parts (be sure that leads and components do not touch thermally hot parts), (3) the AC supply, (4) high voltage, and (5) antenna wiring. Always inspect in all areas for pinched, out-of-place, or frayed wiring. Do not change spacing between a component and the printed-circuit board, Check the AC power cord for damage.
- 5) Components, parts, and/or wiring that appear to have overheated or that are otherwise damaged should be replaced with components, parts and/or wiring that meet original specifications. Additionally determine the cause of overheating and/or damage and, if necessary, take corrective action to remove and potential safety hazard.
- 6) Product Safety Notice-Some electrical and mechanical parts have special safety-related characteristics which are often not evident from visual inspection, nor can the protection they give necessarily be obtained by replacing them with components rated for higher voltage, wattage, etc. Parts that have special safety characteristics are identified by shading, an () or a () on schematics and parts lists. Use of a substitute replacement that does not have the same safety characteristics as the recommended replacement part might create shock, fire and/or other hazards. Product safety is under review continuously and new instructions are issued whenever appropriate.

1-2 Servicing Precautions

CAUTION: Before servicing Instruments covered by this service manual and its supplements, read and follow the Safety Precautions section of this manual.

Note: If unforeseen circumstance create conflict between the following servicing precautions and any of the safety precautions, always follow the safety precautions. Remember; Safety First

1-2-1 General Servicing Precautions

- (1) a. Always unplug the instrument's AC power cord from the AC power source before (1) removing or reinstalling any component, circuit board, module or any other instrument assembly. (2) disconnecting any instrument electrical plug or other electrical connection. (3) connecting a test substitute in parallel with an electrolytic capacitor in the instrument.
 - b. Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.
 - c. Do not apply AC power to this instrument and/or any of its electrical assemblies unless all solid-state device heat sinks are correctly installed.
 - d. Always connect a test instrument's ground lead to the instrument chassis ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.
- Note:** Refer to the Safety Precautions section ground lead last.
- (2) The service precautions are indicated or printed on the cabinet, chassis or components. When servicing, follow the printed or indicated service precautions and service materials.
 - (3) The components used in the unit have a specified flame resistance and dielectric strength. When replacing components, use components which have the same ratings, by () or by () in the circuit diagram are important for safety or for the characteristics of the unit. Always replace them with the exact replacement components.
 - (4) An insulation tube or tape is sometimes used and some components are raised above the printed wiring board for safety. The internal wiring is sometimes clamped to prevent contact with heating components. Install such elements as they were.
 - (5) After servicing, always check that the removed screws, components, and wiring have been installed correctly and that the portion around the serviced part has not been damaged and so on. Further, check the insulation between the blades of the attachment plug and accessible conductive parts.

1-2-2 Insulation Checking Procedure

Disconnect the attachment plug from the AC outlet and turn the power ON. Connect the insulation resistance meter (500V) to the blades of the attachment plug. The insulation resistance between each blade of the

attachment plug and accessible conductive parts (see note) should be more than 1 Megohm.

Note: Accessible conductive parts include metal panels, input terminals, earphone jacks, etc.

1-3 ESD Precautions

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid static electricity) devices can be damaged easily by static electricity.

Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques of component damage caused by static electricity.

- (1) immediately before handling any semiconductor components or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
- (2) after removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
- (3) Use only a grounded-tip soldering iron to solder or unsolder ESD device.
- (4) Use only an anti-static solder removal devices.

Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.

- (5) Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
- (6) Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
- (7) Immediately before removing the protective materials from the leads of a replacement ESD device touch the protective material to the chassis or circuit assembly into which the device will be installed.

CAUTION: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

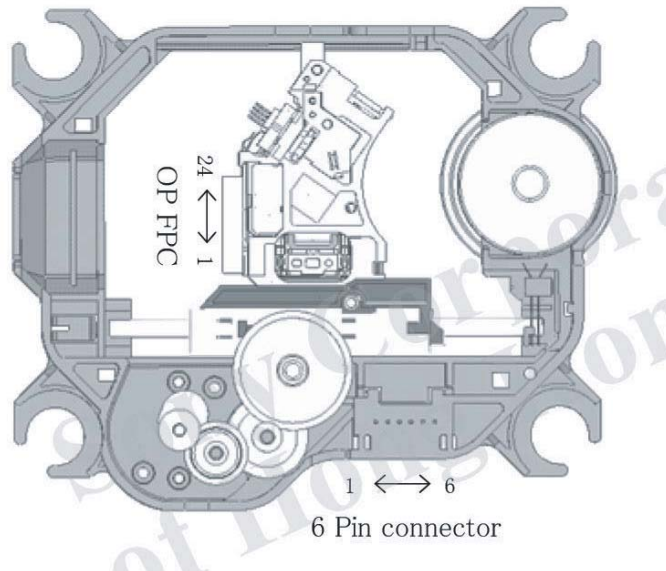
- (8) Minimize bodily motions when handling unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

2. Reference Information

2-1 Component Descriptions

2-1-1 DVD SONY HM-313 PUH

Connector Pin Definition



Terminal of FPC connector for OP

Pin No.	Name
1	FCS-
2	FCS+
3	TRK+
4	TRK-
5	C/c
6	D/d
7	MSW
8	RF
9	A/a
10	B/b
11	F
12	GND
13	Vc
14	Vcc
15	E
16	N/C
17	CD VR
18	DVD VR
19	CD LD
20	PD
21	N/C
22	N/C
23	DVD LD
24	LD GND

Revision History

Revised date	Contents of revision	Reason for revision	Page	Remarks
2009 4 9	1 st Release	Initial Version		Ver 1.0

Contents of Specifications

No	Specifications	Page
	Revision History	1
	Contents of Specification	2
1	Applications	3
2	Type	3
3	Usage	3
4	Structure	3
5	Function	4
6	Pin Assignment	17
7	Absolute Maximum Ratings	18
8	Recommend Operation Conditions	18
9	Electrical Characteristics	19
10	Marking on Devices	29
11	Package Description	29
12	Packing Description	31
13	Solder-Reflow Condition	36
14	Manual Solder Condition	38
15	Storage Condition	38
16	Other	38

1 Applications

This present specifications are applied to IC MT1389G.

2 Type

MT1389G

3 Usage

High Definition DVD Player SOC with HDMI™¹ Tx

4 Structure

0.13um CMOS process, Silicon material, Monolithic IC, 128pin LQFP with EPAD, 3.3/1.2 Dual operation voltages.

Mediatek Confidential Only for Vtrek.

¹ "HDMI™, the HDMI™ logo and High-Definition Multimedia Interface are trademarks or registered trademark of HDMI™ Licensing LLC."

5 Function

5-1 General Description

MediaTek MT1389G is a cost-effective DVD system-on-chip (SOC) which incorporates advanced features like MPEG-4 video decoder, high quality TV encoder, state-of-art de-interlace processing, and HDMI™ 1.3 compatible transmitter. The MT1389G enables consumer electronics manufacturers to build high quality, USB2.0, MS/SD/MMC reader, feature-rich DVD players, portable DVD players or any other home entertainment audio/video devices.

World-Leading Technology: Based on MediaTek's world-leading DVD player SOC architecture, the MT1389G is the New generation of the DVD player SOC. It integrates the MediaTek 3rd generation front-end digital RF amplifier and the Servo/MPEG AV decoder.

Enjoy the attractive video on digital TV: The most popular HDTV input format is HDMI™ interface and it provides up to 1080P high resolution video output and high quality audio output.

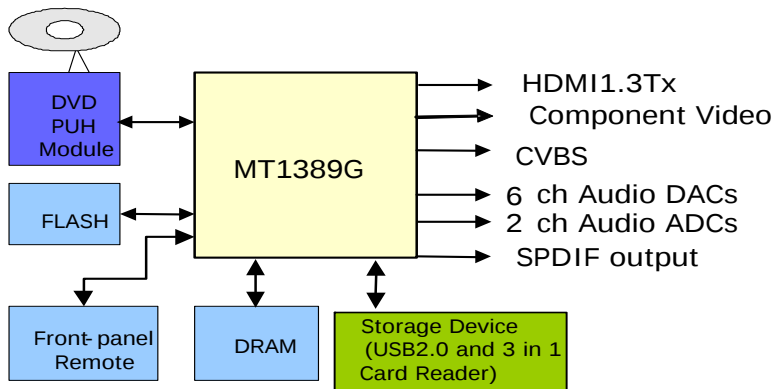
Rich Feature for High Valued Product: To enrich the feature of DVD player, the MT1389 equips a simplified MPEG-4 advanced simple profile (ASP) video decoder to fully support the DivX² Home Theater profile. It makes the MT1389-based DVD player be capable of playback MPEG-4 content which become more and more popular.

Incredible Audio/Video Quality: The progressive scan of the MT1389G utilized MediaTek's MDDi™ advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. It also supports a patent-pending edge-preserving algorithm to remove the saw-tooth effect. The 148MHz/12-bit video DACs provide users a whole new viewing experience. It also supports a 3:2 pull down algorithm to give the best film effect. Built-in 6ch audio DACs and 2ch audio ADCs could give the variable function solutions.

High Performance Memory Storage Device: As the core of Portable DVD players need more capability to support current multimedia contents. The MT1389G provides the interface for the 3-in-1 card reader, which supports Memory-Stick, Secure Digital Memory Card, and MultiMediaCard, to connect with the mainstream digital camera FLASH cards. For the USB application, we adopt USB2.0 High speed specification to reach rich-contents transference. USB 2.0 High speed will support for high-speed devices. USB 2.0 High Speed is suitable for high-performance devices such as high-density storage devices. In addition, USB 2.0 High Speed supports USB 1.0/1.1 devices, offering impressive and even better compatibility to customers

² DivX is a trademark of DivXNetworks

³ USB High Speed : maximum 480Mbit/sec. USB Full Speed : maximum 12Mbit/sec.



DVD Player System Diagram

Key Features

- RF/Servo/MPEG Integration
- DivX Home Theater Level MPEG4 ASP Video decoder
- Support DivX Ultra
- High Performance Audio Processor
- Progressive Scan
- Internal 6CH Audio DAC
- Internal 2CH Audio ADC
- MDDi: Motion-Adaptive, Pure Edge™ De-interlacing
- 148MHz/12-bit TV Encoder
- USB2.0 High Speed (Host)
- 3-in-1 MS/SD/MMC reader
- HDMI™ 1.3 Tx with CEC support
- USB 2.0 High Speed (Host)

5-2 Key Features

- RF/Servo/MPEG Integration
- Embedded 6ch Audio DAC
- Embedded 2ch Audio ADC for Karaoke
- High Performance Audio Processor
- High Performance Progressive Video Processor
- HDMI™ 1.3 Tx with CEC support
- MDDi: Motion-Adaptive Pure Edge™ De-interlacing
- High Quality 148MHz/12-bit TV Encoder
- Support DivX Ultra
- USB 2.0 High-Speed

Applications

Standard DVD Players

5-3 General Feature lists

■ Super Integration DVD player single chip

- High performance analog RF amplifier
- Servo controller and data channel processing
- MPEG-1/MPEG-2/JPEG video
- Dolby AC-3/DTS Decoder
- Unified memory architecture
- Versatile video scaling & quality enhancement
- OSD & Sub-picture
- Built-in clock generator
- Built-in progressive video processor
- HDMI™ 1.3 Tx with CEC support
- MDDi: Motion-Adaptive, Pure Edge™ De-interlacing
- Built-in High Quality 148MHz/12-bit TV Encoder
- Audio effect post-processor
- Built-in 5.1-ch Audio DAC
- Built-in 2-ch Audio ADC for Karaoke
- USB 2.0 High-Speed
- MS/SD/MMC 3-in-1 card reader

■ Speed Performance on Servo/Channel Decoding

- DVD-ROM up to 4XS
- CD-ROM up to 24XS

■ Channel Data Processor

- Digital data slicer for small jitter capability
- Built-in high performance data PLL for channel data demodulation
- EFM/EFM+ data demodulation
- Enhanced channel data frame sync protection & DVD-ROM sector sync protection

■ Servo Control and Spindle Motor Control

- Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
- Built-in ADCs and DACs for digital servo control
- Provide 2 general PWM
- Tray control can be PWM output or digital output

■ Embedded Micro controller

- Built-in 8032 micro controller
- Built-in internal 373 and 8-bit programmable lower address port
- 1024-bytes on-chip RAM
- Up to 2M bytes FLASH-programming interface
- Supports 5/3.3-Volt. FLASH interface
- Supports power-down mode
- Supports additional serial port

■ DVD-ROM/CD-ROM Decoding Logic

- High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
- Automatic sector Mode and Form detection
- Automatic sector Header verification
- Decoder Error Notification Interrupt that signals various decoder errors
- Provide error correction acceleration

■ Buffer Memory Controller

- Supports 16Mb/32Mb/64Mb/128Mb SDRAM
- Supports 16-bit SDRAM data bus
- Provides the self-refresh mode SDRAM
- Block-based sector addressing

■ Video Decoder

- Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
- Decodes MPEG-4 Advanced Simple Profile
- Support DivX 3.11/4.x/5.x Home Theater Profile
- Support DivX Ultra
- Smooth digest view function with I, P and B picture decoding
- Baseline, extended-sequential and progressive JPEG image decoding
- Support CD-G titles

■ Video/OSD/SPU/HLI Processor

- Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
- 65535/256/16/4/2-color bitmap format OSD,
- 256/16 color RLC format OSD
- Automatic scrolling of OSD image
- Support 480i/480p/576i/576p Display
- Support 720p/1080i Display
- Support 1080p Display
- Simultaneous HD/SD output

■ 2-D Graphic Engine

- Support decode Text and Bitmap
- Support line, rectangle, and gradient fill
- Support bitblt
- Chroma key copy operation

■ Audio Effect Processing

- Dolby Digital (AC-3)
- DTS decoding
- MPEG-1 layer 1/layer 2 audio decoding
- High Definition Compatible Digital (HDCD)
- Windows Media Audio (WMA)
- Dolby ProLogic II
- IEC 60958/61937 output
 - PCM / bit stream / mute mode
- Pink noise and white noise generator
- Karaoke functions
 - Microphone echo
 - Microphone tone control
 - Vocal mute/vocal assistant
 - Key shift up to +/- 8 keys
 - Chorus/Flanger/Harmony/Reverb
- Channel equalizer
- 3D surround processing include virtual surround and speaker separation

■ TV Encoder

- Four 148MHz/12-bit DACs
- Support NTSC, PAL-BDGHINM, PAL-60
- Support 525p, 625p progressive TV format
- Support Macrovision 7.1 L1 and 1.3 (525p/625p).
- CGMS-AWSS
- Closed Caption

■ MDDi™ Progressive Scan Video

- Automatic detect film or video source
- 3:2 pull down source detection
- Advanced Motion adaptive de-interlace
- PureEdge™ edge preserving technology
- PureEdge™ edge preserving technology V2
- Minimum external memory requirement

■ HDMI™ Tx V1.3

- Compatible with HDMI™ 1.3, DVI 1.0, HDCP 1.3
- Support EIA/CEA 861B 480i/ 480p/ 576i/ 576p/ 720p/ 1080i/ 1080p
- Maximum 8 channels 192k audio output
- Support audio sampling rate conversion
- Hot-plug and power-on detection
- HDMI™ display full screen
- CEC function support
- Deep Color support
- xvYcc Support

■ Image Resizer

Video case

- Support progressive / Interlaced frame scaling
- Support input & output maximum size: 4096x4096

JPEG case

- Input memory layout of source images must be scan line based
- Deal with one block line (height:8 / 16) each round
- Input maximum size: 65535x65535
- Output maximum size: 4096x4096
- Support a output scaling window at arbitrary location in an output frame buffer
- Y / Cb / Cr separated

■ Serial Flash Interface

- Supports 4Mb/8Mb/16Mb/32Mb/64Mb SPI interface Serial Flash

■ External Interface

- USB2.0 High Speed (Host)
- Memory-Stick, Secure Digital Memory Card, and MultiMediaCard Interface

■ Outline

- 128-pins EPAD LQFP package
- 3.3/1.2-Volt. Dual operating voltages

Version 1.0

Specifications are subject to change without notice

General Feature – Third Party Proprietary Right

1. Dolby License

Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

2. Macrovision License

This device is protected by U.S. patent numbers 4,631,603, 4,577,216, 4,819,098 and other intellectual property rights.

3. DTS License

©1996-2006 DTS, Inc.

4. Microsoft License

This product included technology owned by Microsoft Corporation and cannot be used or distributed without a license from Microsoft GP.

5-4 Pin Definitions

Abbreviations:

- SR: Slew Rate
- PU: Pull Up
- PD: Pull Down
- SMT: Schmitt Trigger
- 4mA~16mA: Output buffer driving strength.

Pin	Main	Alt.	Type	Description
Analog Interface (66)				
119	RFIP		Analog Input	AC coupled DVD RF signal input RFIP
120	RFIN	OPOUT GPI36	Analog Input	1) AC coupled DVD RF signal input RFIN 2) GPI36
121	RFG	OPINP	Analog Input	Main beam, RF AC input path
122	RFH	OPINN	Analog Input	Main beam, RF AC input path
123	RFA		Analog Input	RF main beam input A
124	RFB		Analog Input	RF main beam input B
125	RFC		Analog Input	RF main beam input C
126	RFD		Analog Input	RF main beam input D
127	RFE		Analog Input	RF sub beam input E
128	RFF		Analog Input	RF sub beam input E
1	AVDD12_2		Analog power	Analog 1.2V power
2	AVDD33_1		Analog Power	Analog 3.3V power
3	XTALI		Input	27MHz crystal input
4	XTALO		Output	27MHz crystal output
5	V20		Analog output	Reference voltage 2.0V
6	V14		Analog output	Reference voltage 1.4V
7	REXT	GPO5	Analog Input / Digital output	1) Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS. 2) GPO5
8	MDI1		Analog Input	Laser power monitor input
9	LDO1		Analog Output	Laser driver output
10	LDO2		Analog Output	Laser driver output
11	AVDD33_2		Analog Power	Analog 3.3V power
12	DMO		Analog Output	Disk motor control output. PWM output

Pin	Main	Alt.	Type	Description
13	FMO		Analog Output	Feed motor control. PWM output
14	TRAY_OPEN	GPIO	Analog Output	Tray PWM output/Tray open output
15	TRAY_CLOSE	GPIO	Analog Output	Tray PWM output/Tray close output
16	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator
17	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
18	FG	GPIO2	Analog	1) Motor Hall sensor input 2) GPIO2
19	USB_DP		Analog Inout	USB port DPLUS analog pin
20	USB_DM		Analog Inout	USB port DMINUS analog pin
21	VDD33_USB		USB Power	USB Power pin 3.3V
22	PAD_VRT	GPIO37	Analog	1) USB generating reference current 2) GPIO37
23	VDD12_USB		USB Power	USB Power pin 1.2V
82	EXT_RES		Analog Input	EXTERNAL RESISTER FOR HDMI™ TX
83	AVDD33_12		Analog Power	3.3V VDD FOR HDMI™ TX
84	TXCN		Analog Output	Negative TX CLK
85	TXCP		Analog Output	Postive TX CLK
86	AVDD12_C		Analog Power	1.2V VDD FOR HDMI™ TX
87	TX0N		Analog Output	Negative TX CH0
88	TX0P		Analog Output	Postive TX CH0
89	ASS12		Analog Power	1.2V GND FOR HDMI™ TX
90	TX1N		Analog Output	Negative TX CH1
91	TX1P		Analog Output	Postive TX CH1
92	AVDD12_L		Analog Power	1.2V VDD FOR HDMI™ TX
93	TX2N		Analog Output	Negative TX CH2
94	TX2P		Analog Output	Postive TX CH2
95	DACVDDC		Power	3.3V power pin for video DAC circuitry
96	VREF	GPO14	Analog	1) Bandgap reference voltage 2) GPO14
97	FS		Analog	Full scale adjustment (suggest to use 560 ohm)
98	CVBS		Analog	Analog CVBS or C
99	DACVDDB		Power	3.3V power pin for video DAC circuitry
100	Y/G		Analog	Green, Y, SY, or CVBS
101	B/CB/PB		Analog	Blue, CB/PB, or SC

Pin	Main	Alt.	Type	Description
102	R/CR/PR		Analog	Red, CR/PR, CVBS, or SY
103	AKIN2	GPIO19	Analog	1) Y5 2) HSYN/VSYN output 3) Audio Mute 4) SPDIF 5) MCDATA 6) GPIO19
104	ADVCM	GPIO20	Analog	1) Y6 2) HPLG 3) GPIO20
105	AKIN1	GPIO21	Analog	1) Y7 2) HSYN/VSYN output 3) Audio Mute 4) ASDATA3 5) GPIO21
106	AADVDD		Power	3.3V power pin for 2ch audio ADC circuitry
107	APLLVDD_ GPIO	GPIO34	Analog	1) 3.3V Power pin for audio clock circuitry 2) SPDIF out(8SG) 3) GPIO34 4) SPDIF output3
108	PAPLLCAP	GPIO35	Analog	1) AF1 L external capacitance connection 2) GPIO35
109	LFE	GPIO	Analog Output	1) ACLK 2) GPIO_LFE
110	ARS	GPIO	Analog Output	1) ABCK 2) GPIO_ARS
111	AR	GPIO0	Analog Output	1) RXD2 2) ASDATA2 3) GPIO_AR
112	AVCM		Analog	Audio DAC reference voltage
113	AL	GPIO	Analog Output	1) TXD2 2) ASDATA1 3) GPIO_AL
114	ALS	GPIO	Analog Output	1) ALRCK 2) GPIO_ALS
115	CENTER	GPIO	Analog Output	1) Audio Mute 2) ASDATA0 3) GPIO_CENTER
116	ALACVDD1		Analog Power	3.3V power pin for audio DAC circuitry
117	ADACVDD2		Analog Power	3.3V power pin for audio DAC circuitry
118	AVDD12		Analog Power	Analog 1.2V power
General Power (4)				
52, 79	DVDD12		Power	1.2V power pin for internal digital circuitry
40, 71	DVDD33		Power	3.3V power pin for internal digital circuitry

Pin	Main	Alt.	Type	Description
Micro Controller , Flash Interface and GPIO(11)				
34	GPIO3	INT_	InOut 8mA, SR SMT	1) INT_ 2) MS_CLK set B 3) Microcontroller port 3-1 (Internal Pull-Up) 4) iPod_TXD 5) GPIO3 6) CEC
35	GPIO4		InOut 4mA, PD	1) MS_BS set B 2) ASDATA0 3) ALRCK 4) Microcontroller port 3-4 (Internal Pull-Up) 5) GPIO4
31	GPIO6		InOut 4mA, PU	1) TXD1 2) Y3 3) SD_CLK set B 4) MS_D0 set B 5) ASDATA2 6) Microcontroller port 3-5 (Internal Pull-Up) 7) GPIO6
24	SF_CS_		InOut 8mA, SR PU, SMT	1) Serial Flash Chip Select 2) Trap value in power-on reset : 1 : Serial Flash ATMEL mode 0 : Serial ST/SST mode
25	SF_DO		InOut 8mA, SR PD, SMT	Serial Flash Dout
26	SF_DI		InOut 8mA, SR PU, SMT	1) Serial Flash Din 2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
27	SF_CK		InOut 8mA, SR PD, SMT	Serial Flash Clock
28	UP1_6	SCL	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-6 2) RXD3 3) DDC 4) I2C SCK
29	UP1_7	SDA	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-7 2) TXD3 3) DDC 4) I2C SDA
32	PRST_		Input 4mA, SR PU, SMT	Power on reset input, active low
33	IR	GPI	Input 4mA, SR SMT	1) IR control signal input 2) GPI
Dram Interface (37) (Sorted by position)				

Pin	Main	Alt.	Type	Description
41	RD0		InOut, 2mA	DRAM data 0
42	RD1		InOut 2mA	DRAM data 1
43	RD2		InOut 2mA	DRAM data 2
44	RD3		InOut 2mA	DRAM data 3
45	RD4		InOut 2mA	DRAM data 4
46	RD5		InOut 2mA	DRAM data 5
47	RD6		InOut 2mA	DRAM data 6
48	RD7		InOut 2mA	DRAM data 7
49	DQM0		InOut 2mA, PD	Data mask 0
50	RD15		InOut 2mA	DRAM data 15
51	RD14		InOut 2mA	DRAM data 14
53	RD13		InOut 2mA	DRAM data 13
54	RD12		InOut 2mA	DRAM data 12
55	RD11		InOut 2mA	DRAM data 11
56	RD10		InOut 2mA	DRAM data 10
57	RD9		InOut 2mA	DRAM data 9
58	RD8		InOut 2mA	DRAM data 8
59	DQM1		InOut 2mA, PD	Data mask 1
60	RCLK		InOut 4mA, PD	Dram clock
61	RA11		InOut 2mA, PD	DRAM address bit 11
62	RA9		InOut 2mA, PD	DRAM address 9
63	RA8		InOut 2mA, PD	DRAM address 8
64	RA7		InOut 2mA, PD	DRAM address 7
65	RA6		InOut 2mA, PD	DRAM address 6
66	RA5		InOut 2mA, PD	DRAM address 5

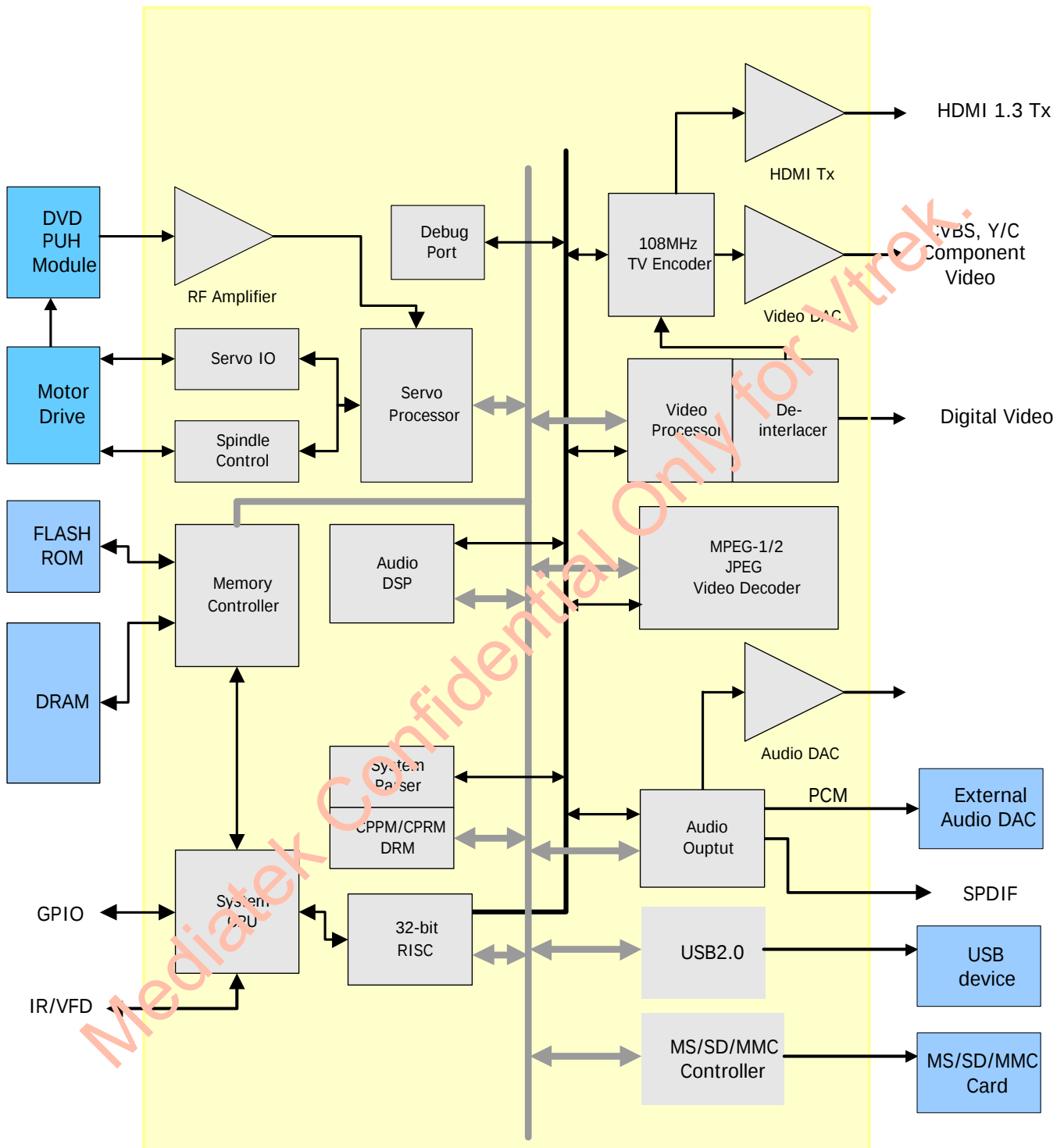
Pin	Main	Alt.	Type	Description
67	RA4		InOut 2mA, PD	DRAM address 4
68	RWE		Output 2mA, PD	DRAM Write enable, active low
69	CAS		Output 2mA, PD	DRAM column address strobe, active low
70	RAS		Output 2mA, PD	DRAM row address strobe, active low
72	BA0		InOut 2mA, PD	DRAM bank address 0
73	BA1		InOut 2mA, PD	DRAM bank address 1
74	RA10		InOut 2mA, PD	DRAM address 10
75	RA0		InOut 2mA, PD	DRAM address 0
76	RA1		InOut 2mA, PD	DRAM address 1
77	RA2		InOut 2mA, PD	DRAM address 2
78	RA3		InOut 2mA, PD	DRAM address 3
39	GPIO7	CKE_	InOut 4mA, PD	1) Y1 2) HSYN/VSYN output 3) HSYN/VSYN input 4) SD_CLK set A 5) MS_CLK set A 6) ACLK 7) ASDATA1 8) MCDATA 9) CEC 10) Microcontroller port 1-4 (Internal Pull-Up) 11) GPIO7
GPIO (6)				
38	GPIO8		InOut 4mA, PD	1) Y1 2) HSYN/VSYN output 3) HSYN/VSYN input 4) SD_CMD set A 5) MS_BS set A 6) ASDATA2 7) ACLK 8) Audio Mute 9) MCDATA 10) DDC 11) Microcontroller port 1-5 (Internal Pull-Up) 12) GPIO8

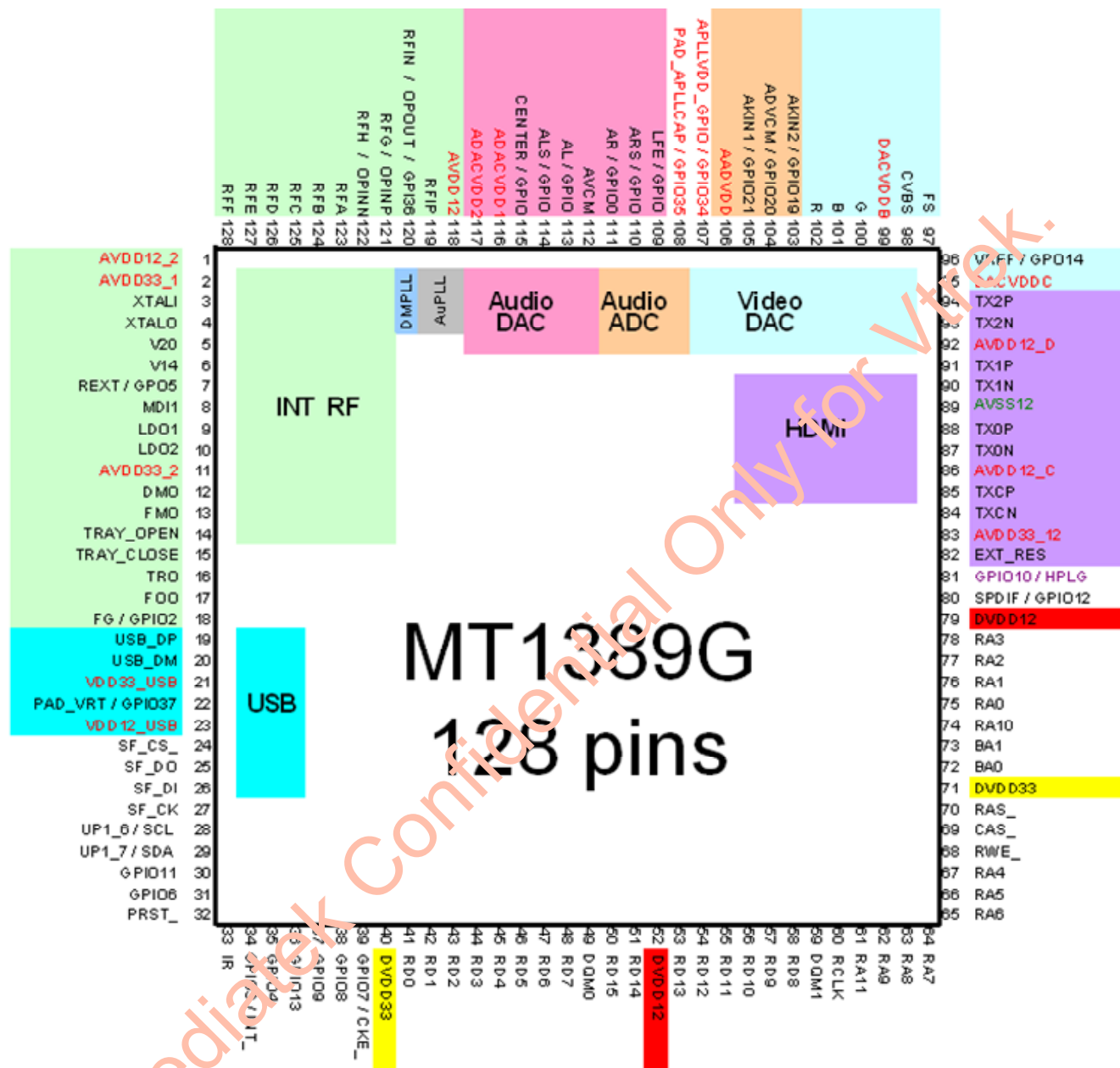
Pin	Main	Alt.	Type	Description
37	GPIO9		InOut 4mA, PD	1) Y2 2) SD_DATA set A 3) MS_D0 set A 4) ASDATA1 5) ABCK 6) DDC 7) GPIO9
81	GPIO10	HPLG	InOut 4mA, PD	1) DDC 2) GPIO10
30	GPIO11		InOut 4mA	1) RXD1 2) Y4 3) HSYN/VSYN output 4) SD_CMD set B 5) ABCK 6) ASDATA0 7) Audio Mute 8) CEC 9) DDC 10) Microcontroller port 3-0 (Internal Pull-Up) 11) iPod_RXD 12) GPIO11
80	SPDIF	GPIO12	InOut 2mA, PD	1) SPDIF output 2) GPIO12
36	GPIO13		InOut 4mA, PD	1) YCLK 2) SD_D0 set B 3) ALRCK 4) Audio Mute 5) GPIO13

Note:

1. The Main column is the main function, Alt. means alternative function.

5-5 Functional Block





7 Absolute Maximum Ratings

Symbol	Parameters	Suggest Value	Unit
VDD3	3.3V Supply voltage	-0.2 to 3.6	V
VDD2	1.2V Supply voltage	-0.1 to 1.3	V
VDDA	Analog Supply voltage	-0.2 to 3.6	V
V _{IN} (3.3V)	Input Voltage (3.3V IO)	-0.2 to 3.6	V
V _{IN} (5V-tolerance)	Input Voltage (5V-tolerance IO)	-0.3 to 5.5	V
V _{OUT}	Output Voltage	-0.2 to VDD3+0.3	V
T _{STG}	Storage Temperature	-45 to 150	°C

8 Recommend Operation Condition

Symbol	Parameters	Min	Typ	Max	Unit
T _{OP}	Operating Temperature	0		70	°C
T _J	Junction Operation Temp.	0	25	115	°C
VDD3	3.3V Supply voltage	3.1	3.3	3.6	V
VDD2	1.2V Supply voltage	1.1	1.2	1.3	V
VDDA	Analog Supply voltage	3.1	3.3	3.6	V
V _{IH} (3.3V)	Input voltage high (3.3V IO)	2.0	-	-	V
V _{IL} (3.3V)	Input voltage low (3.3V IO)	-	-	0.8	V
I _{IH}	High level input current			10	UA
I _{IL}	Low level input current	-10			UA
P _D	Power dissipation		1.5		W
P _{DOWN}	Power down mode			0.1	W
f _{clk}	Input frequency of clock		27		MHz

9 Electrical Characteristics

9-1 DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V _{OH} (3.3V)	Output voltage high (3.3V IO) (*I _{OH} = 2 ~ 16mA)	2.4	-	-	V
V _{OL} (3.3V)	Output voltage low (3.3V IO) (*I _{OL} = 2 ~ 16mA)	-	-	0.4	V
R _{pu}	Pull-up Resistance	40	75	190	KΩ
R _{pd}	Pull-down Resistance	40	75	190	KΩ
FOO _{OFF}	Offset voltage between FOO zero output and V _{REF}	-50	0	50	mV
TRO _{OFF}	Offset voltage between TRO zero output and V _{REF}	-40	0	40	mV
DMO _{OFF}	Offset voltage between DMO zero output and V _{REF}	-30	0	30	mV

Note * : The driving current of some IO pad are programmable according to the different application and environment . All setting will be defined according to the F/W progress and test result.

9-2 Built-in Audio-DAC Characteristics

Note *: All parameters is measured on MediaTek's DVD player reference DVD board, the actual performance depends on different PCB design.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{out}	Output swing level: Digital i/p level =0 dBFS , ADAC VDD =3.3V (V _{out} = 1.0 * ADAC VDD / 3.3)	0.9	1.0	1.1	V _P
R _o	Output impedance @ 1kHz		50	100	Ω
R _{L_min}	Minimum resistor load	5			K
C _{L_max}	Maximum capacitor load			20	PF
S/(THD+N)	S/(THD+N) @ 0 dBFS; f _{in} = 1kHz; Fs = 48kHz, A-weighted		81		dBr(A)
DR	Dynamic Range		82		dBr(A)
SNR	Signal to noise ratio; A-weighted		92		dBr(A)
Channel Separation	Close-talk of Left and Right Channel		81		dB

9-3 Built-in Audio-ADC Characteristics

Test signal : 1K Hz sin wave	Vpp(V)	
Max Input (with output THD+N <60 dbfs)	3.227V	59.9dBFS
DC bias level	1.66V	
AKIN DC Level	1.632V	
Test signal : 1K Hz sin wave		
Input (Vpp)	Output THD+N(dBFs)	filter=A-weighting
3V	-62.27	
2.95	-63.9	
2.9	-65.7	
2.828V	-67.7	
2.75V	-69.9	
2.5V	-75.4	
1.5V	-81.9	
0.5V	-84.9	
0V (remove input and short ADVCM with AKIN)	-135.9	
Test signal : 2.8 Vpp		
Input frequency:	Amp(dBFS)	filter=none
1 KHz	-0.422	
4KHz	-0.447	
8khz	-0.518	
16KHz	-0.791	
20KHz	-1.822	
22KHz	-6.848	
Dynamic range	283mVpp	

9-4 Built-in Video-DAC Specifications

Input Codes for Video Application:

	NTSC	NTSC w/setup	525_I	525_I w/setup	525_P
WHITE (235)	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3290
BLACK (16)	960	1120	960	1120	1008
PEDESTAL	960	960	960	960	1008
SYNC TIP	64	64	64	64	64

	525_P w/s	PAL	625_I	625_P	RGB
WHITE (235)	---	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 2282
BLACK (16)	---	1008	1008	1008	0
PEDESTAL	---	1008	1008	1008	-
SYNC TIP	---	64	64	64	-

9-5 Video Output Voltage Level:

High / Low Impedance Mode:

Please contact with FW window for setting High / Low impedance mode.

9-6 Video DAC DC Electrical Characteristics

(Operating Free-Air Temperature, AVDD 3.3V, DVDD = 3.3V).

Analog Output	MIN	TYP	MAX	UNIT
Full Scale Output Current CVBS/Y/C/R/G/B (low impedance mode)	34.3	34.8	35.7	mA
Full Scale Output Current CVBS/Y/C/R/G/B (high impedance mode)	8.52	8.70	8.91	mA
LSB current CVBS/Y/C/R/G/B (low impedance mode)	33.5	34.0	34.86	uA
LSB current CVBS/Y/C/R/G/B (high impedance mode)	8.375	8.500	8.715	uA
DAC-to-DAC Mis-Matching	--	1.48	--	%
Output Compliance	0	--	1.38	V
DAC Output Delay	--	1.5	10	ns
DAC Rise/Fall Time	--	2.1	5	
Voltage Reference				
Reference Voltage Output		1.22		V
Reference Input Current		2.179		MA
Static Performance				

DAC Resolution	12			Bits
DNL Differential Non-Linearity	+/-0.26	+/-0.48	+/-0.6	LSB
INL Integral Non-Linearity	+/-0.40	+/-0.67	*/-0.9	LSB
Dynamic Performance				
Differential Gain		0.77	1.5	%
Differential Phase		0.23	1.5	°
S/N Ratio	70			dB
Power Supply				
Supply Voltage	3.0	3.3	3.6	V

9-7 RF specification

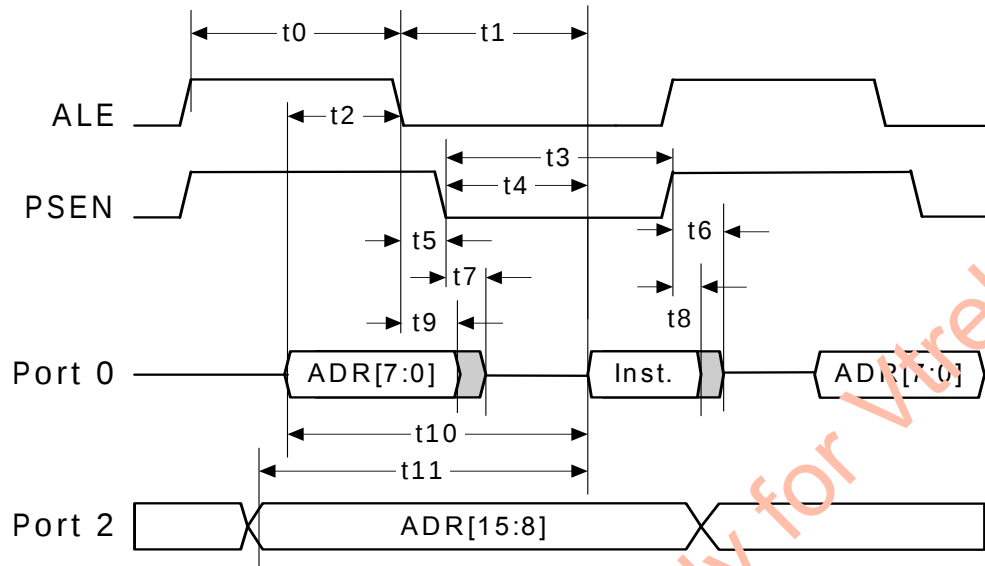
Item	Designator	Conditions	Min	Typ	Max	Unit
3.3V POWER			3.00	3.30	3.60	Volts
Power Down Mode		Enable power down	10	27	50	mA
		Chip Reset	90	151	200	mA
Reference Voltage	V20	Force current =0A	1.85	1.99	2.15	Volts
Reference Voltage	V14	Force current =0A	1.25	1.39	1.55	Volts
APC1(CD)	MDI1	0Ah=10 ;APC1 on MDI1=180mV	166	184	202	mV
	LDO1	0Ah=00 ;APC1 off	3.00	3.28		V
	MDI1→LDO1	0Ah=10; APC1 on	212	254	295	V/V
APC2(DVD)	MDI2	0Bh=10 ;APC2 on MDI2=180mV	166	184	202	mV
	LDO2	0Bh=00 ;APC2 off	3.00	3.28		V
	MDI2→LDO2	0Bh=10; APC2 on High gain	210	265	298	V/V
Focusing Error Gain	MA → FEO	05h=30; low gain With 10KHz Sin Input	7.5	10.3	11.5	dB
Focusing Error Frequency Response	MA → FEO	05h=7C; low gain With 10KHz, 300KHz Sin Input R=G(10KHz)-G(300KHz)	16	23.9		dB
Focusing Error Common Mode Gain	MA → FEO MB → FEO	05h=3F; low gain With 10KHz Sin Input		-34	-20	dB

Item	Designator	Conditions	Min	Typ	Max	Unit
Focusing Error H/L Gain	MA → FEO	Toggle 05h bit5 : FELG With 10KHz Sin Input	2.75	2.99	3.25	V/V
Focusing Error offset Adjustment step	Input Floating Measure FEO	Toggle 4Dh : FEOS[6:0]	65	103	140	mV
Focusing Error THD	MA → FEO	05h= 7C ; low gain With 10KHz Sin Input	30	54		dB
Central Servo Gain	MA → CSO	06h= F0 ; low gain With 10KHz Sin Input	12.5	14.1	15.5	dB
Central Servo Frequency Response	MA → CSO	06h= FF ; low gain With 10KHz, 300KHz Sin Input $R=G(10kHz)-G(300Khz)$	14	21.4		dB
Central Servo Common Mode Gain	MA → CSO MB → CSO	06h= F0 ; low gain With 10KHz Sin Input		-30	-10	dB
Central Servo H/L Gain	MA → CSO	Toggle 06h bit5 : CSOLG With 10KHz Sin Input	2.75	2.97	3.25	V/V
Central Servo offset Adjustment step	Input Floating Measure CSO	Toggle 4Eh : CSOOS[6:0]	65	108	140	mV
Central Servo THD	MA → CSO	06h= F0 ; low gain With 10KHz Sin Input	30	53		dB
Tracking Error Gain	MA → TEO	07h= 70 ; low gain With 10KHz Sin Input	13	15	17	dB
Tracking Error Frequency Response	MA → TEO	07h= 70 ; low gain With 10KHz, 300KHz Sin Input $R=G(10kHz)-G(300Khz)$	16	24.2		dB
Tracking Error Common Mode Gain	MA → TEO MB → TEO	07h= 7F ; low gain With 10KHz Sin Input		-22	-10	dB
Tracking Error H/L Gain	MA → TEO	Toggle 07h bit6, 5 With 10KHz Sin Input	4	5.8	8	V/V
Tracking Error offset Adjustment step	Input Floating Measure TEO	Toggle 4Fh : TEOS[6:0]	65	110	140	mV

Item	Designator	Conditions	Min	Typ	Max	Unit
Tracking Error THD	MA → TEO	07h=7F; low gain With 10KHz Sin Input	30	42		dB
RFL Gain	MA → LVL	08h=60; low gain With 10KHz Sin Input	-6.5	-4.6	-3.5	dB
RFL Frequency Response	MA → LVL	08h=7F; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300KHz)	14	22.7		dB
RFL H/L Gain I	MA → LVL	Toggle 09h bit1 : LVLATN With 10KHz Sin Input	0.3	0.52	0.7	V/V
RFL H/L Gain II	SA → LVL	Toggle 09h bit2 : SBADHG With 10KHz Sin Input	2.5	2.77	3.1	V/V
RFL offset Adjustment step	Input Floating Measure LVL	Toggle 50h : LVLOS[6:0]	65	113	140	mV
RFL THD	MA → LVL	08h=7F; low gain With 10KHz Sin Input	30	44		dB

9-8 Micro Controller Interface

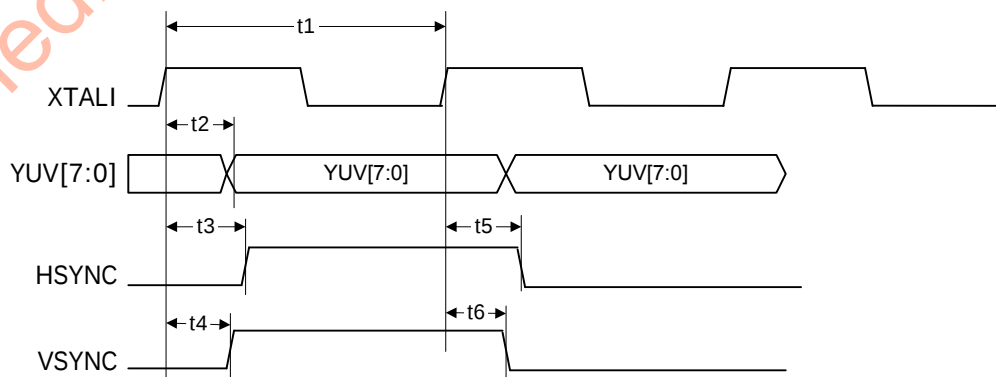
Parameter	Symbol	Min.	Max.	Units
Oscillator Frequency	1/Tf	0	23.3	MHz
ALE Pulse Width	T0	1.5Tf-5		ns
ALE Low to Valid Instruction	T1		2.5Tf-20	ns
ALE Low to PSEN Low	T5	0.5Tf-5		ns
Address Valid to ALE Low	T2	0.5Tf-5		ns
Address Hold After ALE Low	T9	0.5Tf-5		ns
PSEN Pulse Width	T3	2.0Tf-5		ns
PSEN Low to Valid Instruction	T4		2.0Tf-20	ns
Input Instruction Hold After PSEN high	T8	0		ns
Input Instruction Float After PSEN high	T6		1.0Tf-5	ns
Port 0 Address to Valid Instruction	T10		3.0Tf-20	ns
Port 2 Address to Valid Instruction	T11		3.5Tf-20	ns
PSEN Low to Address Float	T7		0	ns



Program Memory Read Cycle Timing Diagram

9-9 Digital Video Output Interface

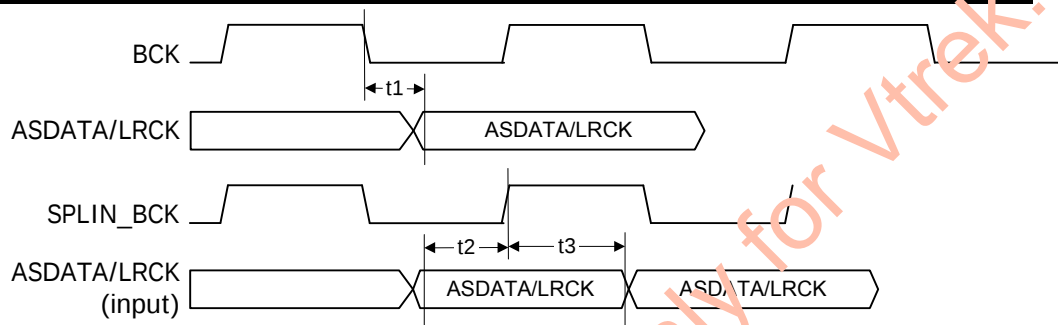
Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/T1		27		MHz
YUV digital output delay	T2			15	ns
HSYNC Rising delay	T3			15	ns
VSYNC Rising delay	T4			15	ns
HSYNC Falling delay	T5			20	ns
VSYNC Falling delay	T6			20	ns



Digital Video Output Interface Timing Diagram

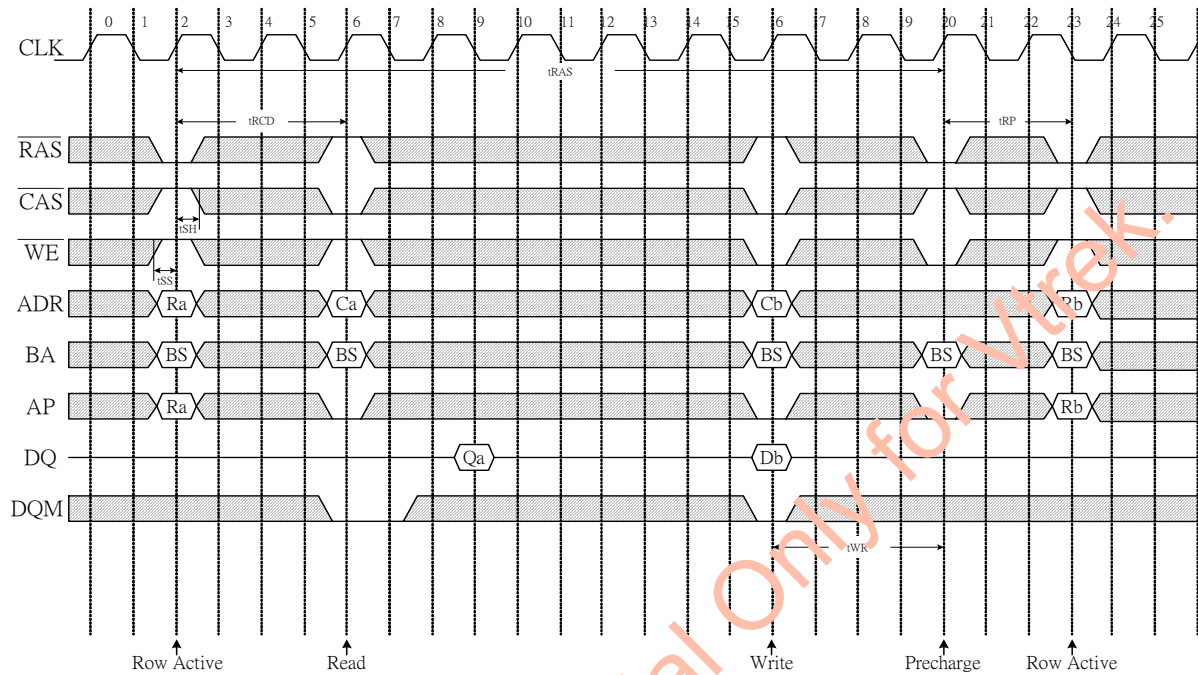
9-10 SPDIF I/O Interface

Parameter	Symbol	Min	Typ	Max	Units
BCK negative edge to ASDATA valid	T1	1.0		3.0	ns
ASDATA/LRCK input setup	T2			3.0	ns
ASDATA/LRCK input hold	T3	1.2			ns



SPDIF Input/Output Timing Diagram

9-11 DRAM Interface



Parameter		Symbol	-6		-7		-75		Units
			Min	Max	Min	Max	Min	Max	
CLK cycle time	CAS latency = 3	tCC	7.5	-	7.5	-	7.5	-	ns
SDRAM input setup time		tSS	1.5		1.75		1.75		ns
SDRAM input hold time		tSH	1		1		1		ns
Active to Precharge command period		tRAS	42	100K	49	100K	52	100K	ns
Precharge to Active command period		tRP	18		20		20		ns
Active to read/write command delay		tRCD	18		20		20		ns
Write recovery time	CL = 3	tWR	6		7		7.5		ns

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

-6T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		42ns	18ns	18ns	6ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	2	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		49ns	20ns	20ns	7ns/10ns
133MHz (7.5ns)	3	7	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7.5T

(Unit: number of clock)

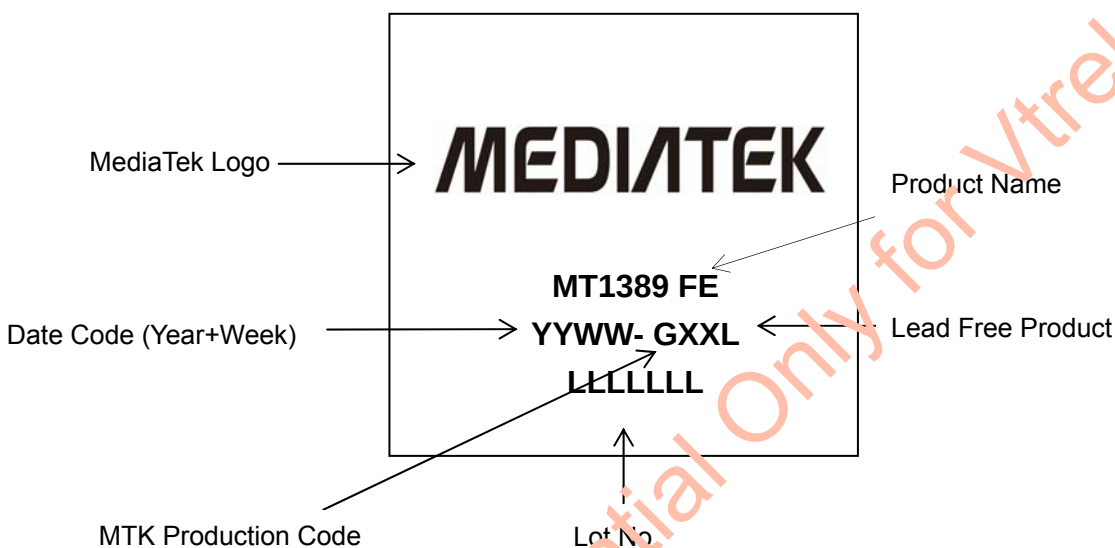
Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		45ns	20ns	20ns	7.5ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-8T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		48ns	20ns	20ns	8ns/10ns
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	3	5	2	2	1

10 Marking on Devices

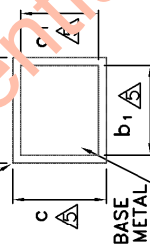
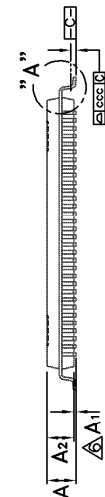
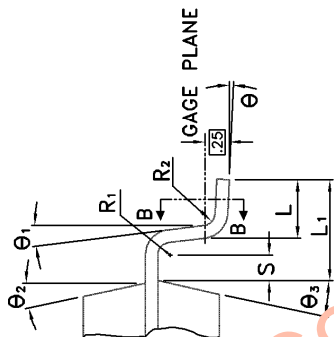
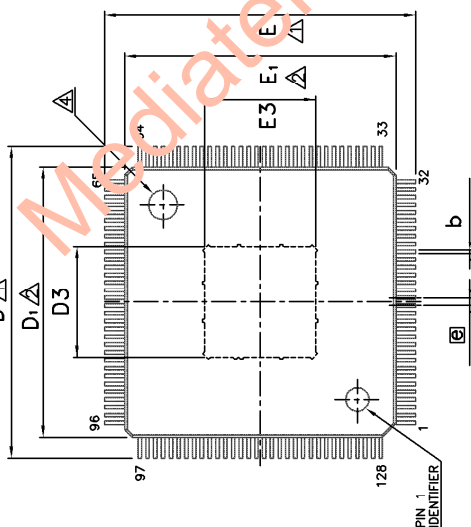


11 Package Description

11-1 Package Outline Dimension

The bend lead are controlled under the criteria 0.075mm (2.5mil).

Symbol	Dimension in mm		Dimension in inch	
	Min	Max	Min	Max
A	—	1.60	—	0.063
A ₁	0.05	—	0.002	—
A ₂	1.35	1.40	0.053	0.055
b	0.13	0.18	0.005	0.007
b ₁	0.13	0.16	0.005	0.006
c	0.09	—	0.004	—
c ₁	0.09	—	0.004	—
D	15.85	16.00	0.624	0.630
D ₁	13.90	14.00	0.547	0.551
E	15.85	16.00	0.624	0.630
E ₁	13.90	14.00	0.547	0.551
⓪	0.40	BSC	0.016	BSC
L	0.45	0.60	0.018	0.024
L ₁	1.00	REF	0.039	REF
R ₁	0.08	—	0.003	—
R ₂	0.08	—	0.003	—
S	0.20	—	0.008	—
θ	0°	3.5°	0°	3.5°
θ ₁	0°	—	0°	—
θ ₂	12° TYP	—	12° TYP	—
θ ₃	12° TYP	—	12° TYP	—
ccc	0.08	—	0.003	—



SECTION B-B

- NOTE :
- △ TO BE DETERMINED AT SEATING PLANE $\square\square$.
 - △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
 - △ DAMBAR DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
 - △ EXACT SHAPE OF EACH CORNER IS OPTIONAL.
 - △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
 - △ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
 - 7. CONTROLLING DIMENSION : MILLIMETER.
 - 8. REFERENCE DOCUMENT : JEDEC MS-026.
 - 9. SPECIAL CHARACTERISTICS C CLASS: ccc

TITLE: 128LD E-PAD LQFP (14x14x1.4mm) PACKAGE OUTLINE
Cu L/F, FOOTPRINT 2.0mm

L/F MATERIAL: C7025 1/2H

L/F	Exposed Pad Size	Dimension in mm	Dimension in inch
① D3/E3	3.61 REF	—	0.142 REF
② D3/E3	5.72 REF	—	0.225 REF
③ D3/E3	8.00 REF	—	0.315 REF
④ D3/E3	7.75 / 6.60 REF	0.305 / 0.260 REF	—

APPR. DWG NO. DB128-SW1

ENG. REV NO. C

Q.M. PRODUCT CODE DB1283C

CHK. DATE 09/07/07

DWG. Mechane SieChang SH NO. 1/1

SILICONWARE PRECISION INDUSTRIES CO., LTD.

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
C	Add exposed pad size ⓪	09/07/07

11-2 Weight of the chip

0.65g

11-3 Material and Finish of Lead Terminals

For Lead-free Package, Materials of terminal is Sn(98%) and Bi (2%) and thickness is 300~600u inch, similar as SnPb.

11-4 Package Material

Lead frame: Cu

Epoxy: 1033BF

Molding compound: G700

12 Packing Description

Package	Pin / Ball count	EA / Tray	Tray / Box	Full Box Q'ty	Box / Carton	Full carton Q'ty
LQFP	128	90	10	900	6	5400

12-1 Tray Description

90ea/ Hard Tray (150°C resistance).



12-2 Desiccants

Size: 130*80 mm.

Weight: 20g

12-3 Aluminum Foil Bag

Size: 250*500 mm.

Thickness: 0.12 +/- 0.005 mm.

Surface impedance: 10^8 - 10^{12} Ohm/SQ

12-4 Box Description

Material: 3 Layer B corrugated paper.

Strength: 1176000 PA.

Box size: 355(L)*157(W)*90.5(H) mm.

Printing: Black (words, warning, index)

12-5 Side Plank

Material: 5 Layer AB corrugated paper

Strength: 1793400 PA.

Size: 405(L)*237(W) mm.

Fixture: 3 pieces of EPE (recyclable material).

Thickness: 20 mm.

12-6 Carton Description

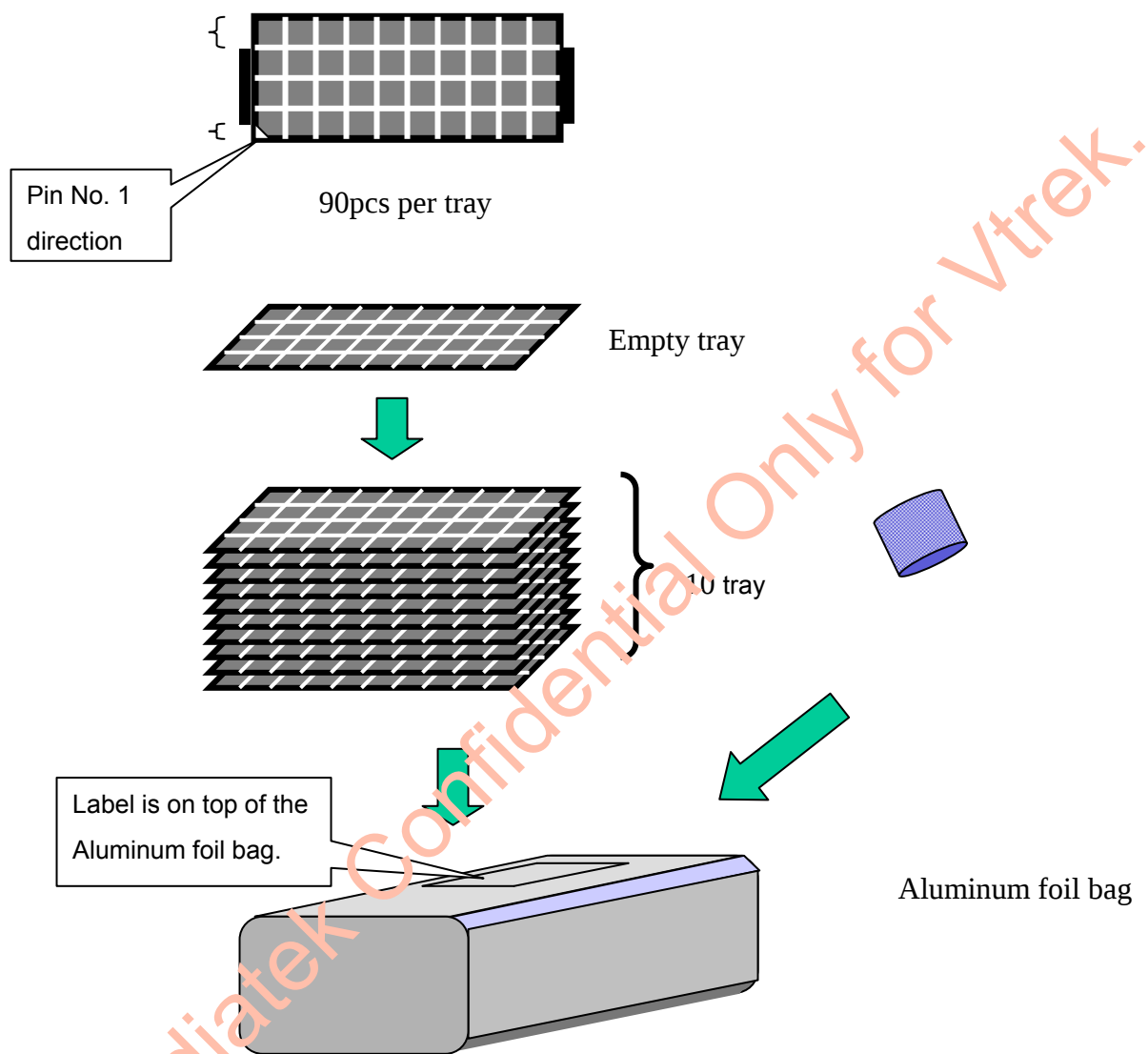
Material: 5 Layer AB corrugated paper.

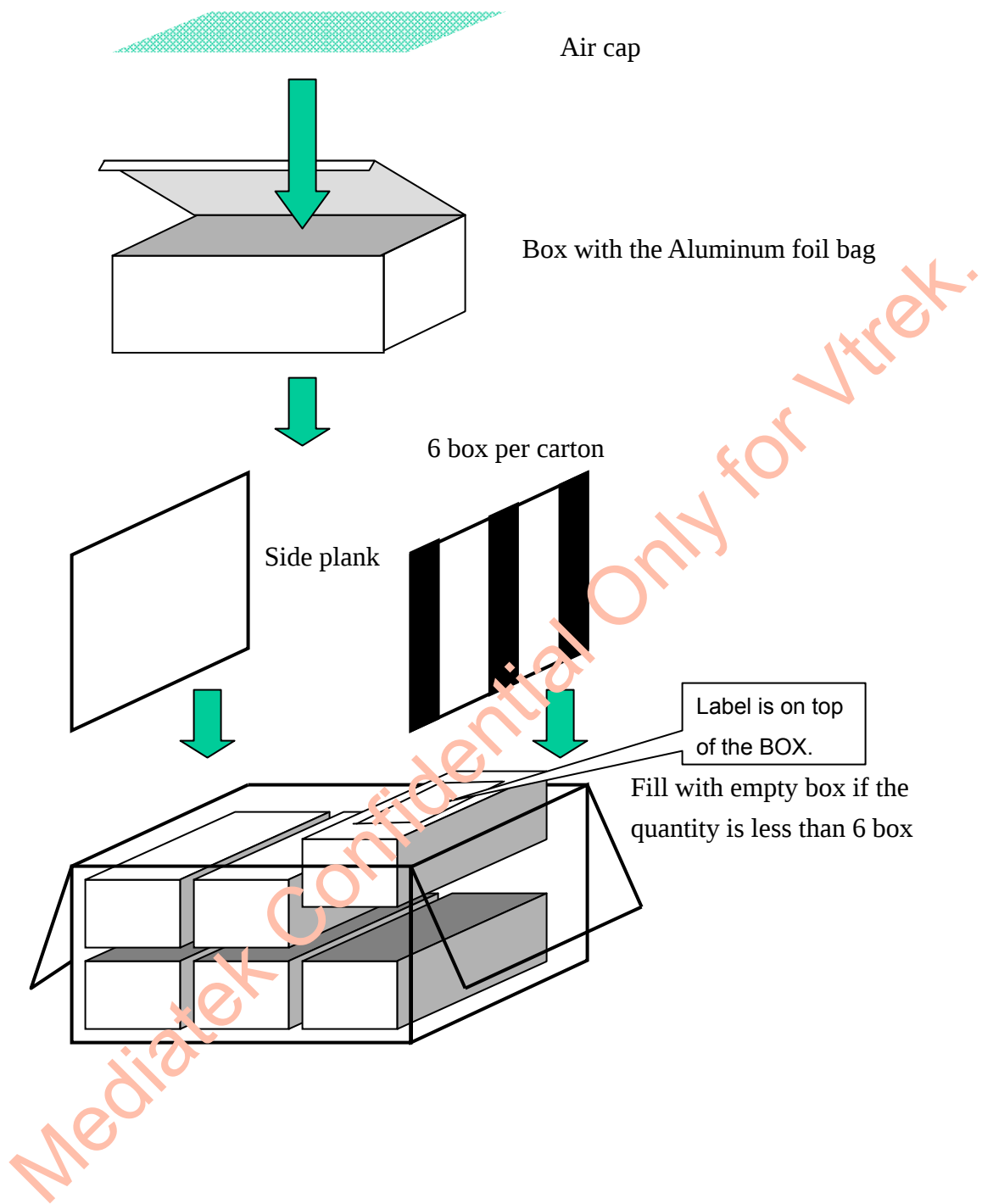
Strength: 1793400 PA.

Carton size: 558(L)*428(W)*264(H) mm.

Printing: Black (words, warning, index)

12-7 Packing Flow





13 Solder-Reflow Condition

13-1 Reflow Condition

MediaTek can guarantee 3 times IR reflow based on the reflow profile (Figure 1).

Average ramp-up rate (T_s to peak): 3 °C /sec. max.

Preheat & Soak: Pb-Free 150~200 °C (SnPb Eutectic 100~150 °C) for 60~120 seconds

Liquidous temperature maintained above Pb-Free 217 °C (SnPb Eutectic 183 °C) for 60~150 seconds

Time within 5 °C of specified classification temperature: Pb-Free 30 seconds (SnPb Eutectic 20 seconds)

Note:

Reflow profiles in this document are for classification/preconditioning and **are not meant to specify board assembly profiles**. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 1.

For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Peak temperature: Defined in Table 2-1 and Table 2-2.

Ramp-down rate: 6 °C /sec. max

Time 25 °C to peak temperature: Pb-Free: 8 minutes max. (SnPb Eutectic 6 minutes max.)

Time between reflow: 5 minutes minimum and 60 minutes maximum

Table 1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 2-1 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

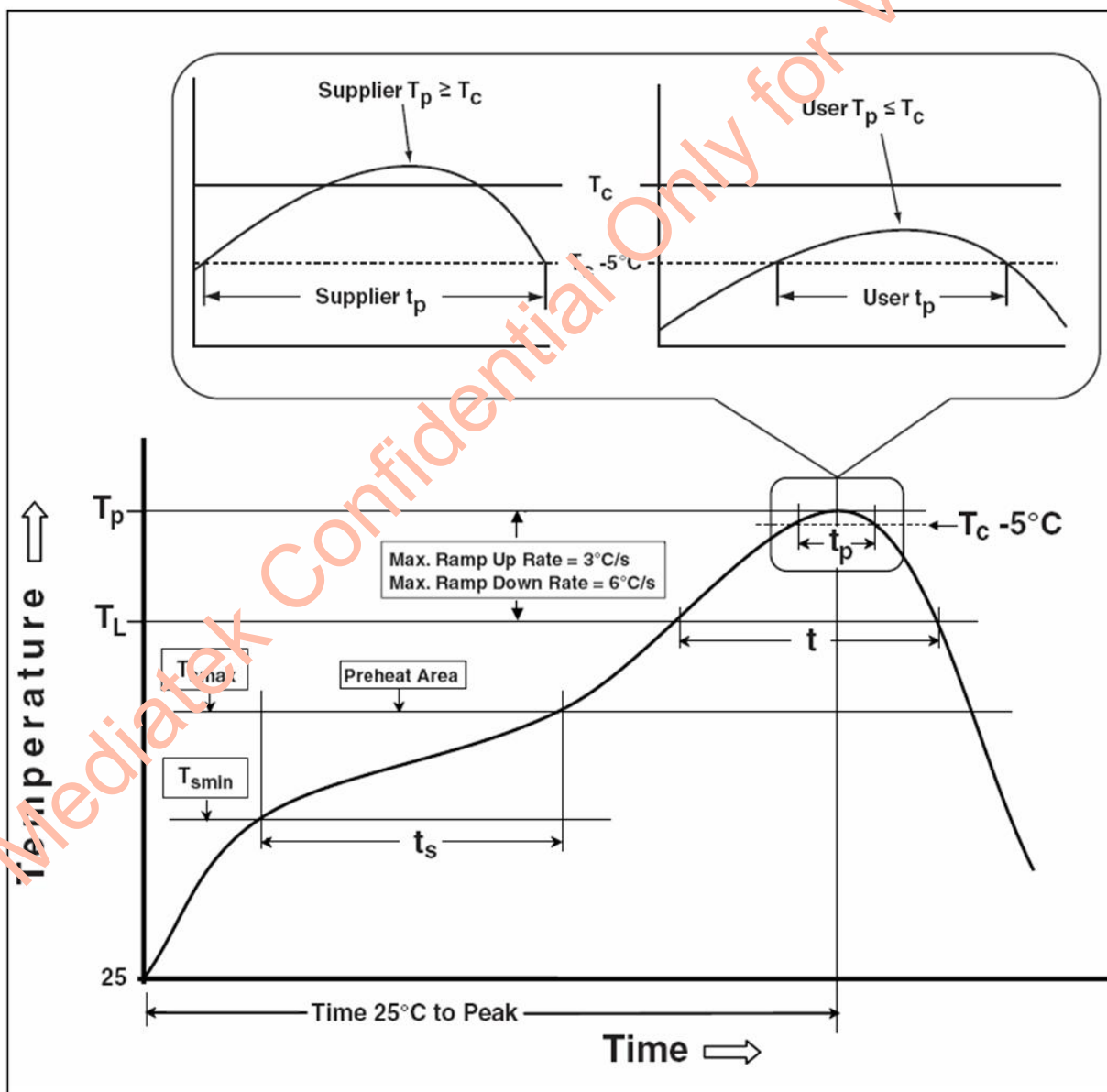


Figure 1 Classification Profile

13-2 Pre-process and Heat Treatment

Procedure: (MRT L3)

[Package opening] → [Baking] → [Humidification] → [Reflow]

A. Conditions between each step of procedure

Be lift for duration of 2 hours or longer at temperature of 30 °C or lower and a humidity of 60% R.H. or lower.

B. Baking 125 °C, 24 hours.

C. Humidification: 30 °C, 60% R.H., 192 Hours

D. Reflow: 3 x 260 °C

14 Manual Solder Condition

The specimen should be in the as-delivered condition. Set the soldering iron at a temperature of 300 +/- 10 °C (at the iron bit). Place the iron and flux-cored solder in parallel with each and every terminal/lead on the back of the board for a duration which does not exceed 5 seconds without applying any mechanical stress on the component body.

It can also be applied under 350 +/- 10 °C at the iron bit within 3 seconds, please treat it carefully under such condition.

The chip can't do DIP soldering.

15 Storage Condition

15-1 Storage Duration

A. Notice the Sealing time.

B. 12 monthly and storage condition: <= 40°C , <= 90% R.H.

C. Warehouse control: First in and First out.

15-2 After Open the Bag

A. SMT: Should finish the SMT process within 168 hours

B. Check the humidity check card: The value should < 20% (blue), if the value >= 30% (red), it means the IC has got moisture.

C. Factory environment control: <= 30°C, <= 60% R.H.

16 Other

If a doubt related to the present specifications arises, the problem will be solved based on discussion between the both parties.

2-1-3 Serial EEPROM, 2K (256 x 8) (24C02) or 16 K (2048 x 8) (24C16)

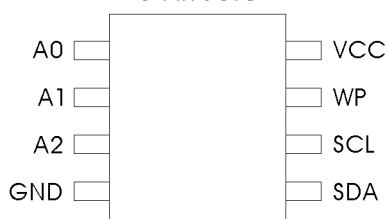
24C02 is used for DVD player while 24C16 is for DVD receiver. The capacity is the only difference between two kinds of serial EEPROM. Both of them use same package and have same pin configuration.

* Features

- Low-Voltage and Standard-Voltage Operation
 - 5.0 (V_{CC} = 4.5V to 5.5V)
 - 2.7 (V_{CC} = 2.7V to 5.5V)
 - 2.5 (V_{CC} = 2.5V to 5.5V)
 - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 100 kHz (1.8v, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
 -
 - ESD Protection: >3000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC, 8-Pin PDIP, 8-Pin MSOP, and 8-Pin TSSOP Packages

* Pin Configurations

8-Pin SOIC



* Pin Description

Pin Name	Function
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock input
WP	Write Protect
NC	No Connect

2-1-4: Boot Sector Flash Memory

A29I 800 Series

1M X 8 Bit / 512K X 16 Bit CMOS 3.0 Volt-only,

Features

- Single power supply operation
 - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- Access times:
 - 70/90 (max.)
- Current:
 - 9 mA typical active read current
 - 20 mA typical program/erase current
 - 200 nA typical CMOS standby
 - 200 nA Automatic Sleep Mode current
- Flexible sector architecture
 - 16 Kbyte/ 8 KbyteX2/ 32 Kbyte/ 64 KbyteX15 sectors
 - 8 Kword/ 4 KwordX2/ 16 Kword/ 32 KwordX15 sectors
 - Any combination of sectors can be erased
 - Supports full chip erase
 - Sector protection:
 - A hardware method of protecting sectors to prevent any inadvertent program or erase operations within that sector. Temporary Sector Unprotect feature allows code changes in previously locked sectors
- Extended operating temperature range: -45°C ~ +85°C for -U series
- Unlock Bypass Program Command
 - Reduces overall programming time when issuing multiple program command sequence
- Top or bottom boot block configurations available
- Embedded Algorithms
 - Embedded Erase algorithm will automatically erase the entire chip or any combination of designated sectors and verify the erased sectors
 - Embedded Program algorithm automatically writes and verifies data at specified addresses
- Typical 100,000 program/erase cycles per sector
- 20-year data retention at 125°C
 - Reliable operation for the life of the system
- Compatible with JEDEC-standards
 - Pinout and software compatible with single-power-supply Flash memory standard
 - Superior inadvertent write protection
- Data Polling and toggle bits
 - Provides a software method of detecting completion of program or erase operations
- Ready / BUSY pin (RY / BY)
 - Provides a hardware method of detecting completion of program or erase operations (not available on 44-pin SOP)
- Erase Suspend/Erase Resume
 - Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation
- Hardware reset pin ($\overline{\text{RESET}}$)
 - Hardware method to reset the device to reading array data
- Package options
 - 44-pin SOP or 48-pin TSOP (I) or 48-ball TFBGA

General Description

The A29L800 is an 8Mbit, 3.0 volt-only Flash memory organized as 1,048,576 bytes of 8 bits or 524,288 words of 16 bits each. The 8 bits of data appear on I/O₀ - I/O₇; the 16 bits of data appear on I/O₀~I/O₁₅. The A29L800 is offered in 48-ball TFBGA, 44-pin SOP and 48-Pin TSOP packages. This device is designed to be programmed in-system with the standard system 3.0 volt VCC supply. Additional 12.0 volt VPP is not required for in-system write or erase operations. However, the A29L800 can also be programmed in standard EPROM programmers.

The A29L800 has the first toggle bit, I/O₆, which indicates whether an Embedded Program or Erase is in progress, or it is in the Erase Suspend. Besides the I/O₆ toggle bit, the A29L800 has a second toggle bit, I/O₂, to indicate whether the addressed sector is being selected for erase. The A29L800 also offers the ability to program in the Erase Suspend mode. The standard A29L800 offers access times of 70 and 90ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The device requires only a single 3.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The A29L800 is entirely software command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by writing the proper program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper program margin.

Device erasure occurs by executing the proper erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper erase margin. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The host system can detect whether a program or erase operation is complete by observing the RY / BY pin, or by reading the I/O₇ ($\overline{Data}$ Polling) and I/O₆ (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The A29L800 is fully erased when shipped from the factory.

The hardware sector protection feature disables operations for both program and erase in any combination of the sectors of memory. This can be achieved via programming equipment.

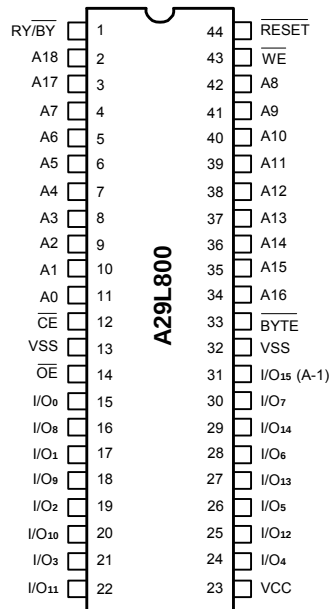
The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any other sector that is not selected for erasure. True background erase can thus be achieved.

The hardware $\overline{RESET}$ pin terminates any operation in progress and resets the internal state machine to reading array data. The $\overline{RESET}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

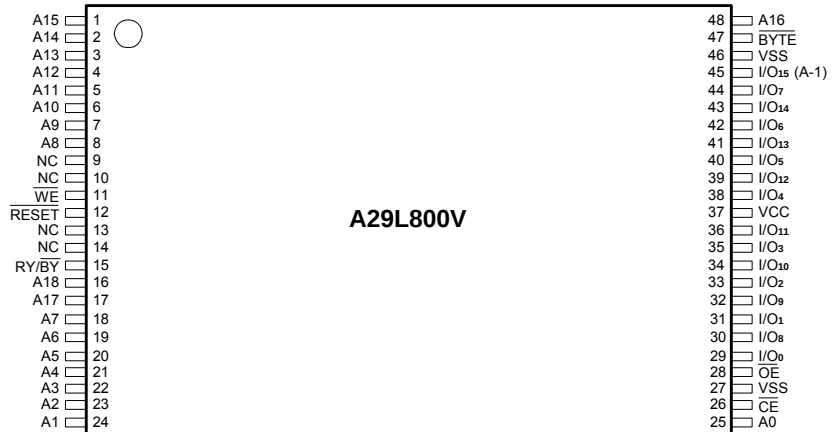
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

Pin Configurations

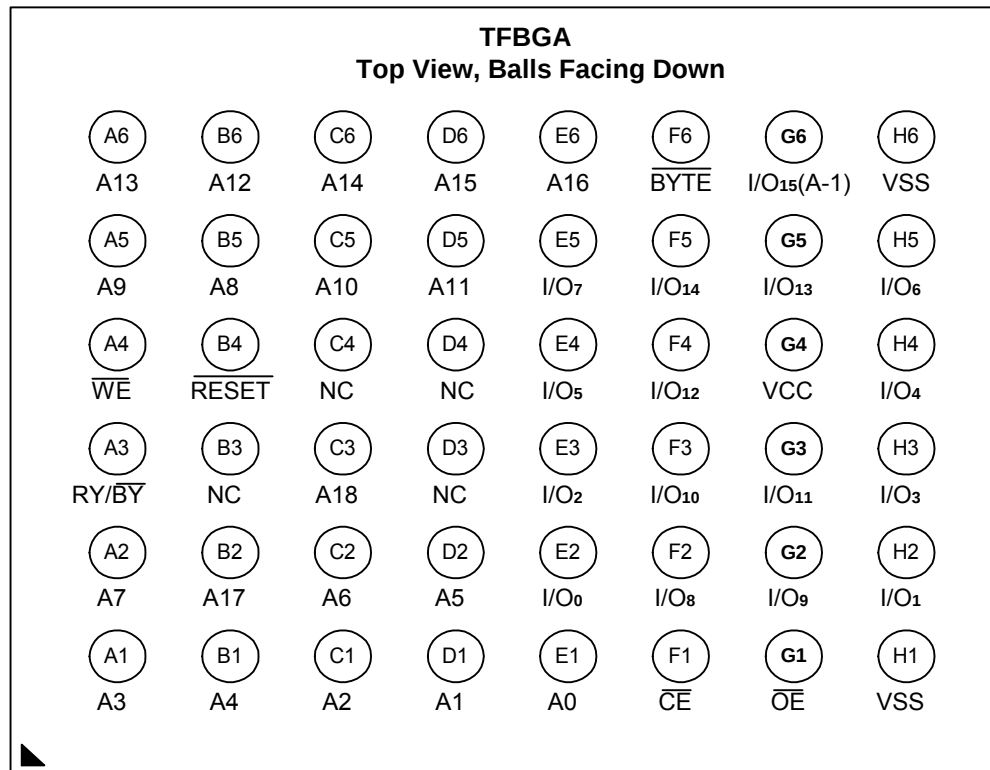
■ SOP



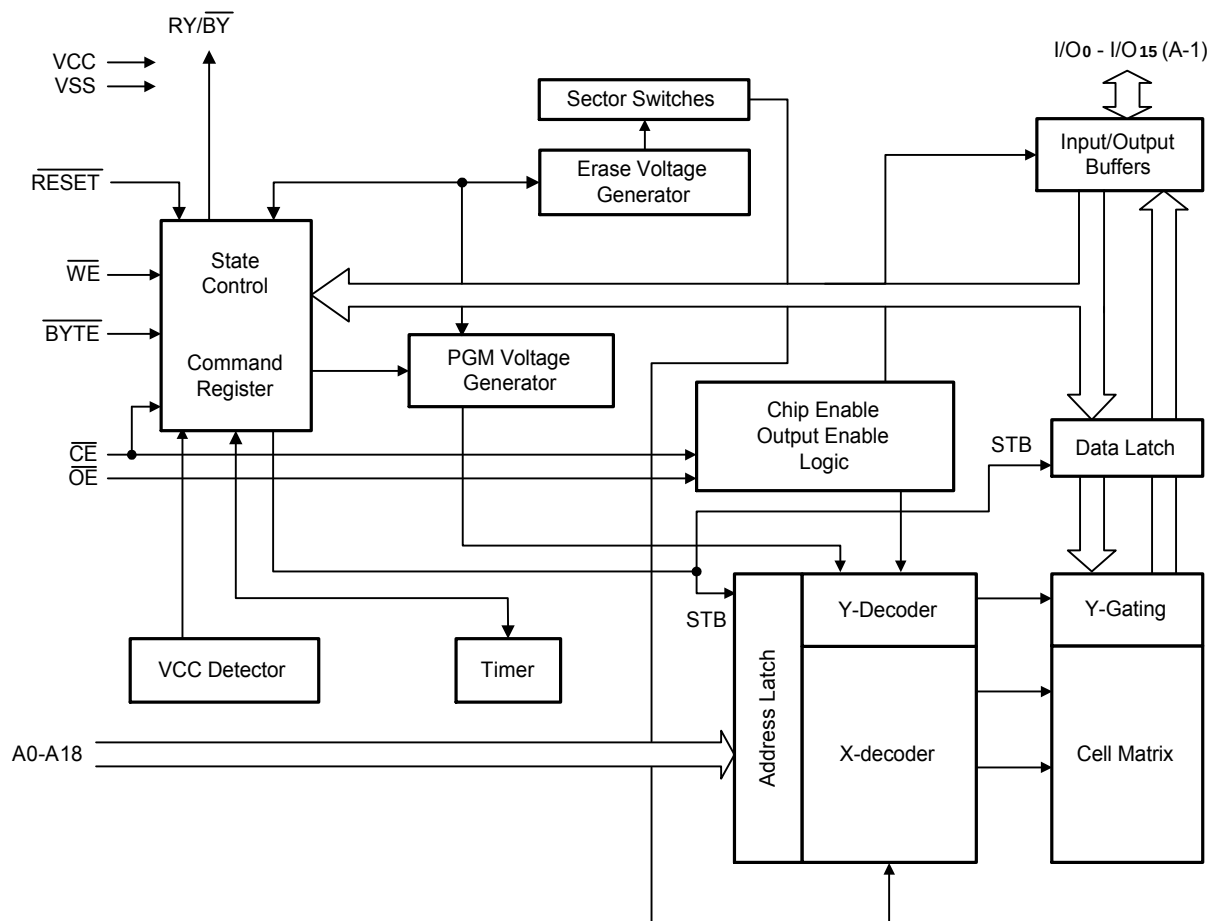
■ TSOP (I)



■ TFBGA



Block Diagram



Pin Descriptions

Pin No.		Description
A0 - A18		Address Inputs
I/O ₀ - I/O ₁₄		Data Inputs/Outputs
I/O ₁₅ (A-1)	I/O ₁₅	Data Input/Output, Word Mode
	A-1	LSB Address Input, Byte Mode
CE		Chip Enable
WE		Write Enable
OE		Output Enable
RESET		Hardware Reset
BYTE		Selects Byte Mode or Word Mode
RY/BY		Ready/BUSY - Output
VSS		Ground
VCC		Power Supply
NC		Pin not connected internally

2-1-5 2 Banks x 512K x 16 Bit Synchronous DRAM HY57V161610E

DESCRIPTION

THE Hynix HY57V161610E is a 16,777,216-bits CMOS Synchronous DRAM, ideally suited for the main memory and graphic applications which require large memory density and high bandwidth. HY57V161610E is organized as 2banks of 524,288x16.

HY57V161610E is offering fully synchronous operation referenced to a positive edge clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 1,2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipeline design is not restricted by a '2N' rule.)

FEATURES

- Single 3.0V to 3.6V power supply
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 50pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM/LDQM
- Internal two banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4, 8 and Full Page for Sequence Burst
 - 1, 2, 4 and 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 1, 2, 3 Clocks

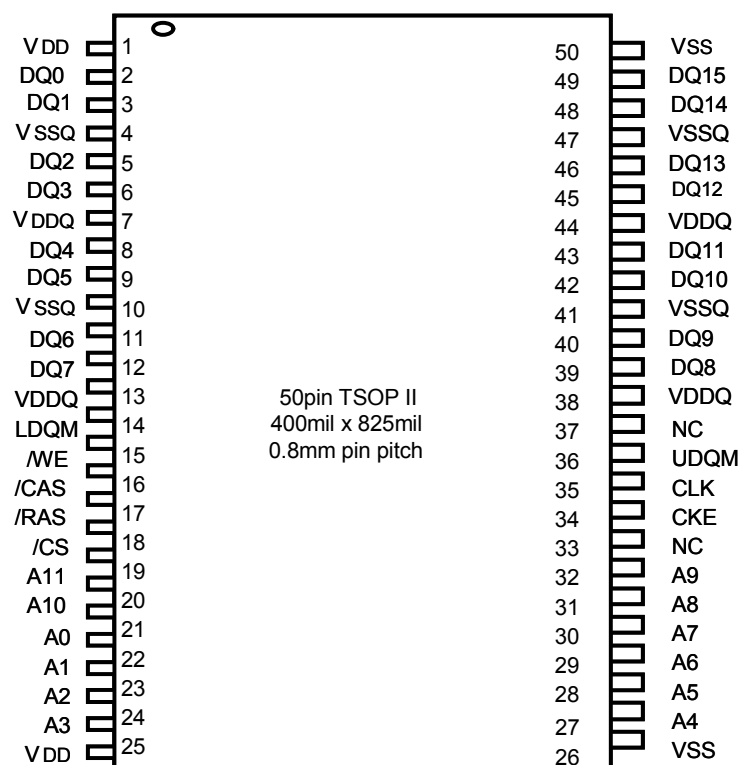
ORDERING INFORMATION

Part No.	Clock Frequency	Organization	Interface	Package
HY57V161610ET-5	200MHz	2Banks x 512Kbits x 16	LVTTL	400mil 50pin TSOP II
HY57V161610ET-55	183MHz			
HY57V161610ET-6	166MHz			
HY57V161610ET-7	143MHz			
HY57V161610ET-8	125MHz			
HY57V161610ET-10	100MHz			
HY57V161610ET-15	66MHz			

Note :

1. VDD(min) of HY57V161610ET-5/55 is 3.15V

PIN CONFIGURATION

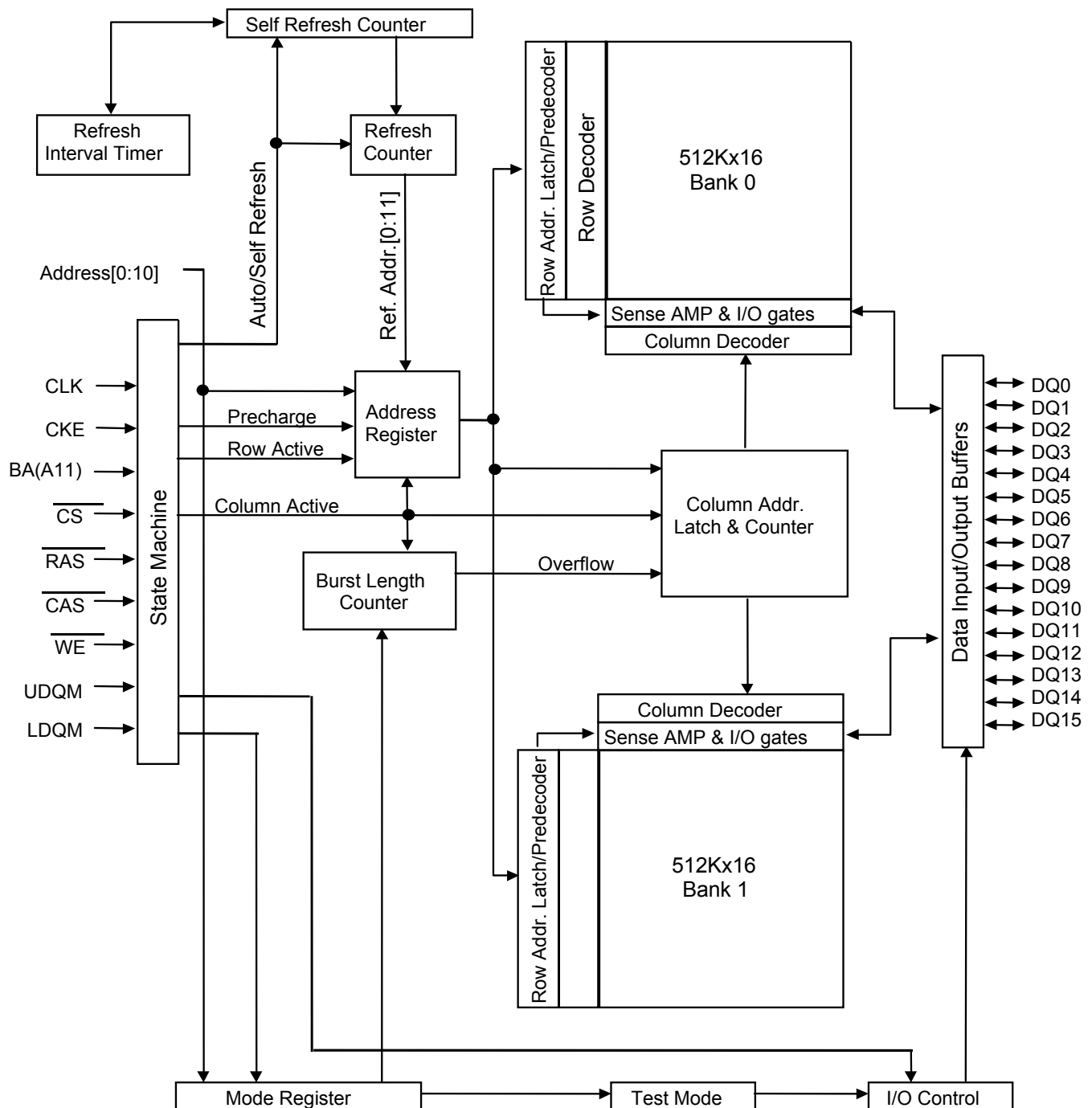


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
$\overline{\text{CS}}$	Chip Select	Command input enable or mask except CLK, CKE and DQM
BA	Bank Address	Select either one of banks during both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ activity.
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation. Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuit and input buffer
VDDQ/VSSQ	Data Output Power/Ground	Power supply for DQ
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mx16 Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature-Time	TSOLDER	260-10	°C ·Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0°C to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1, 2, 3
Input high voltage	VIH	2.0	3.0	VDD + 0.3	V	1, 4
Input low voltage	VIL	-0.3	0	0.8	V	1, 5

Note :

1. All voltages are referenced to VSS = 0V.
2. VDD(min) is 3.15V when HY57V161610ET-7 operates at $\overline{\text{CAS}}$ latency=2
3. VDD(min) of HY57V161610ET-5/55 is 3.15V
4. VIH(Max) : 4.6V AC pulse width with < 3ns of duration.
5. VIL(min) : -1.5V AC pulse width with < 3ns of duration.

AC OPERATING CONDITION (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	VIH / VIL	2.4/0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	tR / tF	1	ns	
Output timing measurement reference level	Voutref	1.4	V	
Output load capacitance for access time measurement	CL	30	pF	1

Note :

1. Output load to measure access times is equivalent to two TTL gates and one capacitance(30pF).
For details, refer to AC/DC output load circuit.
2. VDD(min) is 3.15V when HY57V161610ET-7 operates at $\overline{\text{CAS}}$ latency=2 and tCK2=8.9ns
3. VDD(min) of HY57V161610ET-5/55 is 3.15V'

Troubleshooting

Before resorting to maintenance service, please kindly check by yourself with the following chart.

Symptom	Cause(s)	Remedy
No Power	● The AC power cord is not connected to the power supply or is not connected to a power supply securely.	● Please check that the AC power cord is connected securely.
Picture There is no picture or the picture is distorted.	● The video cable isn't connected securely. ● Video output mode of the unit isn't correctly set. ● Video input mode of the connected TV isn't correctly set.	● Connect the video cable securely. ● Press [V-MODE] repeatedly until the picture becomes normal again. ● Set an appropriate video input mode.
Sound There is no sound or the sound is distorted.	● The audio cables aren't connected securely. ● The volume is set to the minimum level. ● The sound is switched off. ● The disc is in fast forward/reverse playback.	● Connect the audio cables securely. ● Turn up the volume. ● Press [MUTE] on the remote control to switch on the sound. ● Press [PLAY/PAUSE].
Unable to play a disc	● This disc is placed in the disc tray in a wrong way. ● The rating of the disc is higher than the rate set in the parental control item. ● The unit isn't compatible with the disc. ● The disc is dirty.	● Check that the disc is placed in the disc tray with its label side upwards. ● Reset the settings in the parental control item. ● / ● Clean the disc.
The player breaks down when a USB drive is inserted into the player.	● The connected USB drive is probably not a certified one.	● The player cannot play any uncertified USB drive. In case the player breaks down, turn it off, disconnect the power cord from the AC outlet and unplug the USB drive from the player. Then, power on the player again. The player will resume the normal status.
The buttons on the unit doesn't work.	● The unit is being interfered with static electricity etc.	● Switch off and unplug the unit. Then connect the plug to the power supply and switch it on again.
The remote control does not function.	● There is no battery in the remote control. ● The batteries are out of charge. ● The remote control isn't pointed to the remote sensor. ● The remote control is out of its operating area. ● The unit is shut down.	● Install two AAA/1.5V batteries in it. ● Replace the batteries with new ones. ● Make sure that the remote control is pointed to the remote control sensor. ● Make sure the remote control is within the operating area. ● Switch off the unit and disconnect it from the AC outlet. Then power on the unit again.

Specifications

Power supply		AC 100-240V 50/60Hz
Power consumption		25W
Working environment	Temperature	-10~+40℃
	Relative humidity	5%~90%
Disc output	TV System	PAL/NTSC
	Frequency Response	20Hz~20KHz
	S/N(A weight)	>80dB(1KHz)
	Frequency Range	≥70dB(1KHz)
	THD+NOISE	≤ -60dB(1KHz)
	WOW FLUTTER	Below the limit of apparatus measure
Tuner	FM band Range	64MHz-108MHz
Power output (Max)		25WX2
Frequency response		± 1.5dB(20Hz~20KHz)

4. Upgrading System and Changing the Region Code

MTK upgrade:

1. Name upgrade file as "MTK.BIN"(must be in big caps)
2. Record it in a CD-R/W (It can be enclosed a sub-directory which size is about 30M, and the file content can be letter or non used file.)
disc Format: (advise to use the tool NERO burning ROM)
Disc volume: MEDiatek, ISO9660 LEVEL1, MODE1, not JOILET.
3. Put the recorded disc into the DVD player, on the TV will show "upgrade?" after loading. Press PLAY button, the player will automatically upgrade.
4. Do not shut down the player during upgrade, it will restart automatically after upgrade.
5. Upgrade finish!

How to change the region code:

1. Power on the machine, and press OPEN button to push the tray out.
2. Press "1.3.6.9" buttons, the screen display "XXXX", you can change the region code to 0-6 with 0-6 button, the number 0 means REGION FREE.

5. Operating Instruction

Please refer to the User's Manual for the operating instruction of the system.

Maintenance & Troubleshooting

How to handle discs

To handle, clean and protect discs

- Do not touch the playing side of a disc



- Do not stick any paper or glue strip on a disc.



How to clean discs

- Finger prints and dust on surface can affect the sound and picture quality. Clean discs regularly with a soft cotton cloth from disc center to outside.



- For sticky dust, wipe it with wet cloth and with dry cloth, Any kind of solvent, such as diluting agent, gasoline, liquid detergent, gasoline liquid detergent anti-static aerosol used for vinylon LP, may cause disc damage.

How to protect discs

- Keep away from the direct sunshine or any heat source.
- Do not put discs in damp or dirty places, such as bathroom or near humidifiers. Store discs vertically in disc box and store in a dry place. Piling discs on to top of each other or excess weight load on disc box may cause the disc to warp.

Disc Compatibility

- Some DVD discs may have special requirements for playing, with which this player may not be compatible. Please refer to specifications on individual disc.

DISC TYPE	Content	Size	Total Play time
DVD	AUDIO/VIDEO	12CM	About 2hrs. (Single side & single layer)
			About 4hrs. (Single side & double layer)
			About 4hrs. (Double side & Single layer)
			About 8hrs. (Double side & double layer)
CD-DA	AUDIO	12CM	About 74 minutes
MP3	AUDIO	12CM	About 300 minutes

Discs types

This DVD player can play the following types of discs: Discs other than listed above cannot be played by this player.

This player uses NTSC/PAL color system. It cannot play discs recorded with other systems, such as SECAM.

Region code

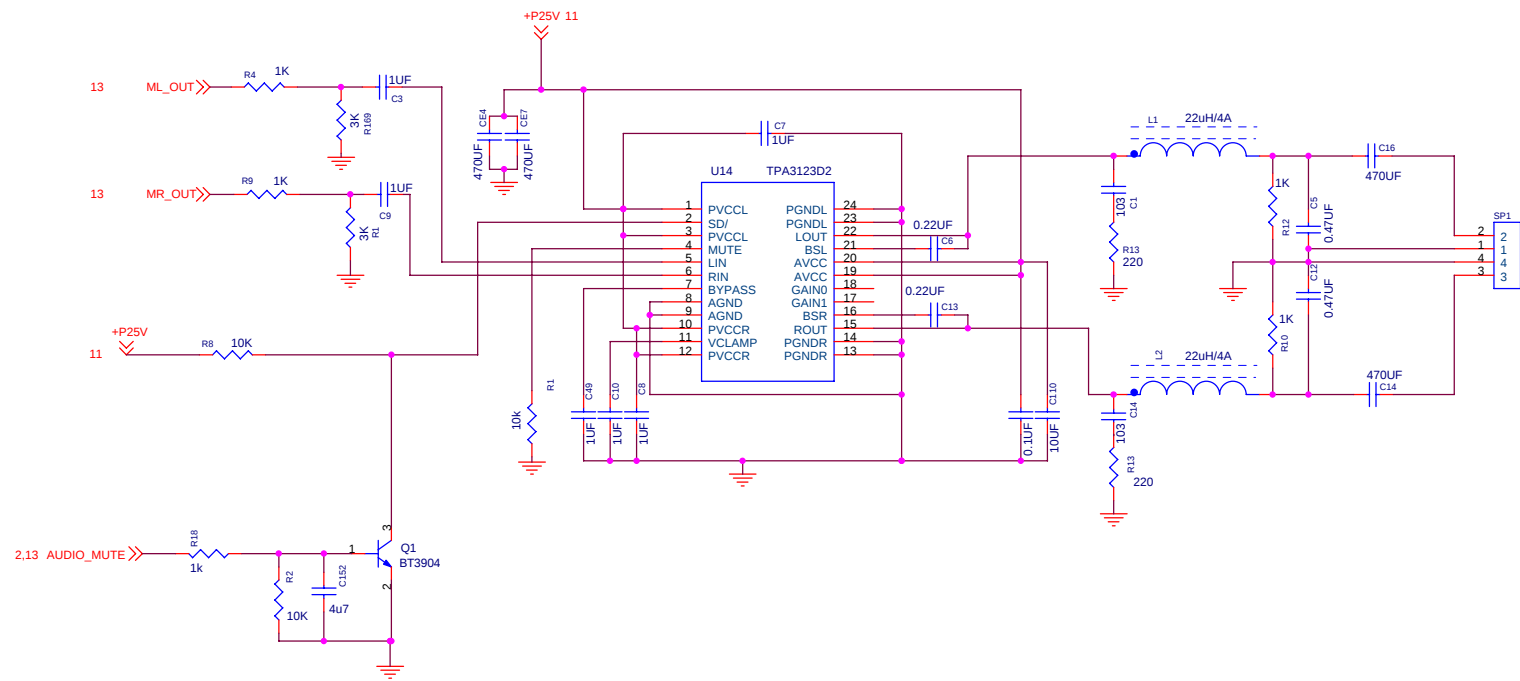
When play the region disc with player unconf-ormity, the screen display "WRONG REGION", you can change the region code, please refer-ence the "How to change the region code".

Copyright

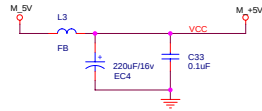
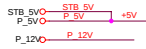
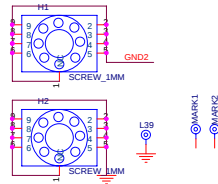
According to the related law, DVD discs without proper authorization are not allowed to be copied broadcast cable broadcast, played publicly or rented. As DVD discs are anti-piracy the copied content is distorted.

TV system

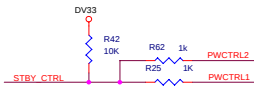
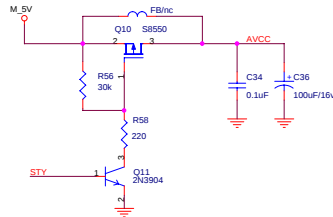
Connect this player to a PAL/NTSC compatible TV.



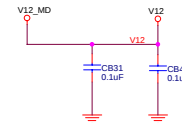
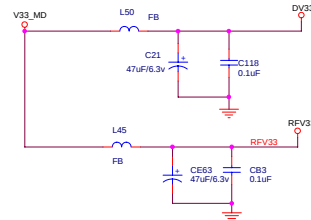
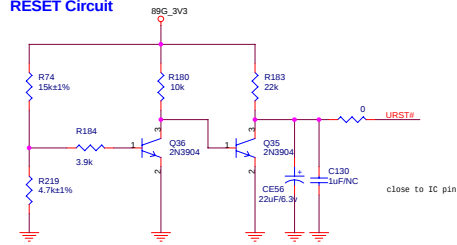
- 1 INDEX & POWER / RESET
- 2 MT1389G LQFP128
- 3 SDRAM & FLASH & MOTOR
- 4 AUDIO & MIC I/F
- 5 VIDEO I/F
- 6 MCR & USB I/F



Standby Power Control



RESET Circuit

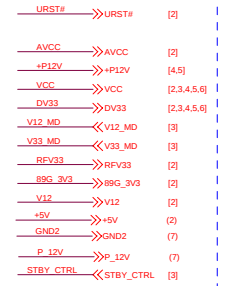


Rev	History	P#	Date
V1	Original release.Base on COMMON1389G_HD65_AT5669_V1.2		2009.09.28

MT1389G 128 PIN GPIO LIST

NAME	PIN	FEATURES
TRAY_OPEN	14	FM/AM SDIO [STBY]
TRAY_CLOSE	15	SWITCH [TROPEN; IOA]
FG / GPIO2	18	TRIN
UPI_6	28	HDMI_SCL
UPI_7	29	HDMI_SDA
GPIO3	34	CEC
GPIO4	35	VSCK [6xyz_LOAD]
GP05	7	TRCLOSE
GPIO6	31	VSDA TxD [6xyz_CLK]
GPIO7	39	SD_CLK MS_CLK
GPIO8	38	SD_CMD MS_BS
GPIO9	37	SD_DATA MS_DATA
GPIO10	81	HPLG
GPIO11	30	SCART1 HSYNC# RxD
GPIO12	80	ASPDIF
GPIO13	36	VSTB
GP014	96	A_MUTE
GPIO19	103	SCART2 VSYNC#
GPIO20	104	STBY_CTRL
GPIO21	105	AKIN1_MIC
ARF	109	PT2313_IS CLK
ARS	110	FM/AM RST
ALS	114	FM/AM SCK
ALF	115	PT2313_IS DATA
GPIO34	107	TROPEN IOA [6xyz_D1#]
GPIO35	108	STBY [6xyz_D2#]
RFIN / OP0UT	120	LIMIT TROUT

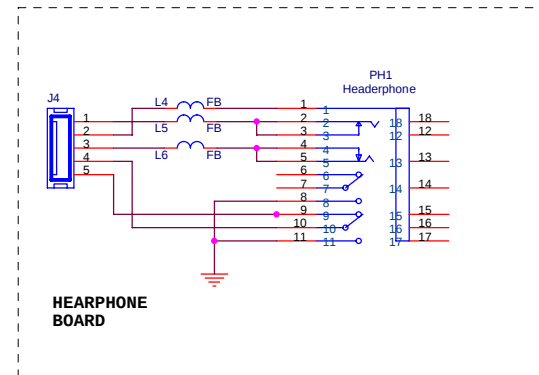
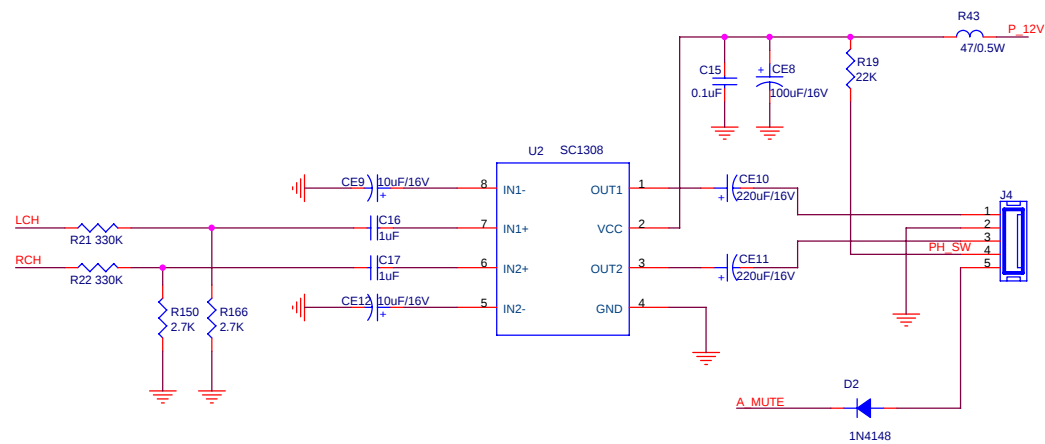
OFF-PAGE CONNECTION

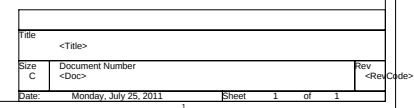


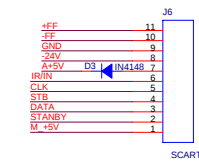
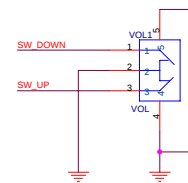
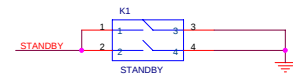
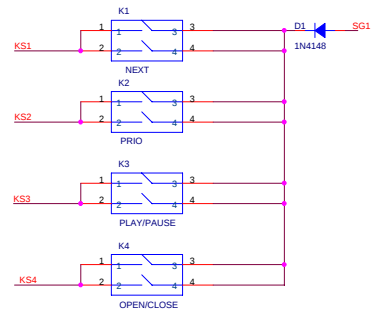
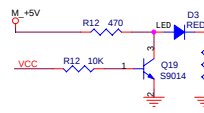
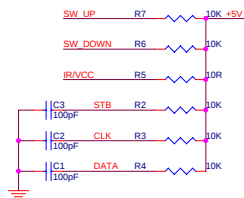
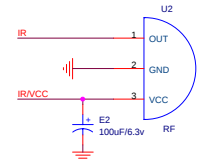
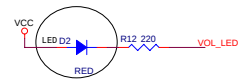
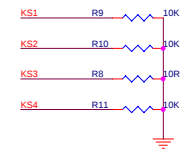
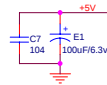
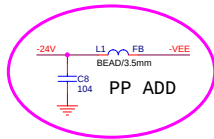
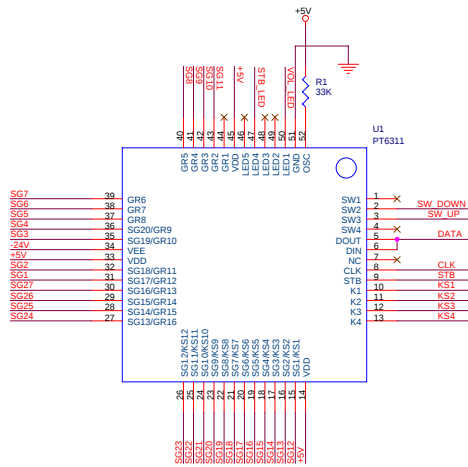
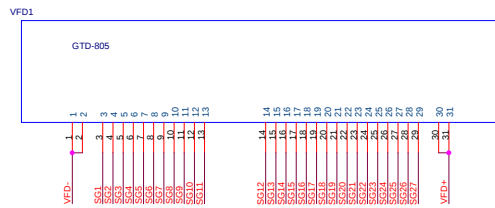
Power

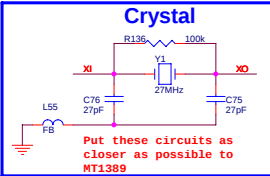
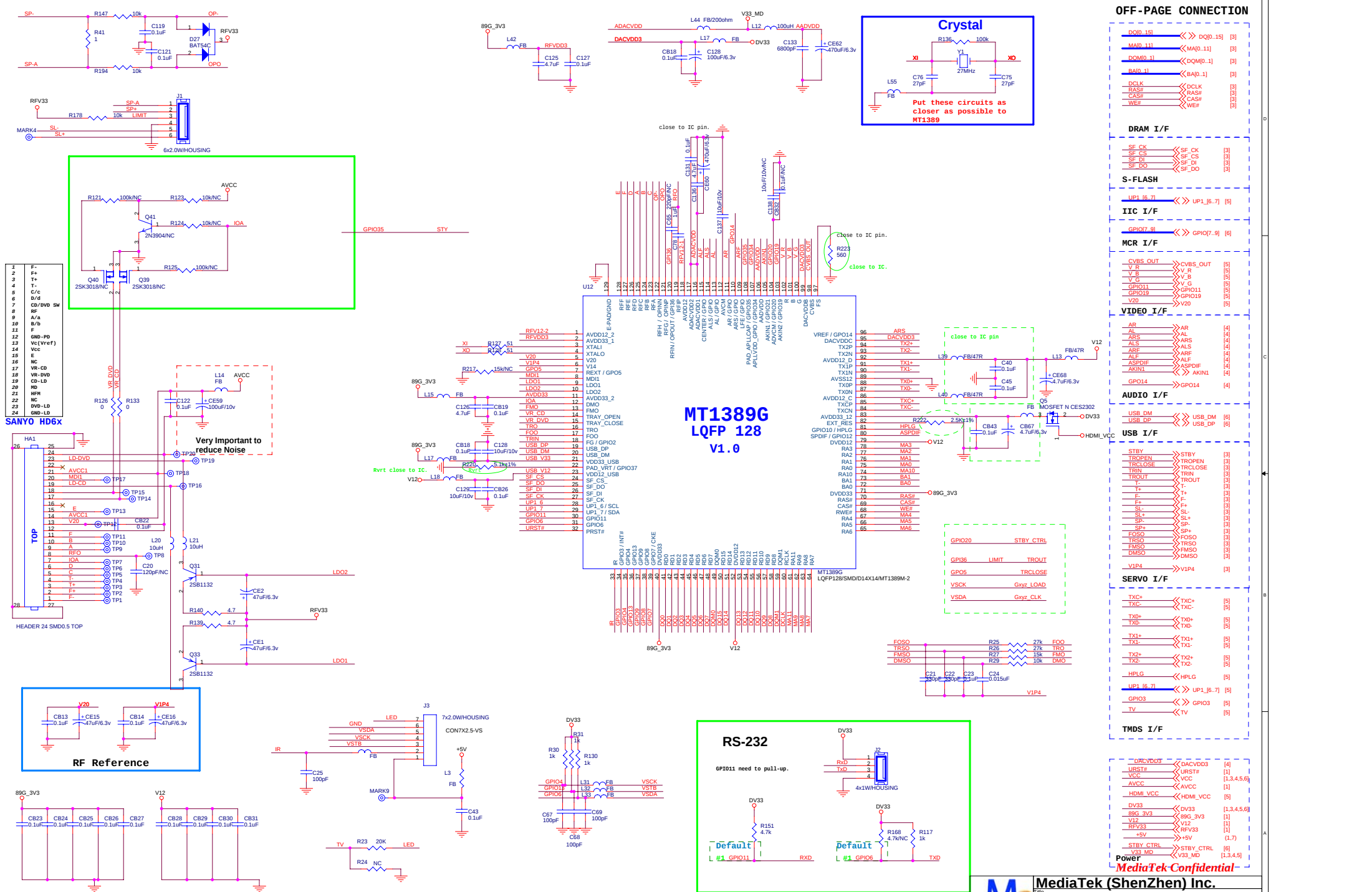
DM808H CIRCUIT 110308 MediaTek Confidential

MediaTek (ShenZhen) Inc.			
COMMON1389G_HD850_AT5669_STBY			
Size	Document Number	Drawn	gubing.tao
Customer	INDEX / POWER / RESET	Checked	Zhenhua.zhang
Date	Monday, July 25, 2011	Sheet	1 of 7









OFF-PAGE CONNECTION

DQ0.15	<<>>	DQ0.15	[3]
MA0.11	<<>>	MA0.11	[3]
DQM0.11	<<>>	DQM0.11	[3]
BA0.11	<<>>	BA0.11	[3]
DCLK	<<>>	DCLK	[3]
RAS#	<<>>	RAS#	[3]
CAS#	<<>>	CAS#	[3]
WE#	<<>>	WE#	[3]

DRAM I/F

SF CK	<<>>	SF CK	[3]
SF CS	<<>>	SF CS	[3]
SF DI	<<>>	SF DI	[3]
SF DO	<<>>	SF DO	[3]

S-FLASH

UP1 [6..7]	<<>>	UP1 [6..7]	[5]
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IIC I/F

GPIO7.9	<<>>	GPIO7.9	[6]
---------	------	---------	-----

MCR I/F

CVBS_OUT	<<>>	CVBS_OUT	[5]
V_R	<<>>	V_R	[5]
V_B	<<>>	V_B	[5]
V_G	<<>>	V_G	[5]
GPIO11	<<>>	GPIO11	[5]
GPIO19	<<>>	GPIO19	[5]
V20	<<>>	V20	[5]

VIDEO I/F

AR	<<>>	AR	[4]
ALS	<<>>	ALS	[4]
ARF	<<>>	ARF	[4]
ALF	<<>>	ALF	[4]
ASPDIF	<<>>	ASPDIF	[4]
AKIN1	<<>>	AKIN1	[4]
GPIO14	<<>>	GPIO14	[4]

AUDIO I/F

USB_DM	<<>>	USB_DM	[6]
USB_DP	<<>>	USB_DP	[6]

USB I/F

STBY	<<>>	STBY	[3]
TROPEN	<<>>	TROPEN	[3]
TRCLOSE	<<>>	TRCLOSE	[3]
TRIN	<<>>	TRIN	[3]
TROUT	<<>>	TROUT	[3]
F+	<<>>	F+	[3]
F-	<<>>	F-	[3]
SL+	<<>>	SL+	[3]
SL-	<<>>	SL-	[3]
SP+	<<>>	SP+	[3]
SP-	<<>>	SP-	[3]
FMSO	<<>>	FMSO	[3]
TRSO	<<>>	TRSO	[3]
FMSO	<<>>	FMSO	[3]
DMISO	<<>>	DMISO	[3]
V1P4	<<>>	V1P4	[3]

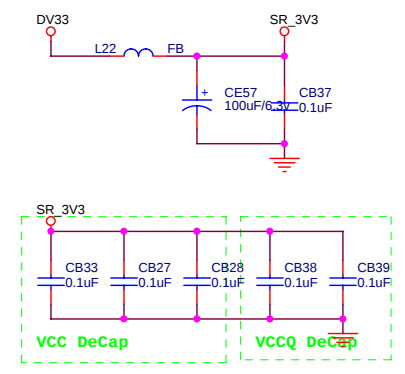
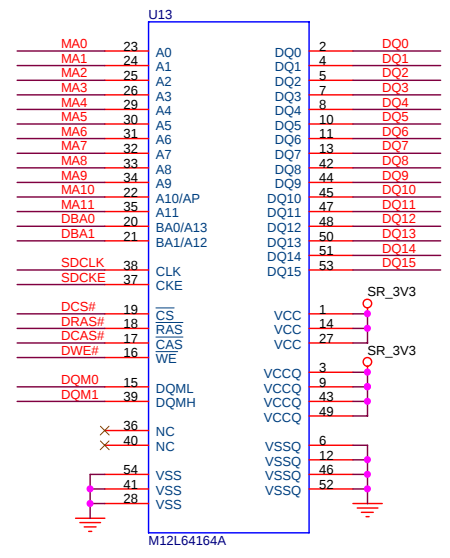
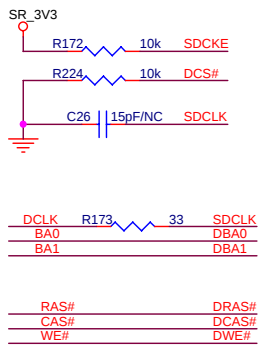
SERVO I/F

TXC+	<<>>	TXC+	[5]
TXC-	<<>>	TXC-	[5]
TXD+	<<>>	TXD+	[5]
TXD-	<<>>	TXD-	[5]
TX1+	<<>>	TX1+	[5]
TX1-	<<>>	TX1-	[5]
TX2+	<<>>	TX2+	[5]
TX2-	<<>>	TX2-	[5]
HPLG	<<>>	HPLG	[5]
UP1 [6..7]	<<>>	UP1 [6..7]	[5]
GPIO3	<<>>	GPIO3	[5]
TV	<<>>	TV	[5]

TMDS I/F

DACVD03	<<>>	DACVD03	[4]
URST#	<<>>	URST#	[1]
VCC	<<>>	VCC	[1,3,4,5,6]
AVCC	<<>>	AVCC	[1]
HDMI_VCC	<<>>	HDMI_VCC	[5]
DV33	<<>>	DV33	[1,3,4,5,6]
89G_3V3	<<>>	89G_3V3	[1]
RFV33	<<>>	RFV33	[1]
+SV	<<>>	+SV	[1,7]
STBY_CTRL	<<>>	STBY_CTRL	[6]
V33_MD	<<>>	V33_MD	[1,3,4,5]

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SDR_DRAM (Dual Layout)

OFF-PAGE CONNECTION

DQ[0..15]	↔	DQ[0..15]	[2]
MA[0..11]	↔	MA[0..11]	[2]
DOM[0..1]	↔	DQM[0..1]	[2]
BA[0..1]	↔	BA[0..1]	[2]
DCLK	↔	DCLK	[2]
RAS#	↔	RAS#	[2]
CAS#	↔	CAS#	[2]
WE#	↔	WE#	[2]

DRAM I/F

SF CK	↔	SF CK	[2]
SF CS	↔	SF CS	[2]
SF DI	↔	SF DI	[2]
SF DO	↔	SF DO	[2]

S-FLASH

STBY	↔	STBY	[2]
TROPEN	↔	TROPEN	[2]
TRCLOSE	↔	TRCLOSE	[2]
TRIN	↔	TRIN	[2]
TROUT	↔	TROUT	[2]
T-	↔	T-	[2]
T+	↔	T+	[2]
F-	↔	F-	[2]
F+	↔	F+	[2]
SL-	↔	SL-	[2]
SL+	↔	SL+	[2]
SP-	↔	SP-	[2]
SP+	↔	SP+	[2]
FOSO	↔	FOSO	[2]
TRSO	↔	TRSO	[2]
FMSO	↔	FMSO	[2]
DMSO	↔	DMSO	[2]
V1P4	↔	V1P4	[2]

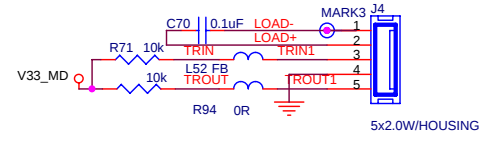
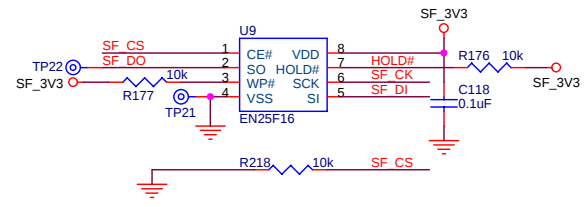
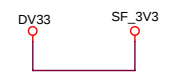
SERVO I/F

DV33	↔	DV33	[1,2,4,5,6]
VCC	↔	VCC	[1,2,4,5,6]
V12_MD	↔	V12_MD	[1]
V33_MD	↔	V33_MD	[1,2,4,5]

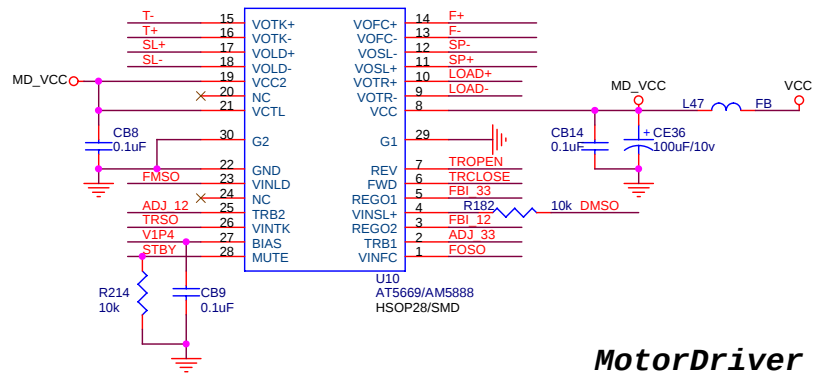
Power

URST#	↔	URST#	[1,2]
-------	---	-------	-------

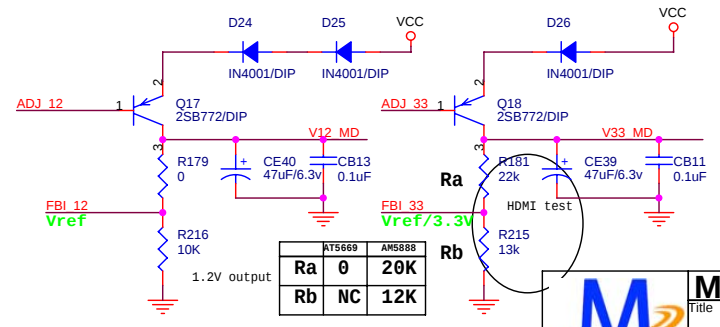
Misc



SerialFlash



MotorDriver



Ra	0	20K
Rb	NC	12K



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MediaTek (ShenZhen) Inc.

Title: **COMMON1389G_HD850_AT5669_STBY**

Size B: **SDRAM / FLASH / MOTOR**

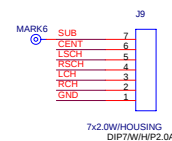
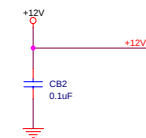
Date: Monday, July 25, 2011

Drawn: **guibing.luo**

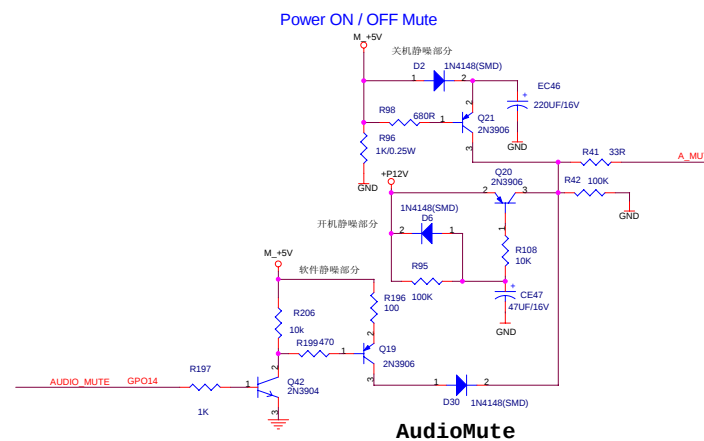
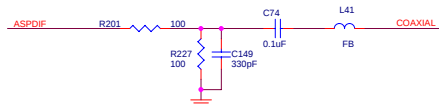
Checked: **Zhenhua.zhang**

Rev 1

Sheet 3 of 7

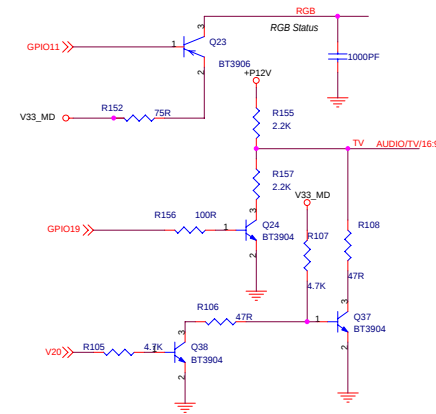
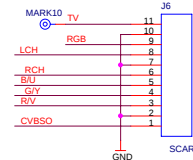
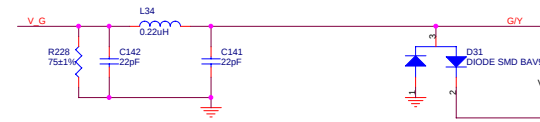
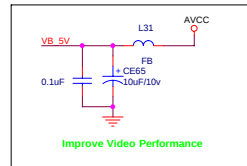
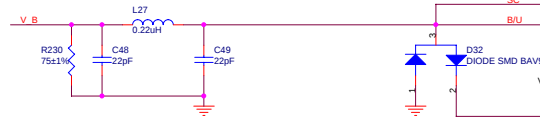
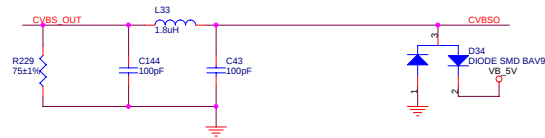
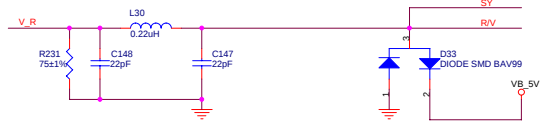


The diagram shows a multi-pin connector labeled P1. It has six signal lines on the left and right sides, each with a color and a number. The lines are: R/V (2), COAXIAL (3), B/U (5), RCH (6), G/Y (8), and LCH (9). The connector has two rows of pins. The top row has pins 1, 2, 3, and 4. The bottom row has pins 5, 6, 7, and 8. The connections are: R/V (2) to pin 2, COAXIAL (3) to pin 3, B/U (5) to pin 5, RCH (6) to pin 6, G/Y (8) to pin 8, and LCH (9) to pin 9. The RCA-3x2 label is at the bottom.



- Power

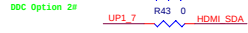
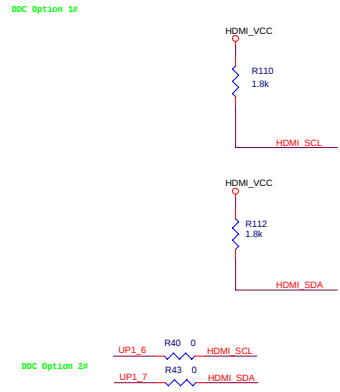
default: Low Impedance Mode



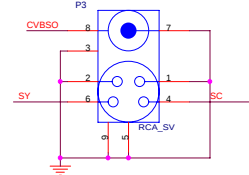
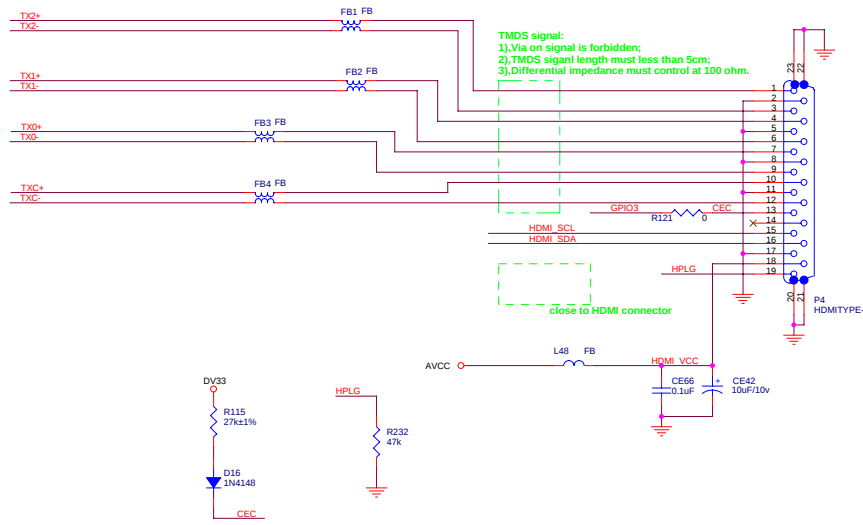
add SCART config circuit

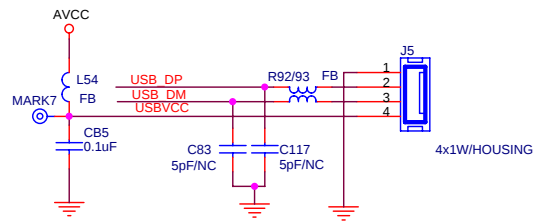
OFF-PAGE CONNECTION			
CVBS_OUT	CVBS_OUT	[2]	[2]
V_R	V_P	[2]	[2]
V_B	V_B	[2]	[2]
V_G	V_G	[2]	[2]
R/V	R/V	[4]	[4]
B/U	B/U	[4]	[4]
G/Y	G/Y	[4]	[4]
VIDEO I/F			
RCH	RCH	[4]	[4]
LCH	LCH	[4]	[4]
TV	TV	[2]	[2]
AUDIO I/F			
GPIO11	GPIO11	[2]	[2]
GPIO19	GPIO19	[2]	[2]
V20	V20	[2]	[2]
SCART/VGA I/F			
TXC+	TXC+	[2]	[2]
TXC-	TXC-	[2]	[2]
TX0+	TX0+	[2]	[2]
TX0-	TX0-	[2]	[2]
TX1+	TX1+	[2]	[2]
TX1-	TX1-	[2]	[2]
TX2+	TX2+	[2]	[2]
TX2-	TX2-	[2]	[2]
HPLG	HPLG	[2]	[2]
UP1_6..7	UP1_6..7	[2]	[2]
GPIO3	GPIO3	[2]	[2]
TMDS I/F			
HDMI_VCC	HDMI_VCC	[2]	[2]
AVCC	AVCC	[1,2,3,4,6]	[1,2,3,4,6]
DV33	DV33	[1,2,3,4,6]	[1,2,3,4,6]
+P12V	+P12V	[1,4]	[1,4]
V33_MD	V33_MD	[1,2,3,4]	[1,2,3,4]
POWER			

DDC

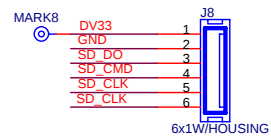
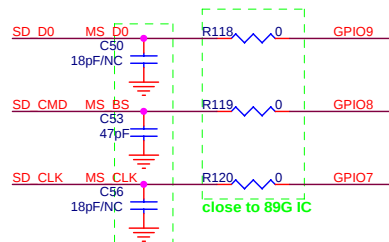


HDMI I/F





USB I/F



OFF-PAGE CONNECTION

GPIO[7..9] << GPIO[7..9] [2]

MCR I/F

USB_DM << USB_DM [2]

USB_DP << USB_DP [2]

USB I/F

DV33 << DV33 [1,2,3,4,5]

AVCC << AVCC [1,2,3,4,5]

+P12V << +P12V [1,4]

Power

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	COMMON1389G_HD850_AT5669_STBY		
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		Sheet 6	of 7



