

FIGARO - 2

DMN8602MK Main Codec Board (DDR SDRAM)

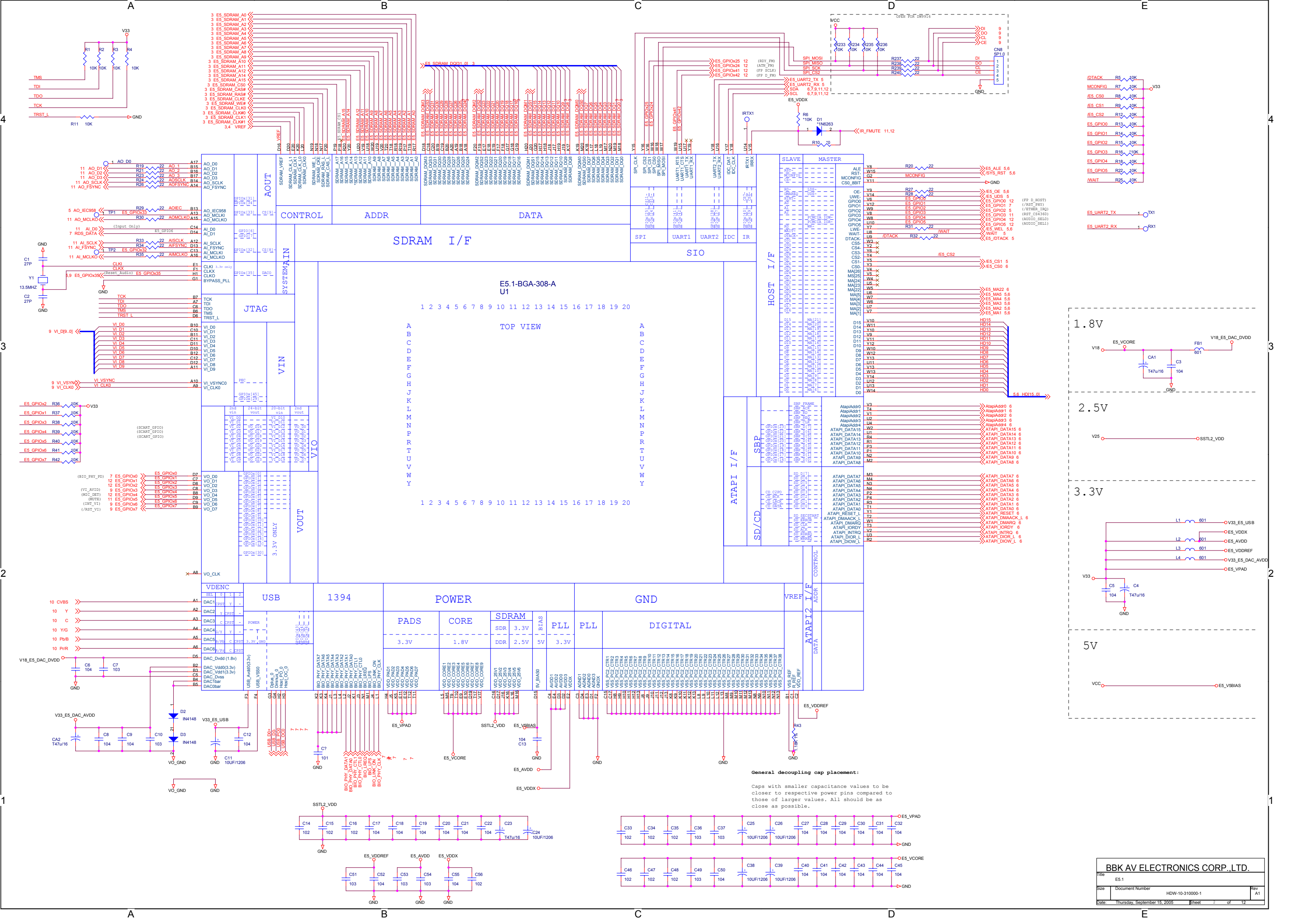
BBK AV ELECTRONICS CORP.,LTD.

REVISION HISTORY

VER	REV	DATE	DESCRIPTION
A	0	08/20/2003	Initial Draft
A	1	09/27/2003	1: Correct net name E5_SDRAM_DQ0 (U27_M18) and E5_SDRAM_DQ1 (U27_M19) . 2: Change net I2C_SCL to IDC_SCL.
A	1	10/26/2003	BBK MODIFY BY FENGHONGJUN

SCHEMATICS CONTENTS

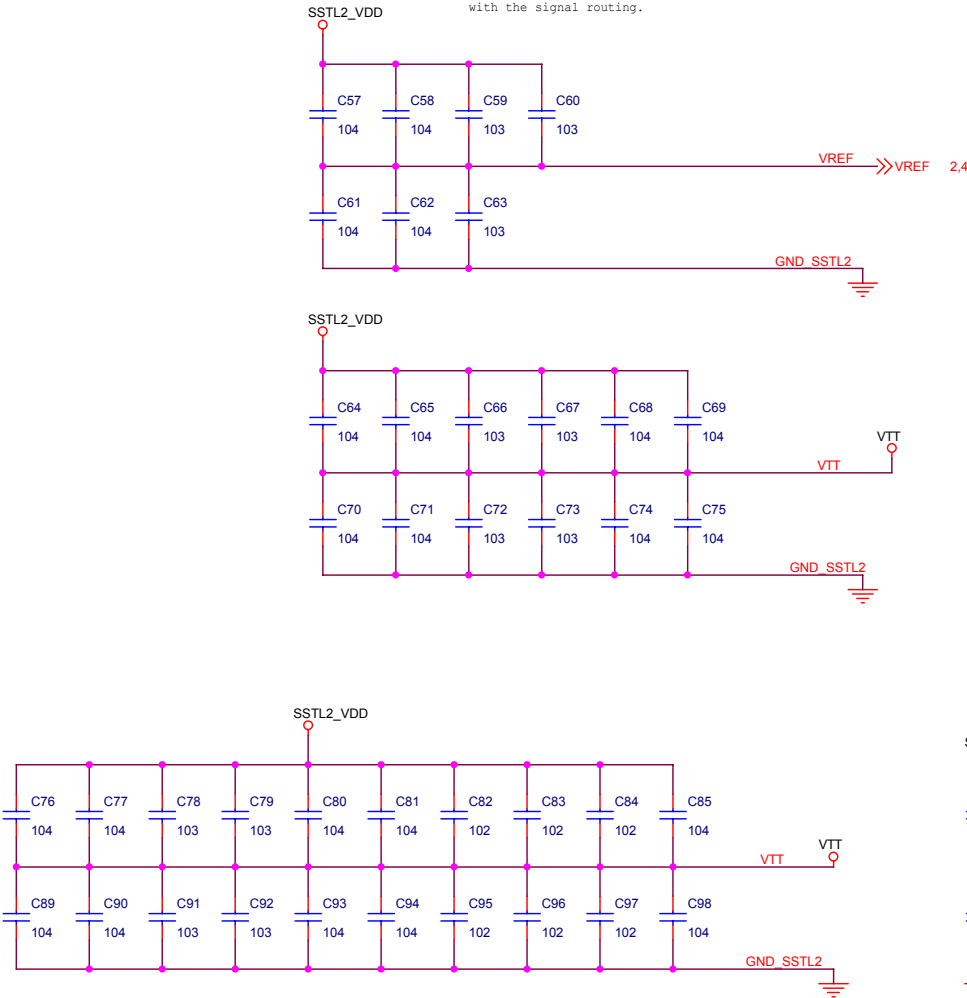
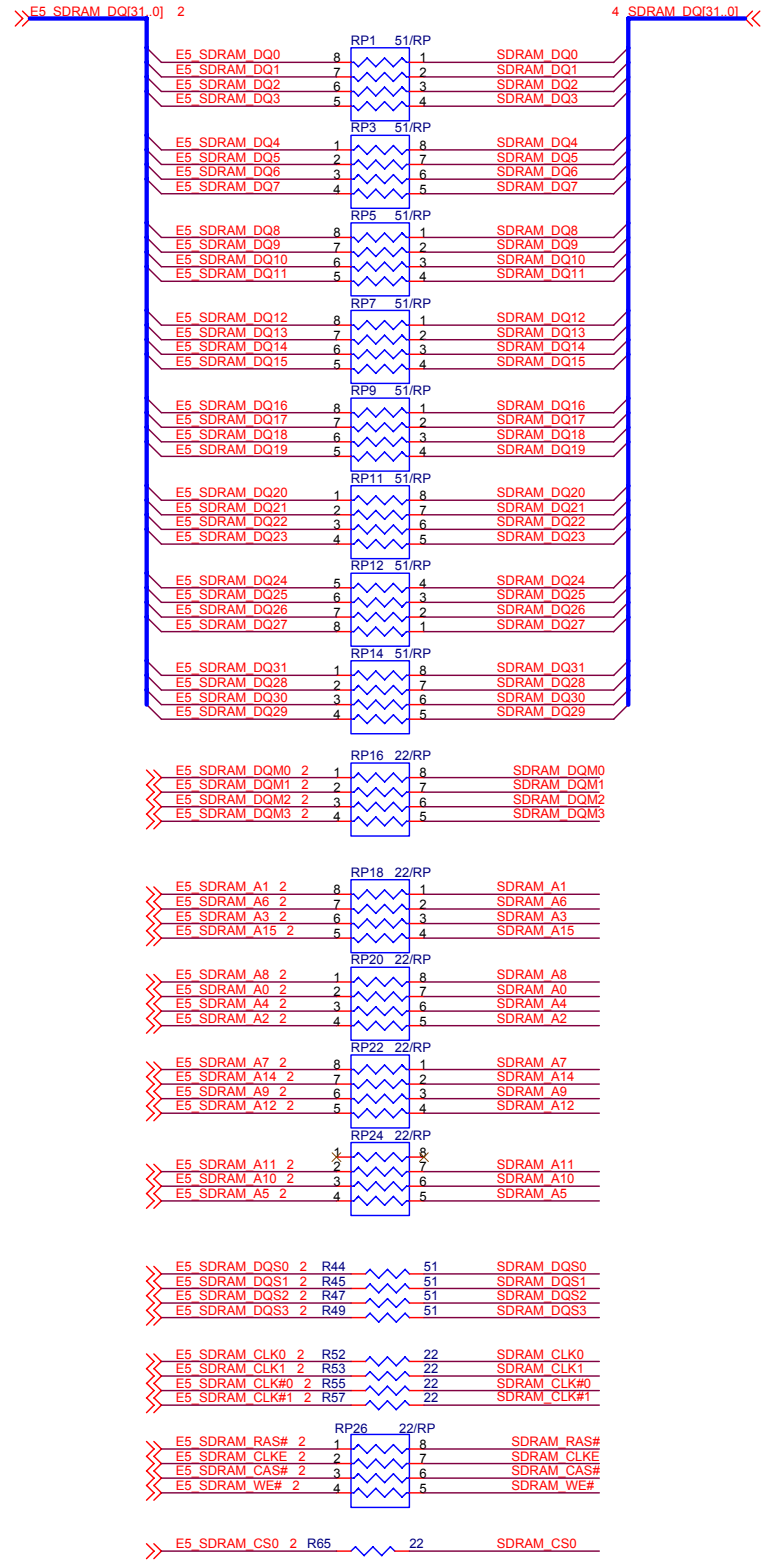
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TERMINATION
AT E5.1

TERMINATION
AT DDR

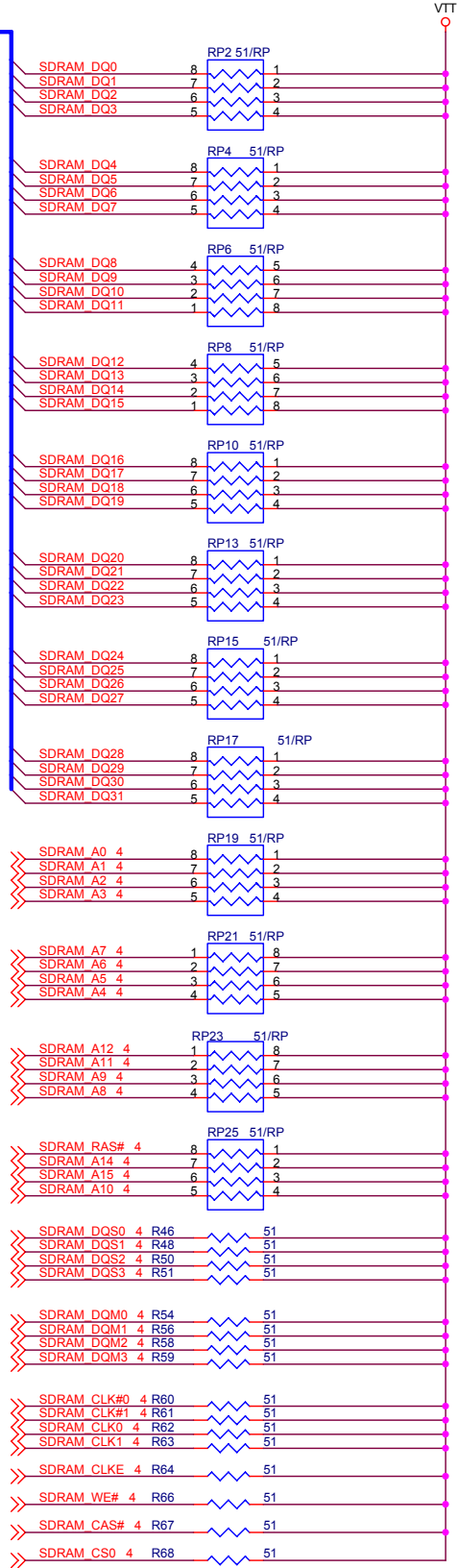
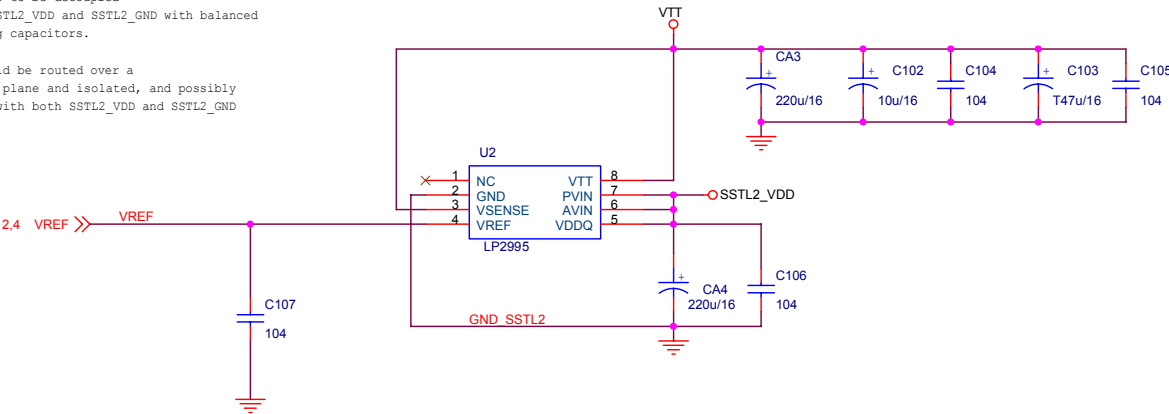
The VTT side of the terminaton resistors should be placed on a wide VTT island on the surface layer. The island is located at each end of the bus, so it does not interfere with the signal routing.

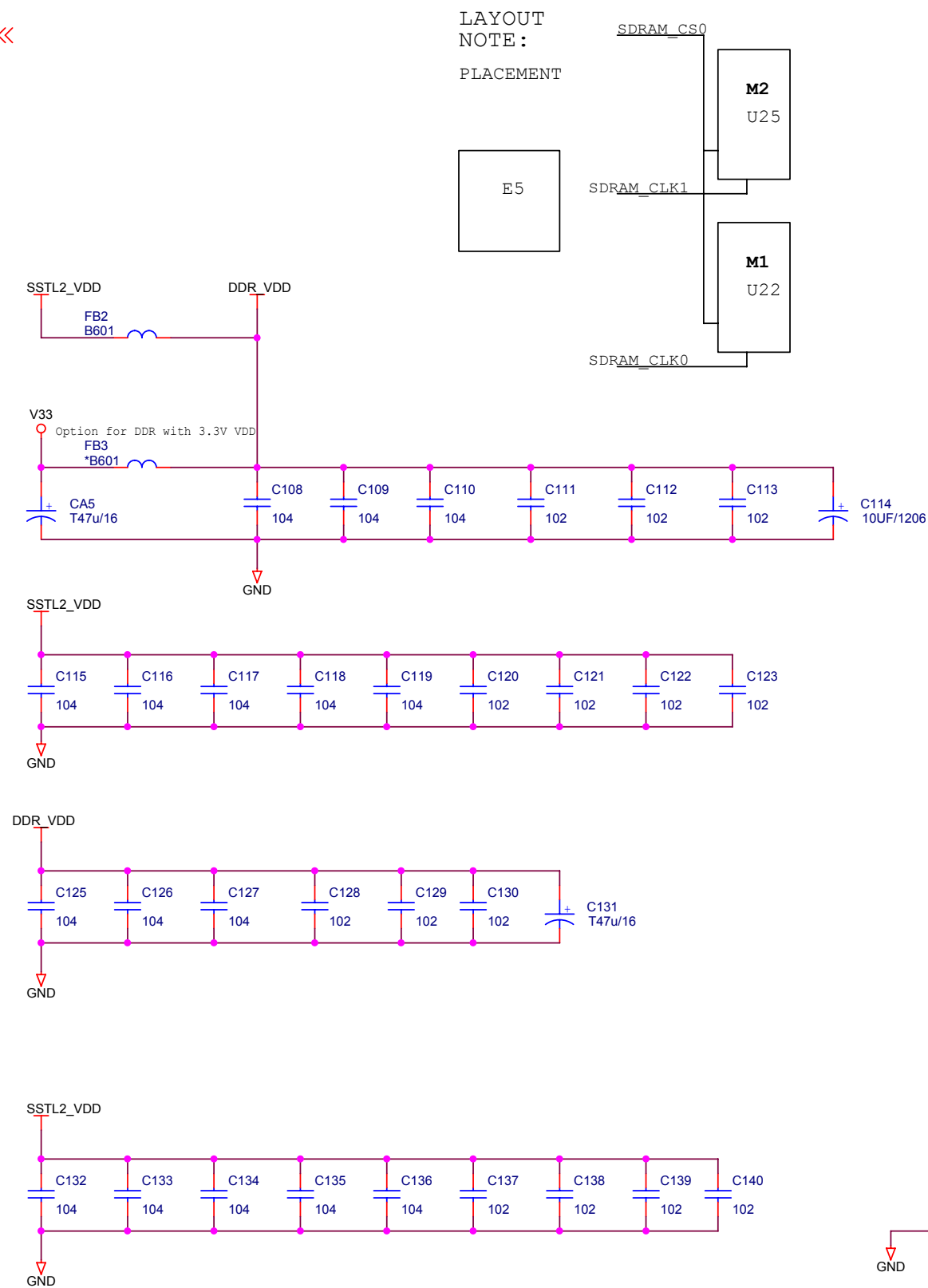
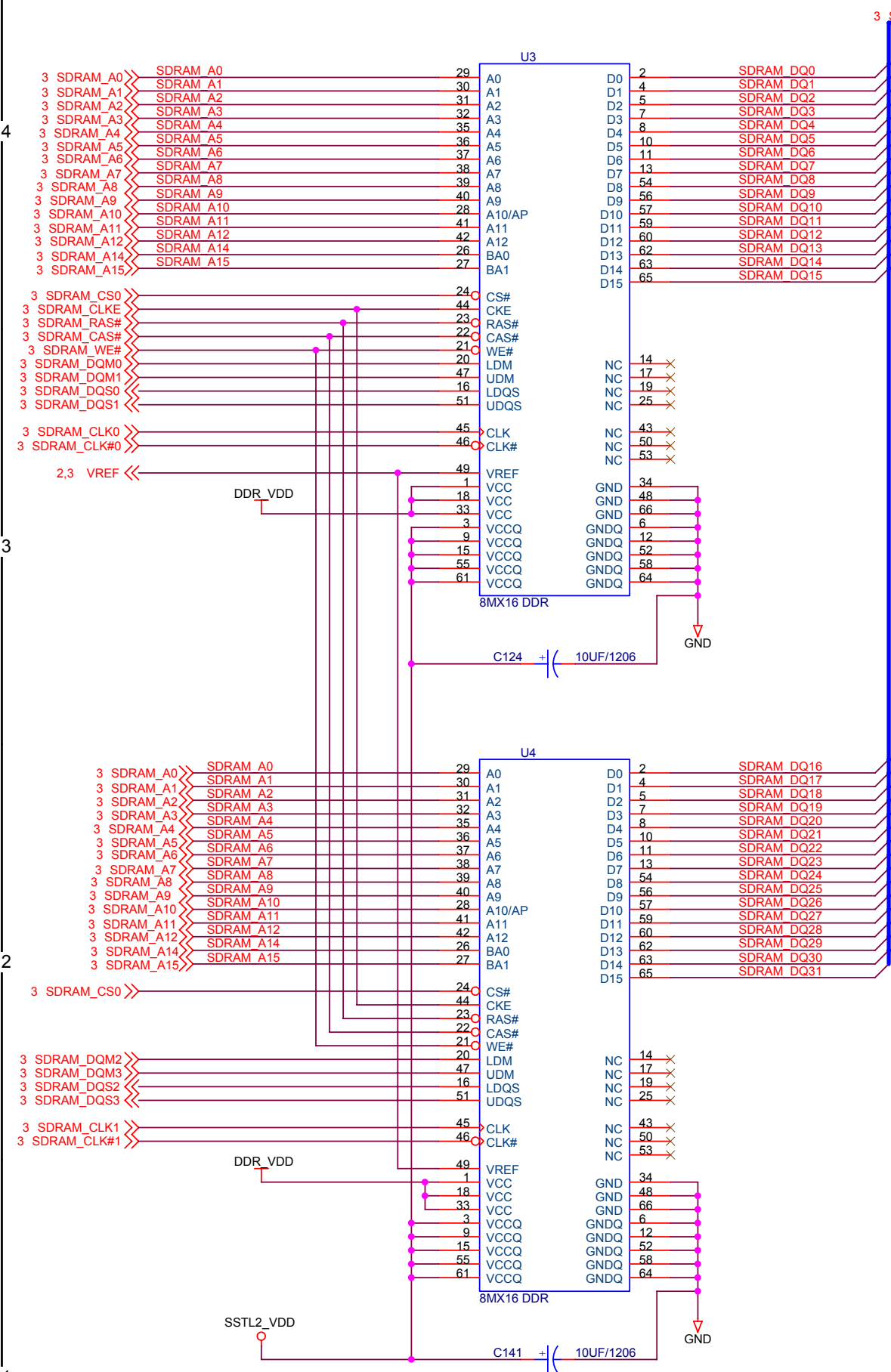


DDR TERMINATION VOLTAGE REGULATOR

VREF needs to be decoupled to both SSTL2_VDD and SSTL2_GND with balanced decoupling capacitors.

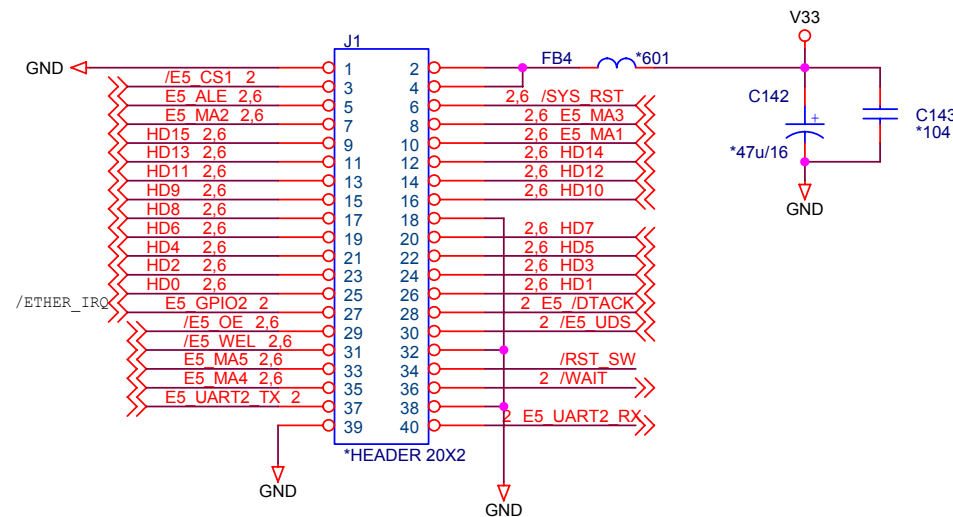
VREF should be routed over a reference plane and isolated, and possibly shielded with both SSTL2_VDD and SSTL2_GND



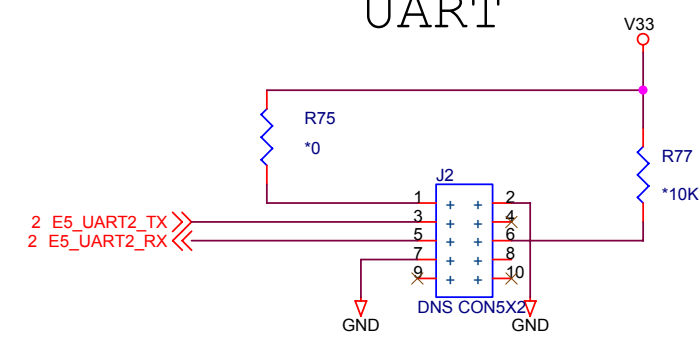


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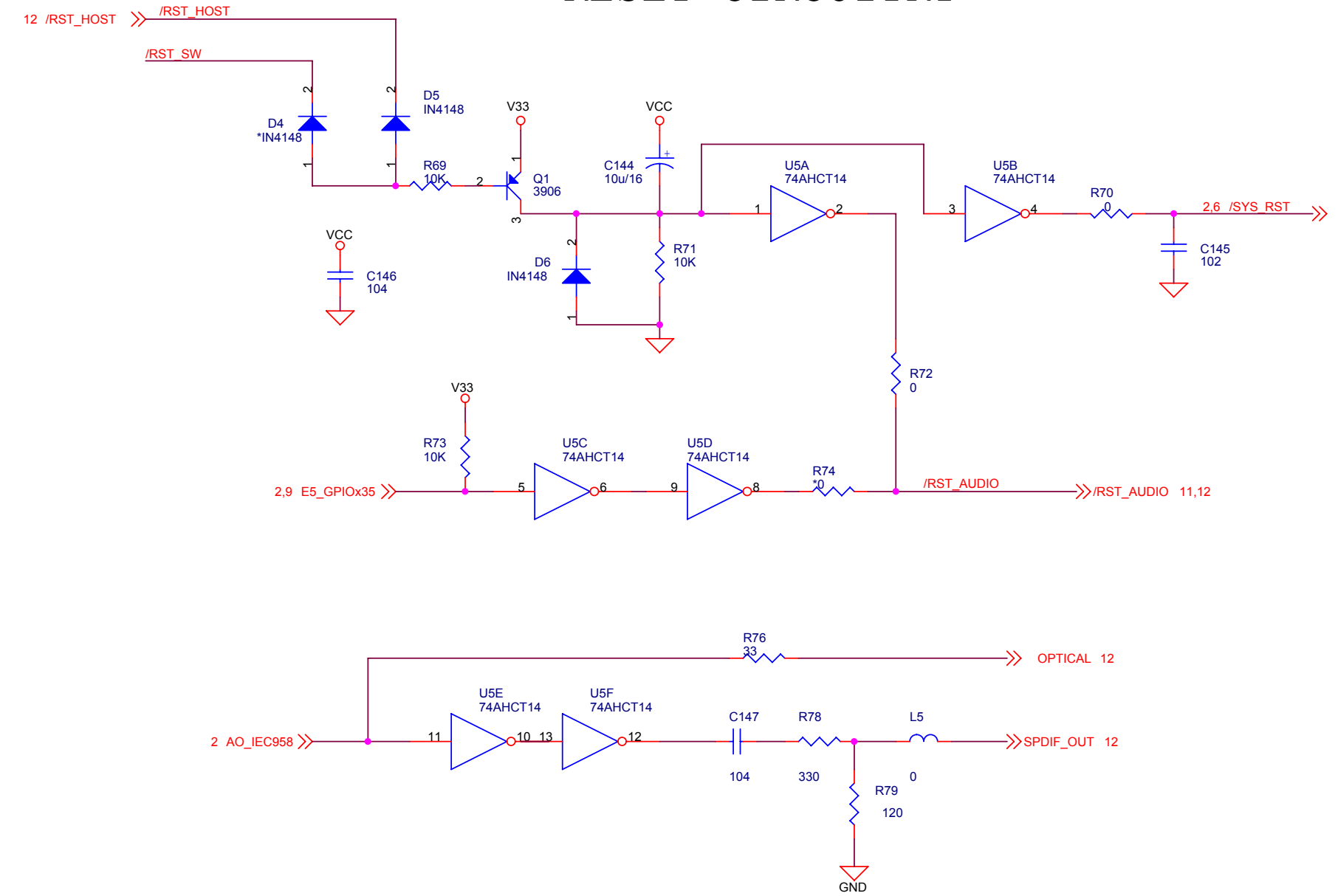
E-Link III Connector



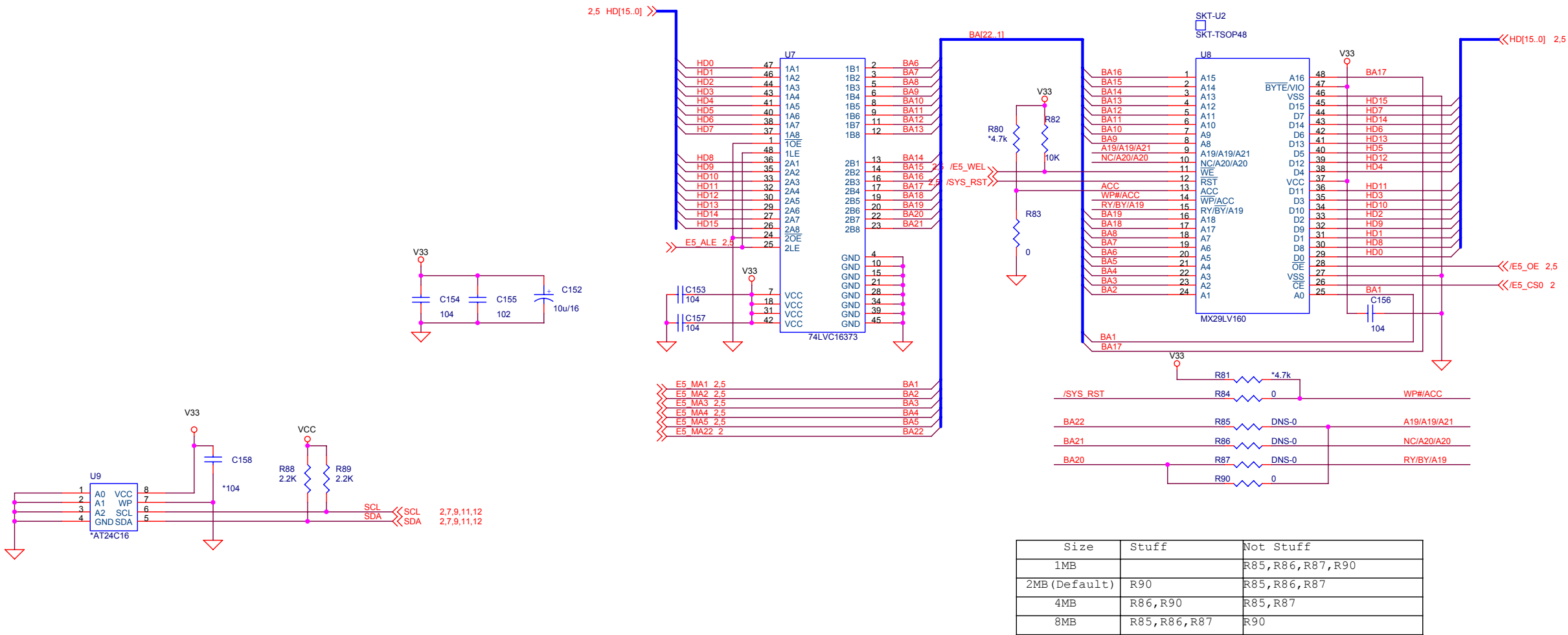
UART



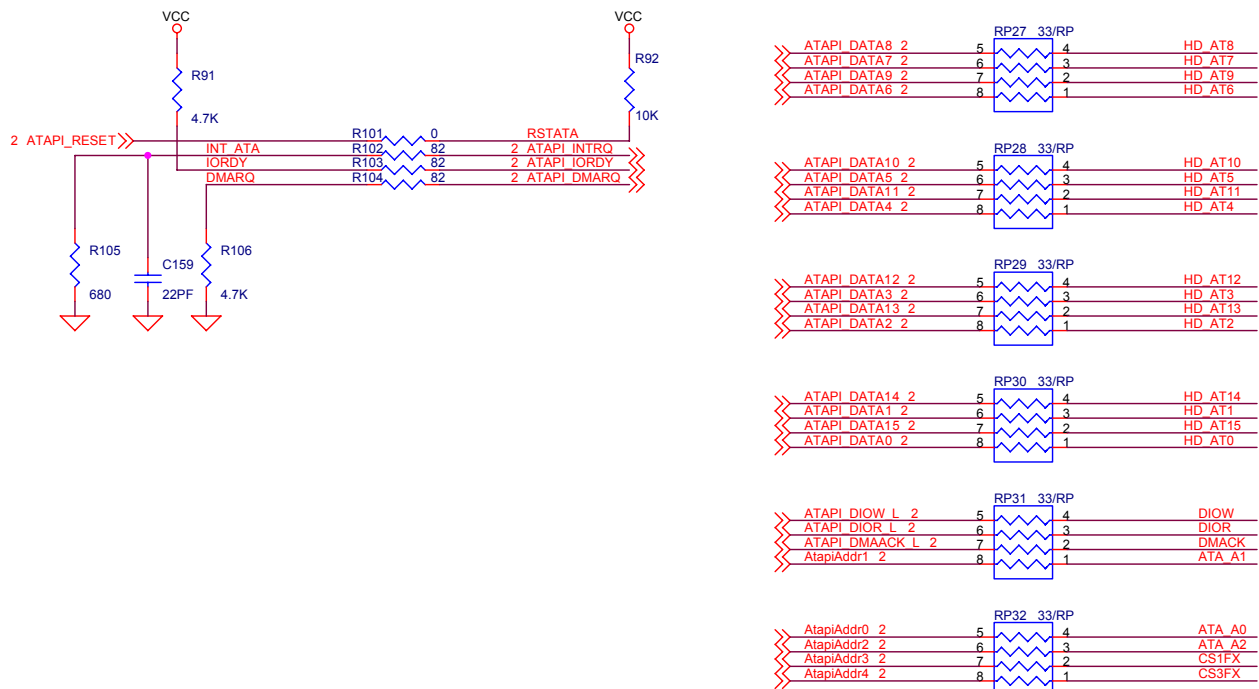
RESET CIRCUITRY



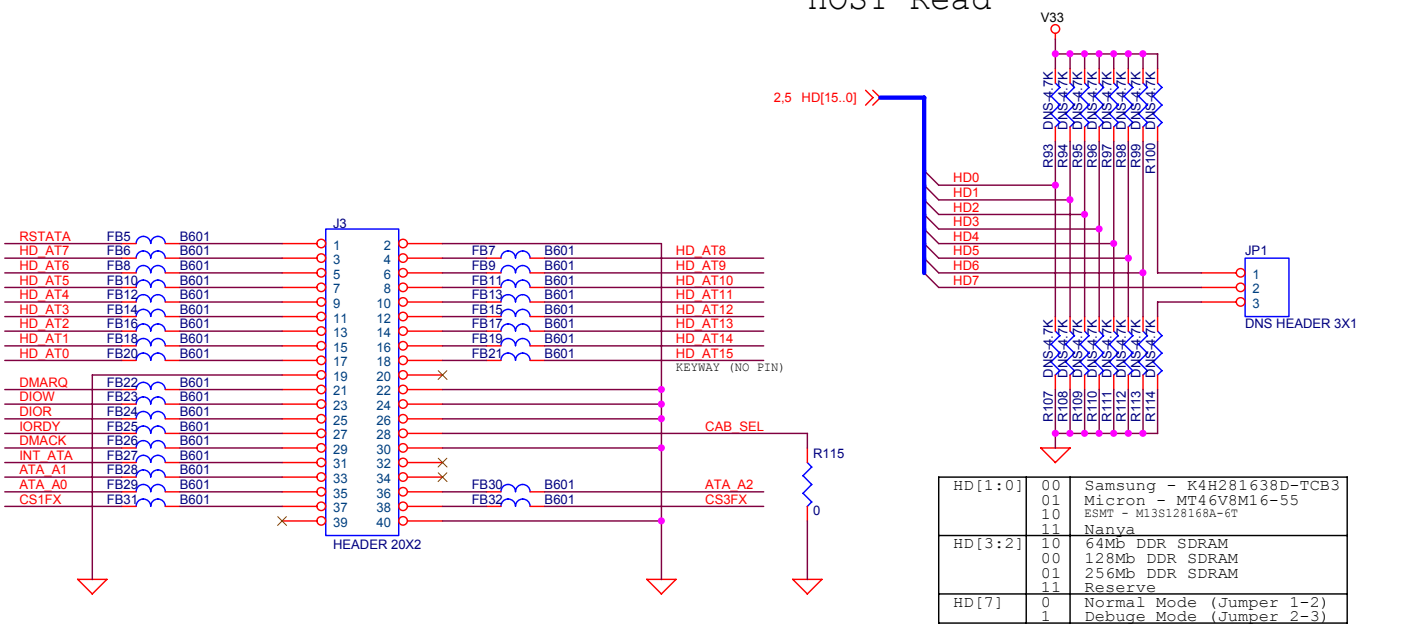
FLASH MEMORY (2 or 4 or 8 Mb)



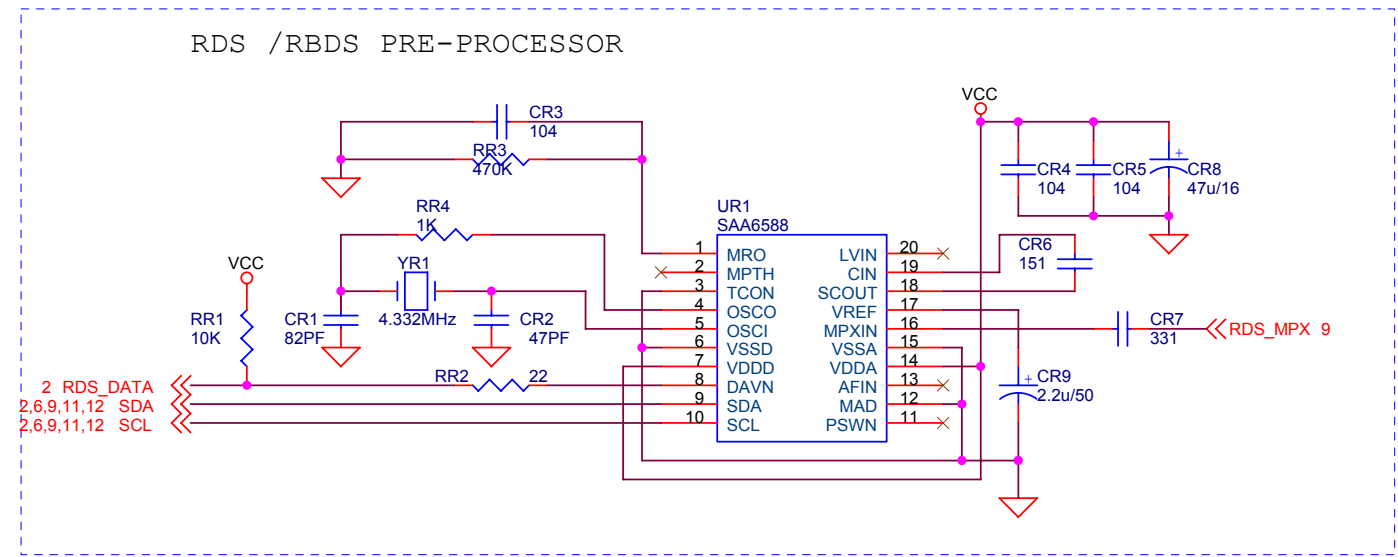
DEDICATED ATAPI INTERFACE



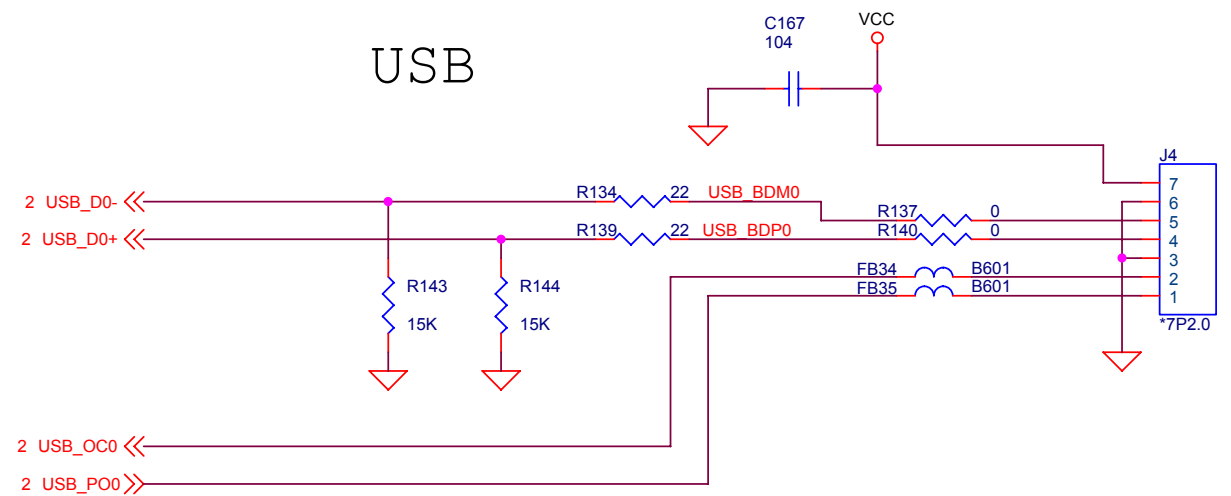
HOST Read



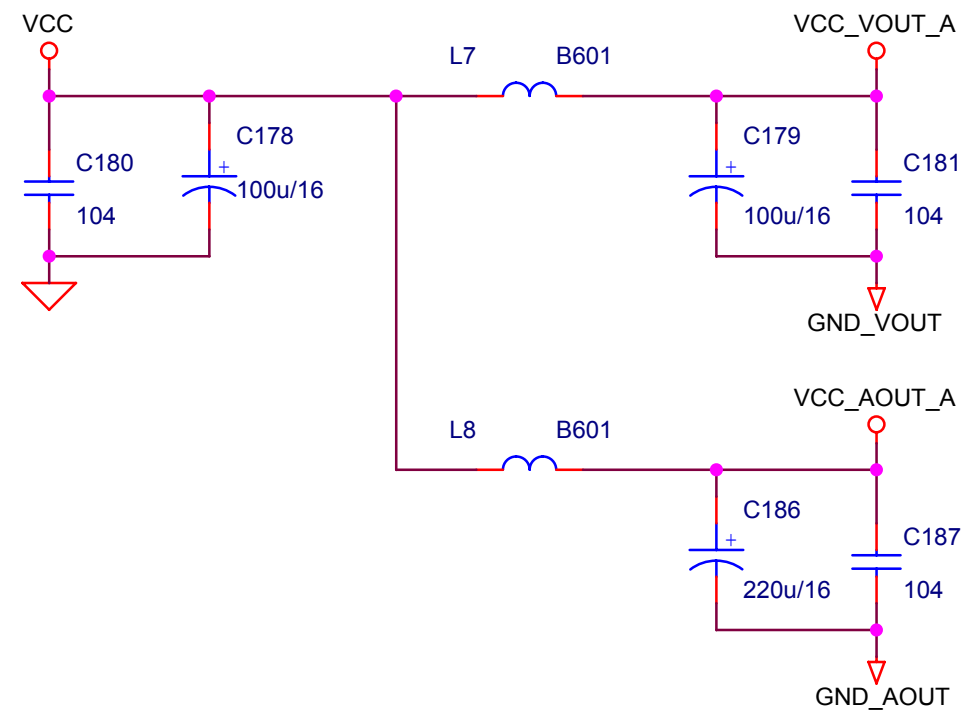
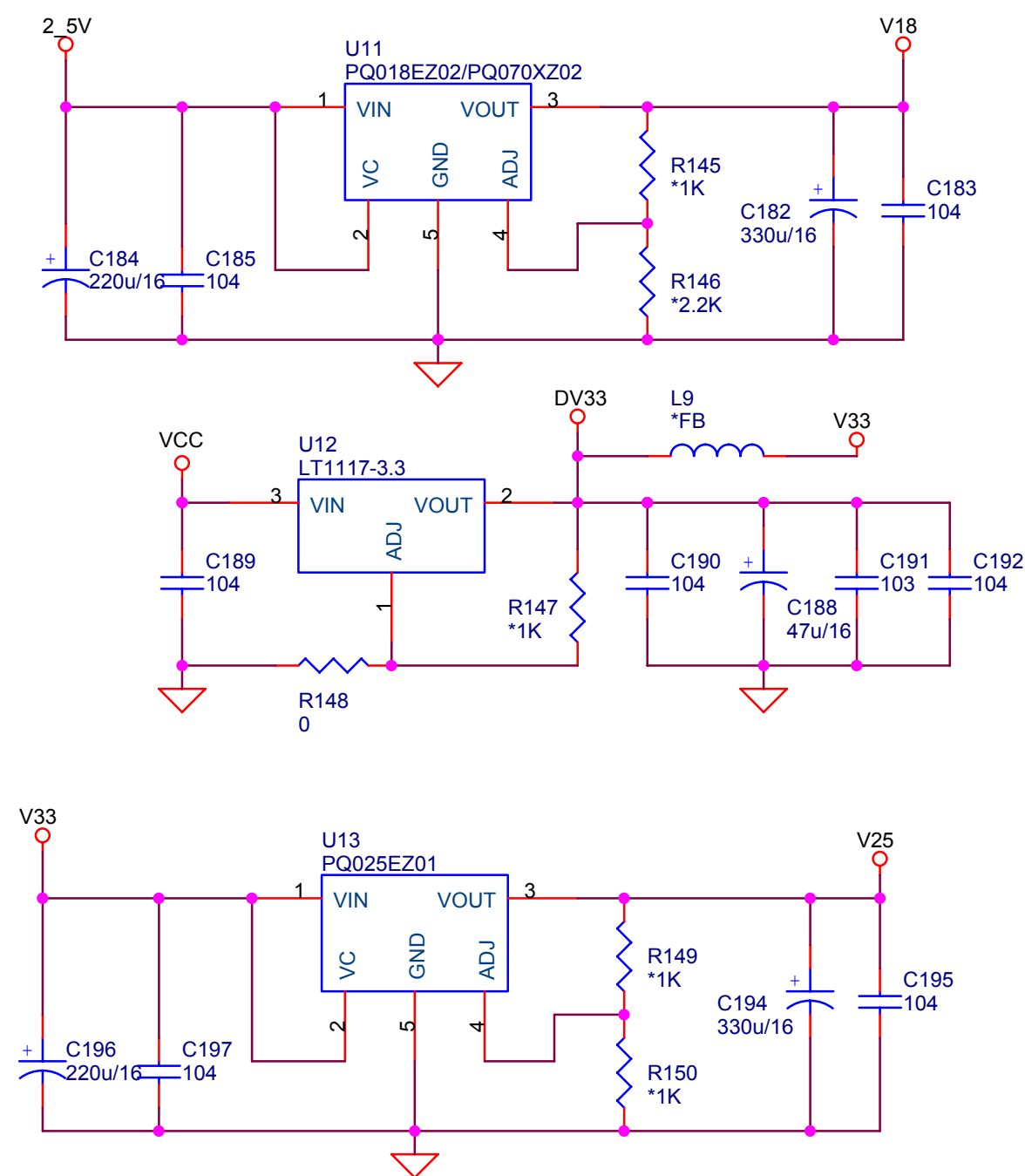
FIREWIRE PHY



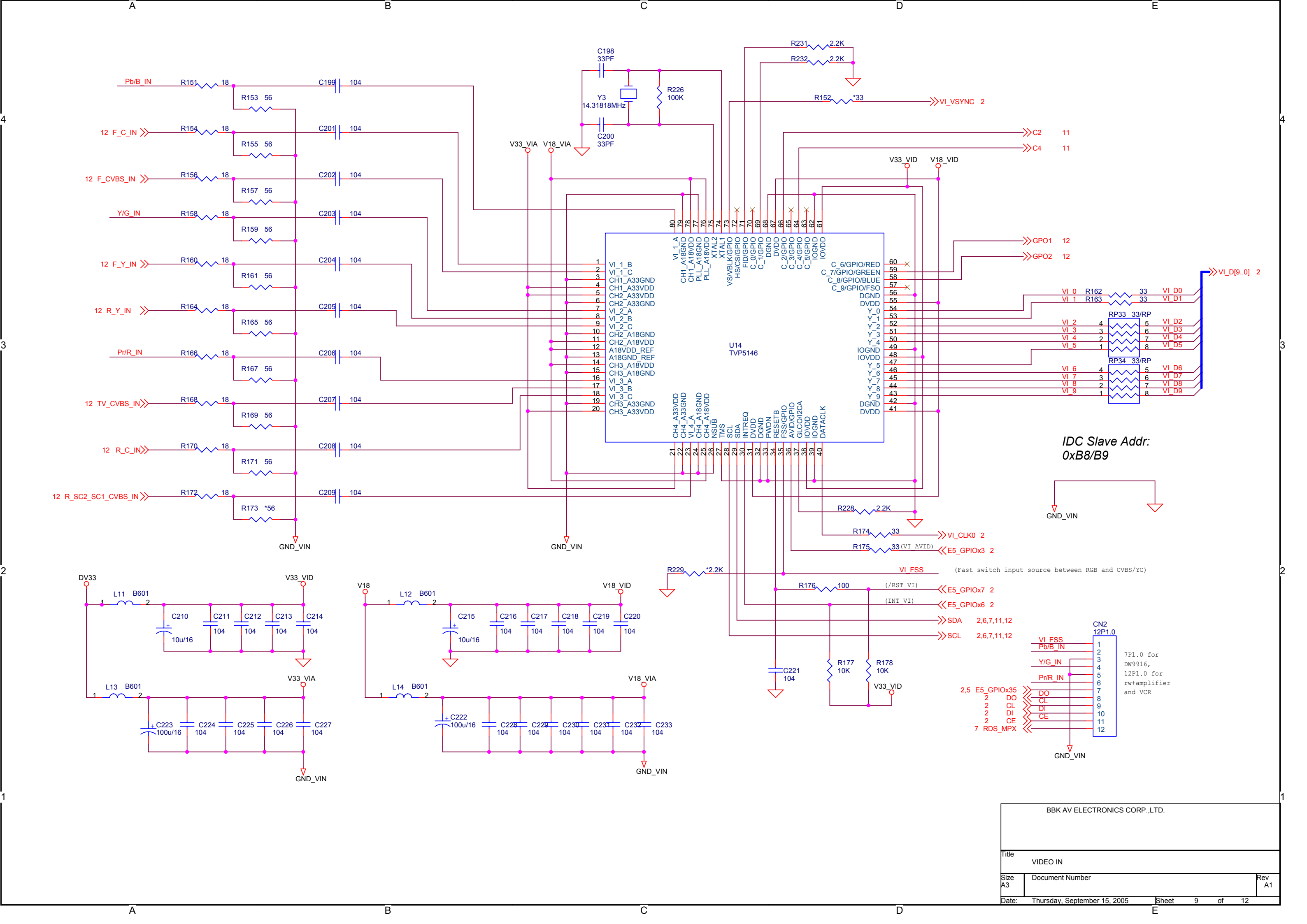
USB

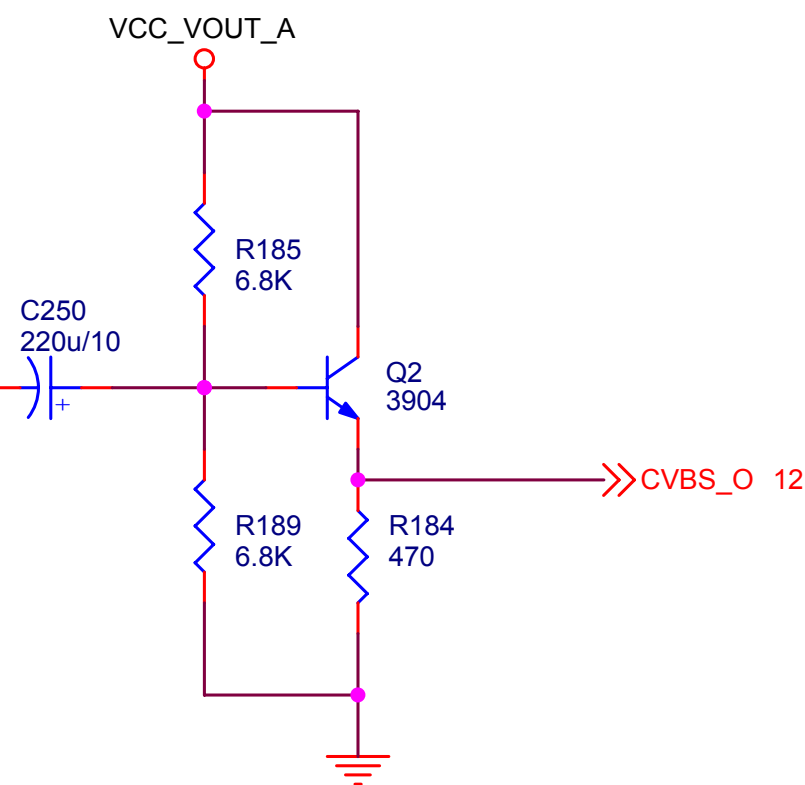
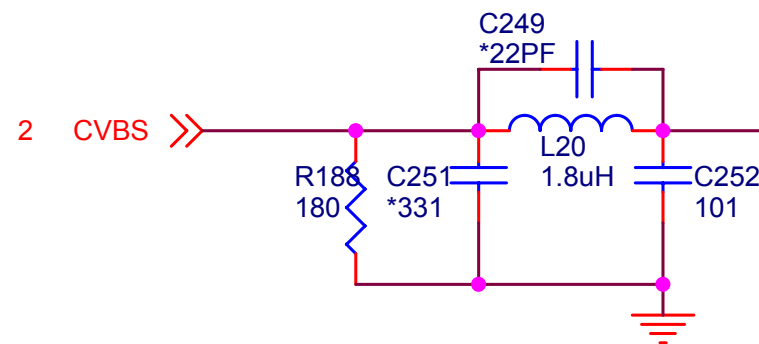
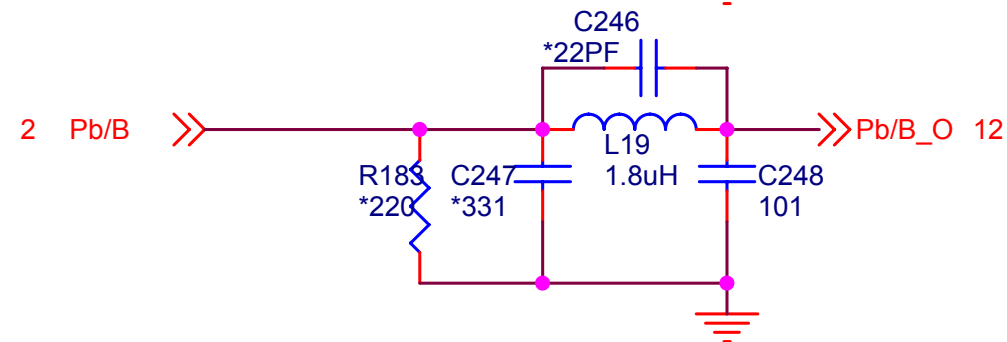
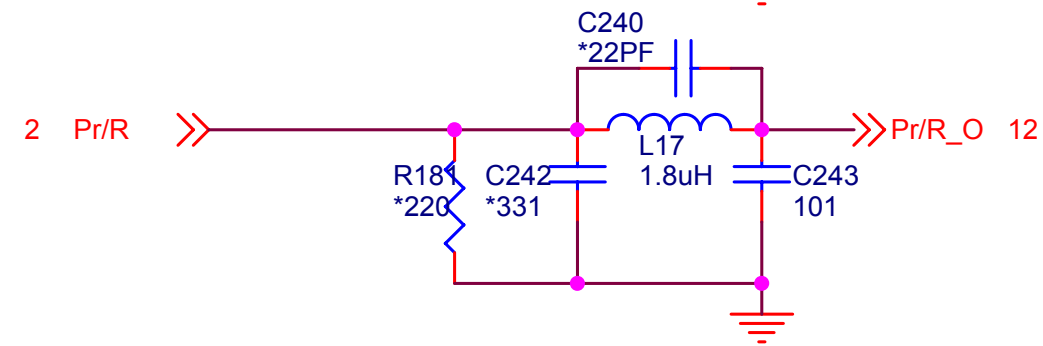
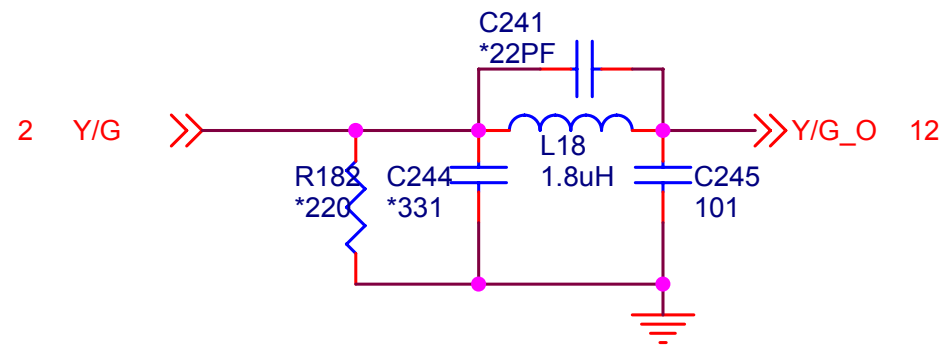
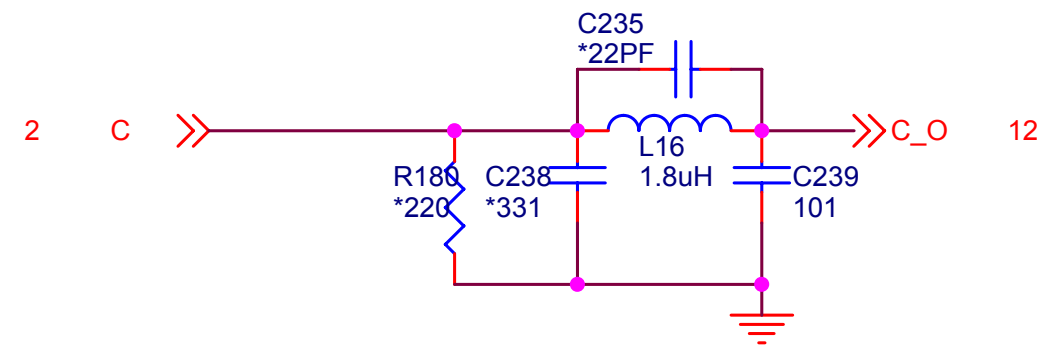
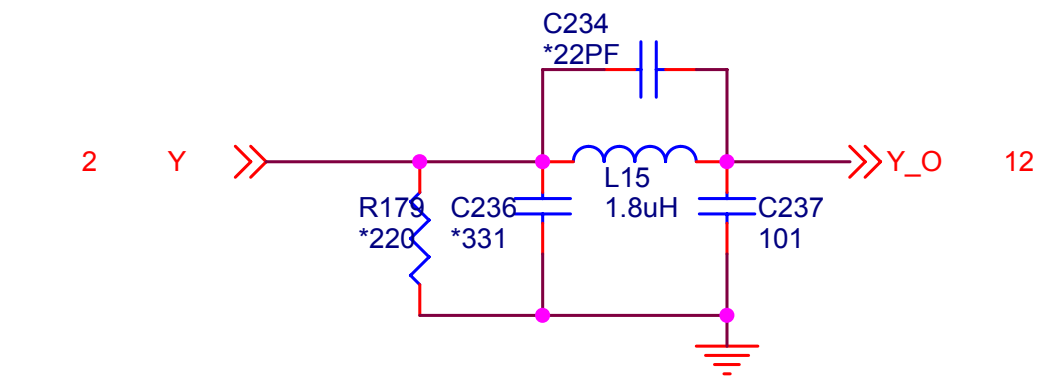


MAIN POWER REG



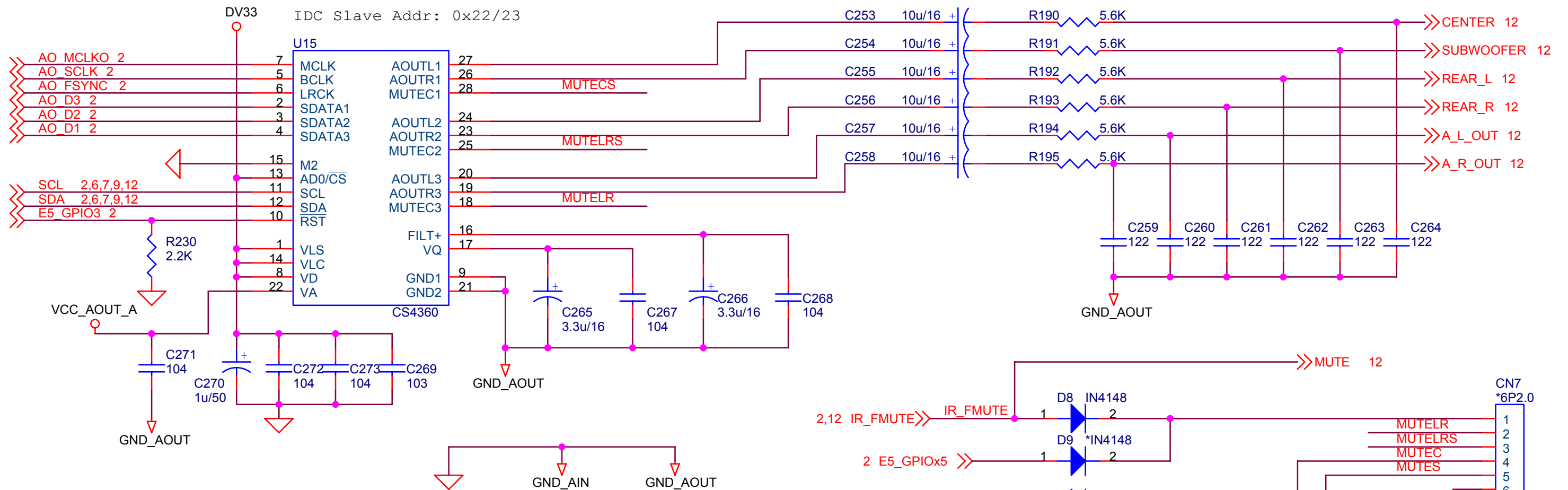
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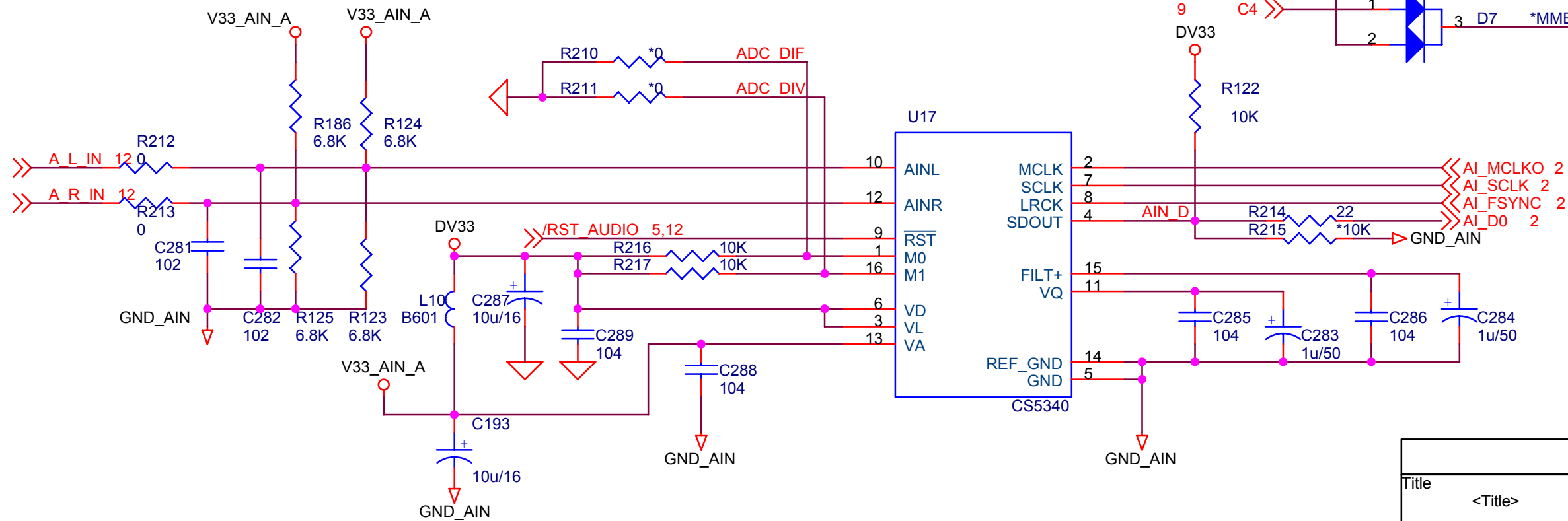


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Audio Out (2 & 6 ch)

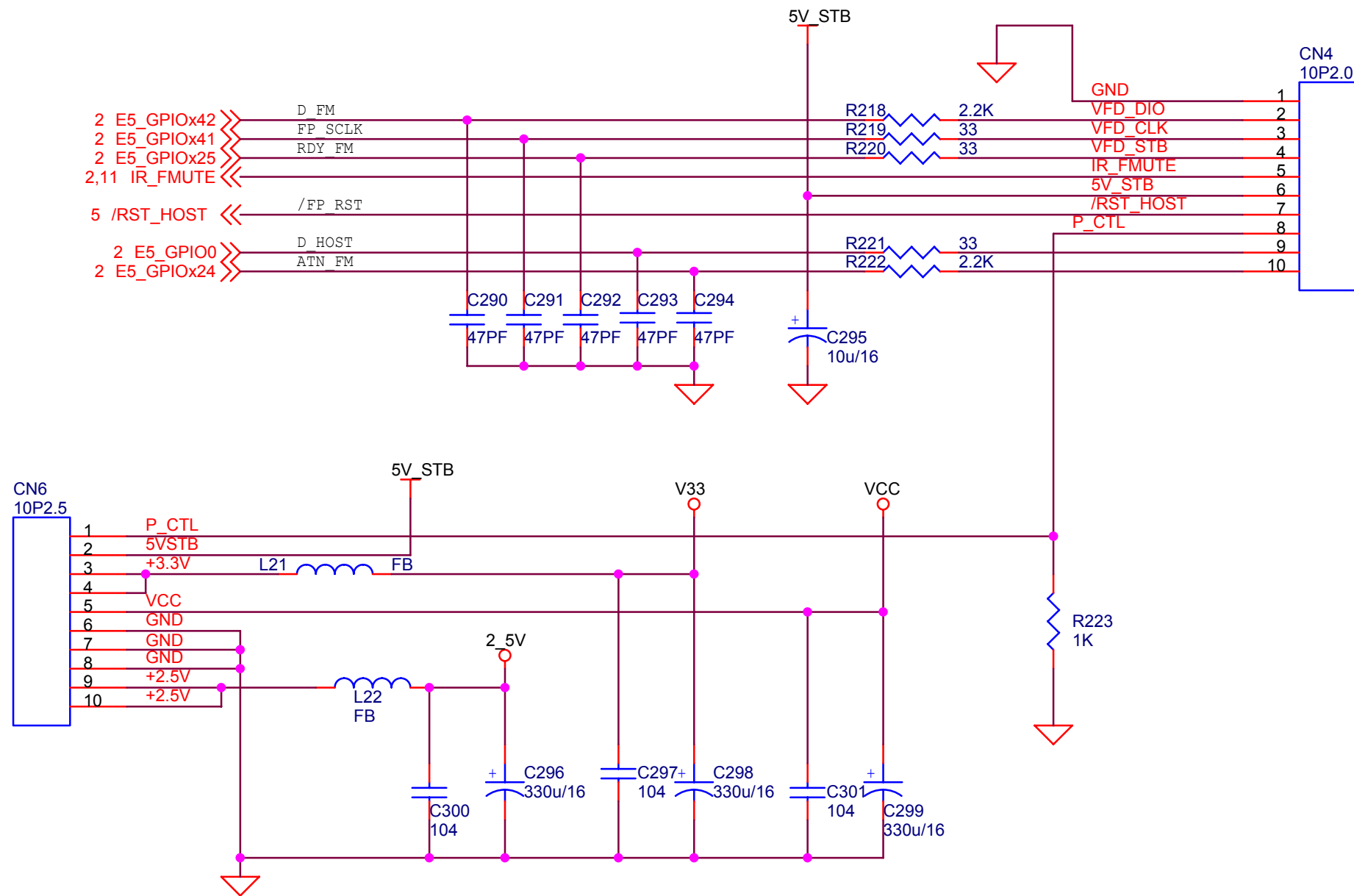


Audio In

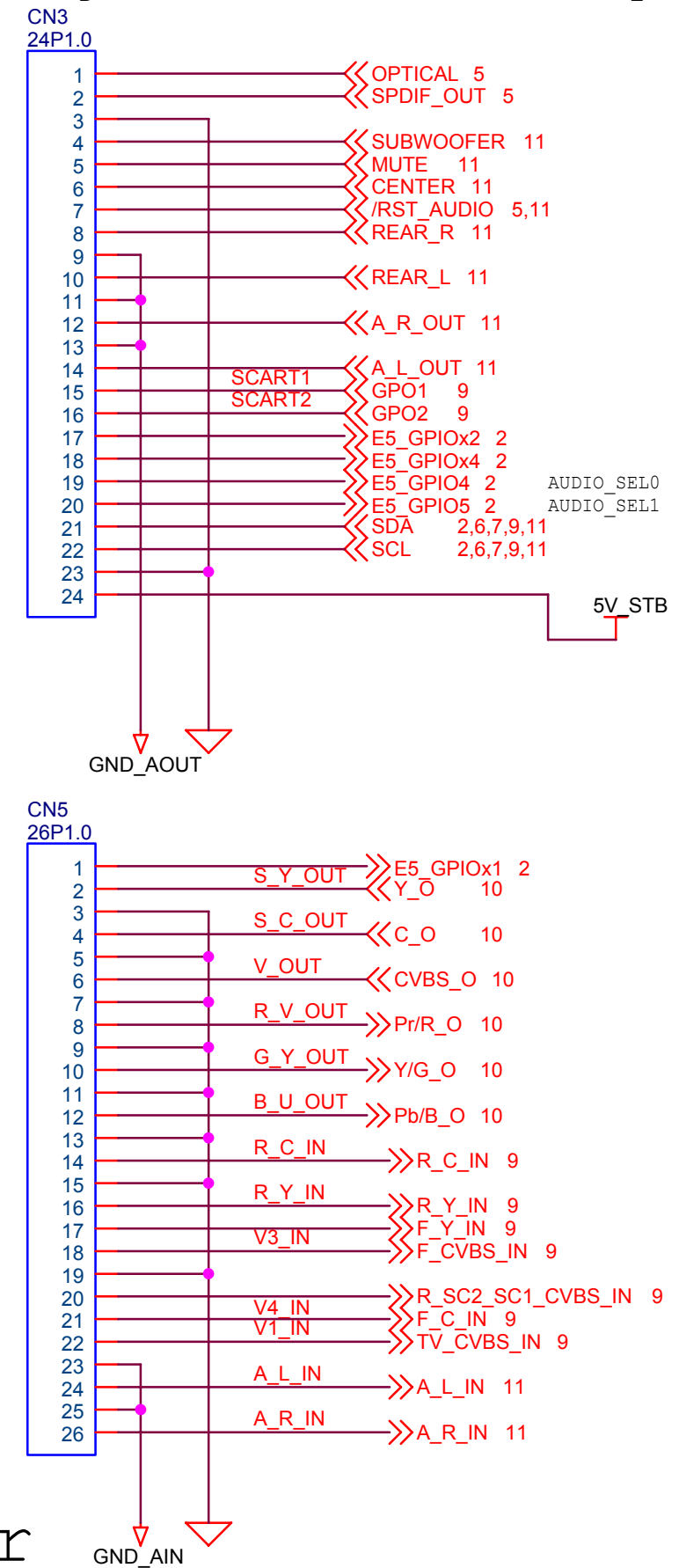


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FRONT PANEL INTERFACE



A/V I/O Connector



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