SERVICE MANUAL

DW9937S

Ver 0.0

INDEX

PREFACE

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BASIC INFORMATION

Features

Introducing American LSI (C-CUBE) Company's latest So C AV system (AVS) recorder processor this unit is, capable of recording all kinds of AV input signals, such as TV, ordinary VCD and DV video camera, into high quality DVD disc. In addition, this player is also a high capacity DVD player, capable of realizing all functions of ordinary DVD player. His 2-in-1 init will make your life more enjoyable and wonderful.

Support multiple input sources recording

1 Composite video input
2 S-video input
3 TV tuner input
4 DV input
5 Analog audio terminal input
6.SCART input

Provide multiple output signals

1.Composite video output
2.S-video output
3.Component video output
4.SCART output
5.L/R double audio channels output
6.Optical / Coaxial output

Multiple DVD recording qualities

This unit provides you with 4 kinds of recording qualities, each of which has different resolution and recording time, to make you choose between high resolution picture quality and super long time of recording.

Multiple recording methods

This unit facilitates your usage with three kinds of recording methods: ordinarily manual recording, time recording, OTR one-touch recording and DV recording.

Convenient menu operation

This unit incorporates convenient interface menu operation. No need for you to remember the multifarious function buttons on remote control, and you can realize the majority of functions through using a few direction and selection buttons.

Standby function

Remote control standby function makes your operation more convenient and helps you fulfill time recording function on the basis of saving electric power.

Highly intelligent upgrading function

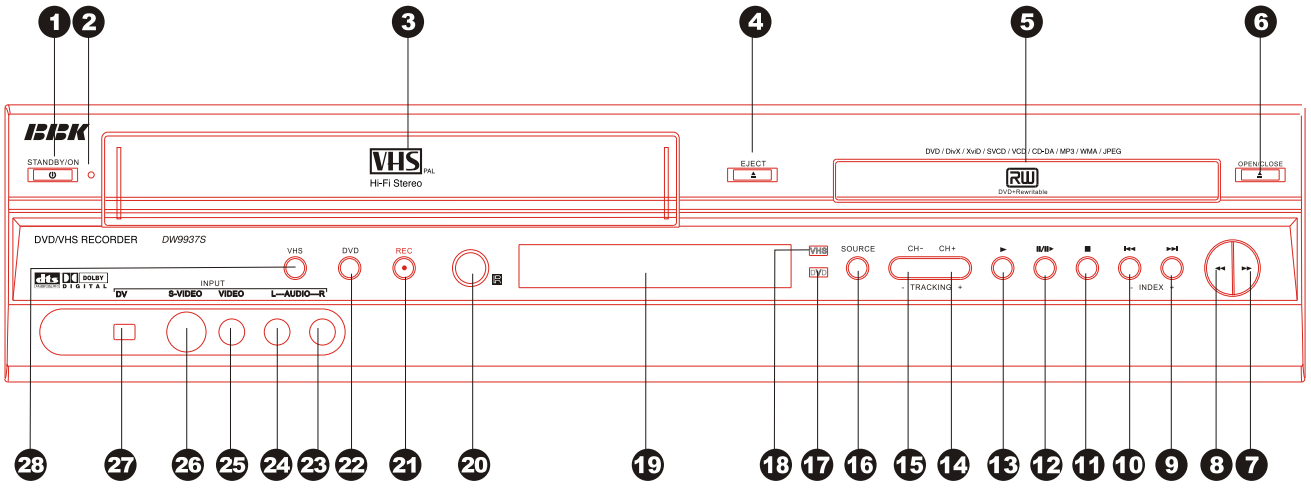
This unit has automatic upgrading function to make you upgrade it into the latest edition with our upgrading disc at any time.

This player can use the following discs

This unit can play DVD, DVD+R, DVD+RW, VCD, SVCD, CD-DA and MP3.
This unit can record DVD+R and DVD+RW

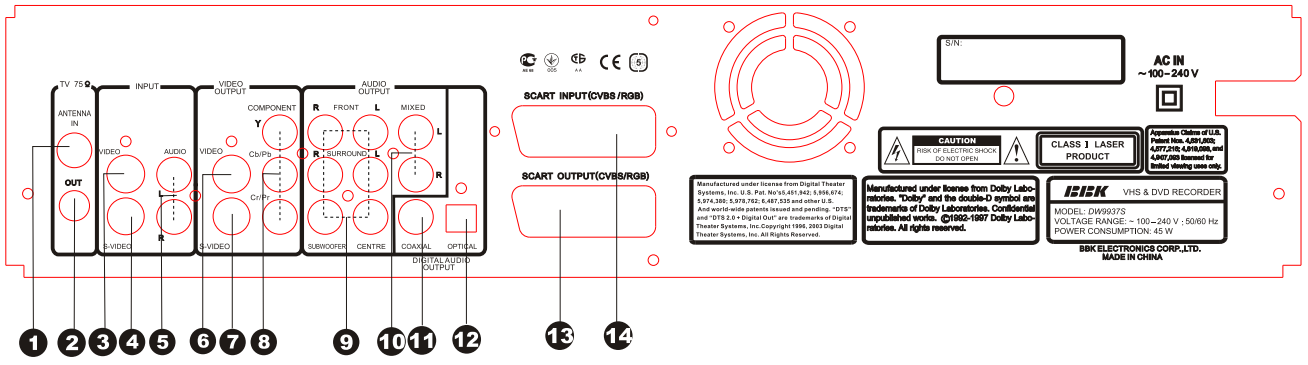
BASIC INFORMATION

Illustration of the Front Panel



1. STANDBY/ON button
2. STANDBY indicator
3. Tape window
4. Tape eject button
5. Disc tray
6. Disc OPEN/CLOSE button
7. FWD button
8. REW button
9. NEXT/INDEX + button
10. PREV/INDEX- button
11. STOP button
12. PAUSE/STEP button
13. PLAY button
14. CH+/TRACKING+ button
15. CH-/TRACKING- button
16. SOURCE button
17. DVD working mode indicator
    - ※ The indicator lighting indicates this unit is working as a DVD Recorder.
    - ※ Flashing shows recording contents of tape to DVD disc.
18. VHS working mode indicator
    - ※ The indicator lighting indicates this unit is working as a VHS.
    - ※ Flashing shows recording contents of disc to tape .
19. VFD display window
20. Infrared remote sensor
21. RECORD button
22. DVDR mode switching button
23. Right audio channel input terminal
24. Left audio channel input terminal
25. Front Video input terminal
26. Front S-Video input terminal
27. DV input terminal
28. VHS mode switching button

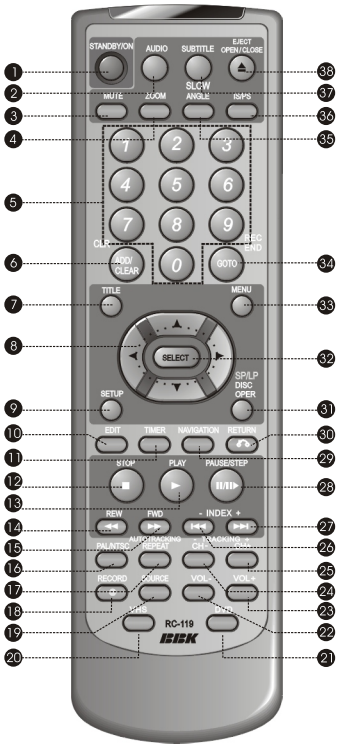
Illustration of the Rear Panel



1. TV TUNER input terminal
   - ※ The antenna cable plug is inserted here
2. TV TUNER output terminal
   - ※ This terminal is directly connected with the TV TUNER Input Terminal inside this unit
3. Rear Video input terminal
4. Rear S-Video input terminal
5. L/R channel audio input terminals
6. COMPOSITE VIDEO output terminal
7. S-VIDEO output terminal
8. COMPONENT VIDEO output terminals
9. 5.1 CH output terminals
10. Mixed L/R channel audio output terminal
11. COAXIAL output terminal
12. OPTICAL output terminal
13. SCART output terminal
14. SCART in/output terminal

BASIC INFORMATION

Illustration of the Remote Control



31 DISC OPER (SP/LP)button

※ Enter the disc operate mode in DVD mode.

※ Switch record quality in VHS recording mode .

32 SELECT button

Confirm the selected item

33 MENU button

※Display the disc menu

※Open/close PBC function

34 GOTO(REC END) button

※ Play from the desire location in DVD mode.

※ Seach the start position of the blank in the tape in VHS mode.

35 ANGLE (SLOW)button

※ Change the viewing angle in DVD mode.

※ In VHS mode, you can slow the normal playback speed by this button. To resume normal playback, press the PLAY(13)button.

36 IS/PS button

Switch between progressive scan and interlacing scan

37 SUBTITLE button

Change subtitle languages

38 OPEN/CLOSE button

Open or close the disc tray

21 DVD button

Switch to DVD working mode

22 VOL- button

Decrease volume

23 VOL+ button

Increase volume

24 CH-(TRACKING-) button

※ Switch to previous channel in the mode of receiving TV programs.

※ In VHS slow playing mode, this button and TRACKING+ button(25) perform the mannual tracking adjusting

Digital auto tracking: When a playback starts, the VHS automatically adjusts the tracking for clear pictures and sound .If the VHS cannot locate the best possible tracking point during playback, hold down button 24 or 25 until you obtain the best possible picture and sound. If the picture flickers or is distorted, hold down button 24 or 25 in the slow or still mode until the picture stabilizes.

NOTES

- Picture noises, flickers or distortion may not be completely eliminated with this adjustment.
- Pressing button 24 or 25 will prohibit auto tracking

25 CH+(TRACKING+) button

※ Switch to next channel in the mode of receiving TV programs .

※ In VHS slow playing mode, this button and [TRACKING-] button(24) perform tracking adjusting function.

26 PREV(INDEX-)button

※ Skip backward in DVD working mode.

※ Search the previous index signal in the tape in VHS playing mode .

27 NEXT (INDEX+)button

※ Skip forward in DVD working mode.

※ Shearch the next index signal in the tape in VHS playing mode .

28 PAUSE/STEP button

Pause or play frame by frame

29 NAVIGATION button

Display/hide menu

30 RETURN button

Back to the previous menu

1 STANDBY/ON button

Switch between standby state and working state

2 AUDIO button

※Switch the audio channel

※Switch the audio stream

3 MUTE button

Enable or disable audio output

4 ZOOM button

Enlarge the DVD/VCD picture

5 NUMBER buttons

6 ADD/CLEAR (CLR) button

※ Add/Clear the content items in the list window or clear the wrong input numbers in DVD working mode.

※ Clear the time counter in VHS working mode.

7 TITLE button

Display DVD titles menu

8 CURSOR buttons

Move the cursor

9 SETUP button

System setup

10 EDIT button

Enter/quit the edit mode

11 TIMER button

Enter/quit the timing record setup

12 STOP button

Stop playing/recording

13 PLAY button

14 REW button

Fast backward play

15 Forward button

Fast forward play

16 PAL/NTSC button

Switch the between PAL and NTSC output system

17 REPEAT (AUTO TRACKING) button

※ Repeat playback in DVD working mode

※ Perform digital auto tracking in VHS working mode. After pressing 24 or 25 button, the auto tracking will stop, and then you can resume it by pressing this button.

18 RECORD button

Record the external signals

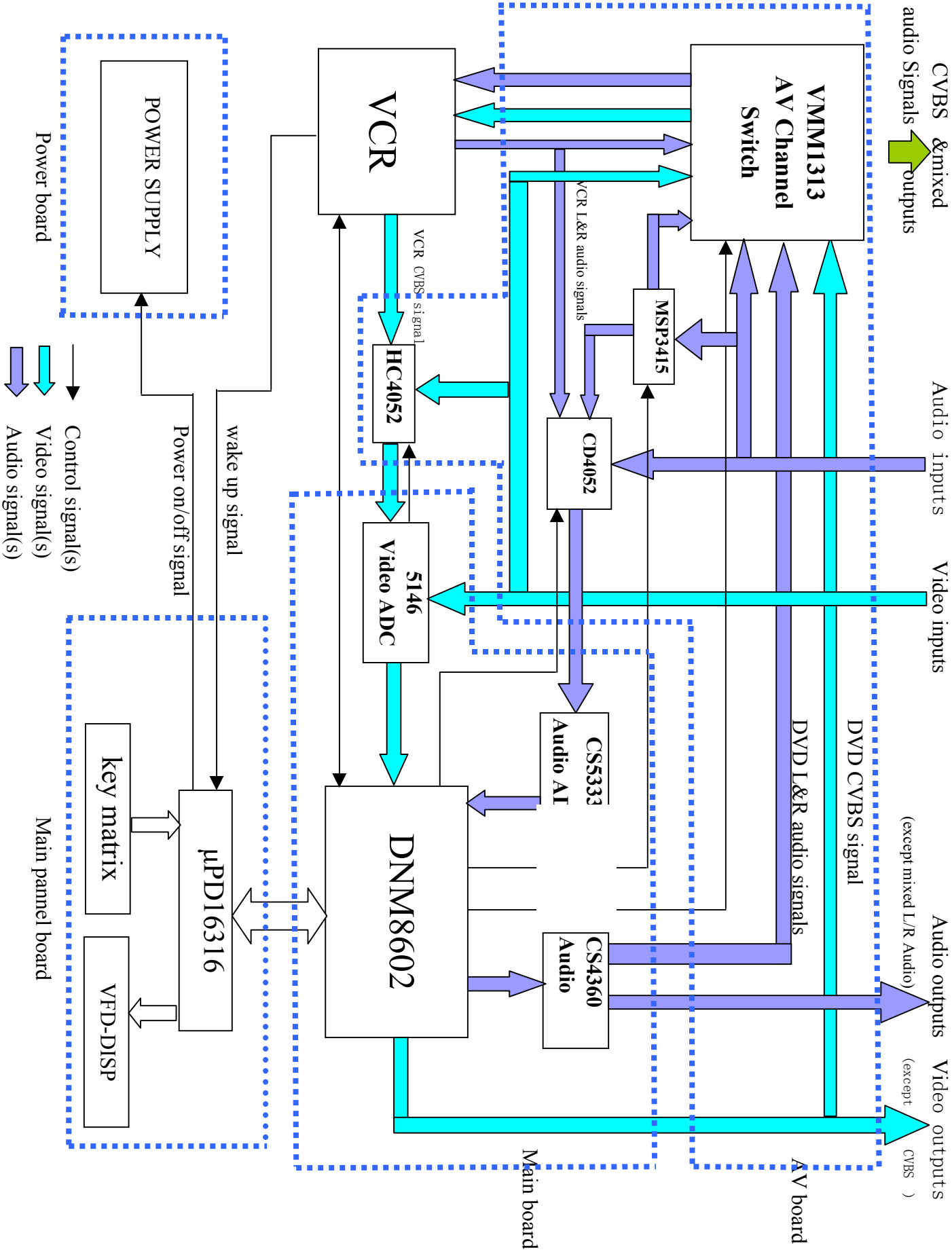
19 SOURCE button

Enter monitoring mode, switch external input signal source.

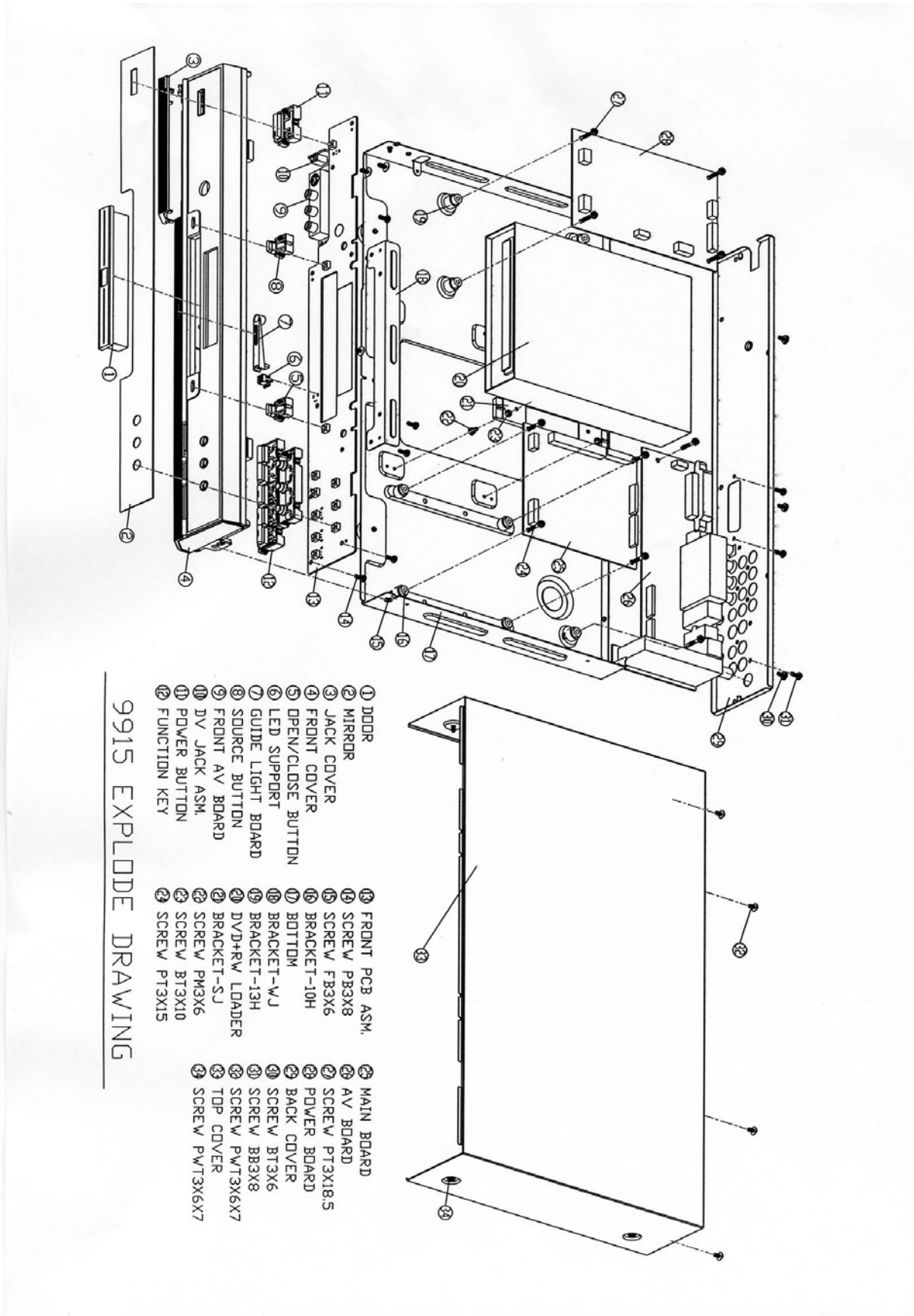
20 VHS button

Switch to VHS working mode

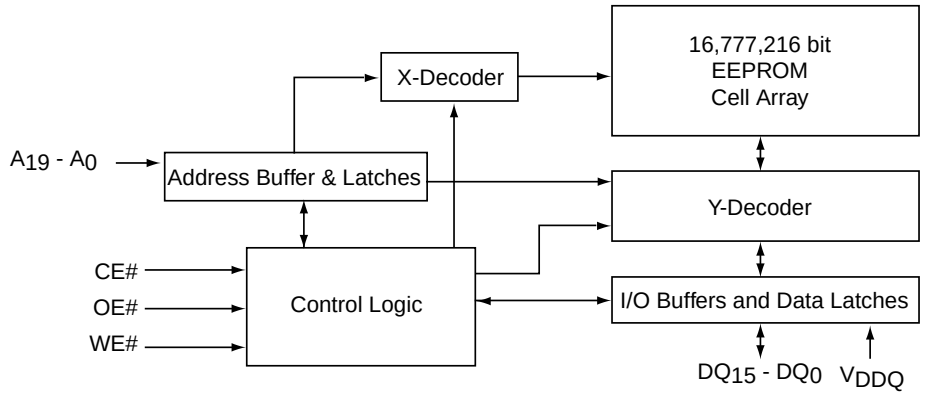
BLOCK DIAGRAM



EXPLODED VIEW



FUNCTIONAL BLOCK DIAGRAM



329 ILL B1.2

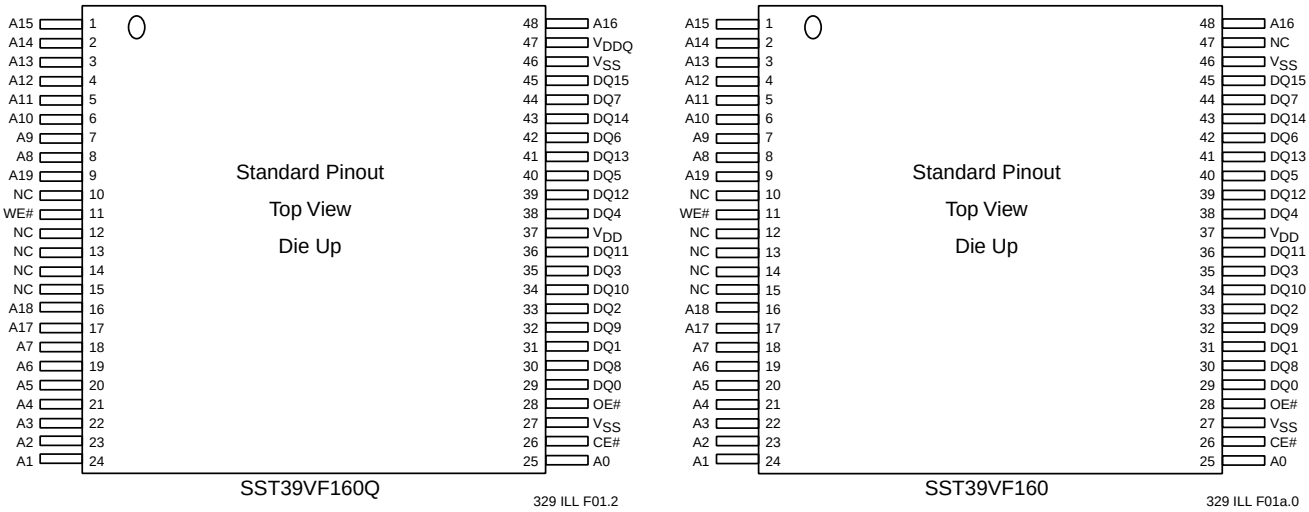


FIGURE 1: PIN ASSIGNMENTS FOR 48-PIN TSOP PACKAGES

	1	2	3	4	5	6
A	A3	A7	NC	WE#	A9	A13
B	A4	A17	NC	NC	A8	A12
C	A2	A6	A18	NC	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	DQ0	DQ2	DQ5	DQ7	A16
F	CE#	DQ8	DQ10	DQ12	DQ14	V_{DDQ}
G	OE#	DQ9	DQ11	V_{DD}	DQ13	DQ15
H	V_{SS}	DQ1	DQ3	DQ4	DQ6	V_{SS}

SST39VF160Q

329 ILL F02.4

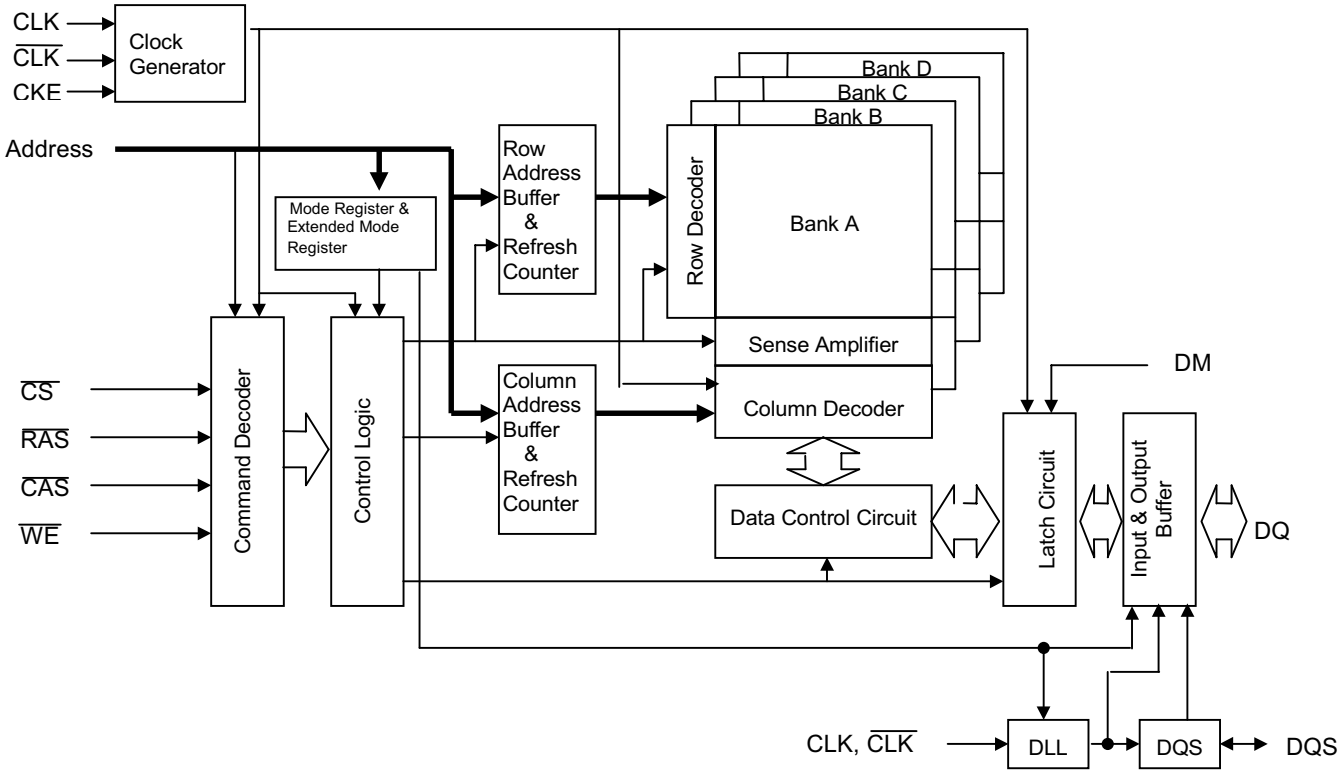
	1	2	3	4	5	6
A	A3	A7	NC	WE#	A9	A13
B	A4	A17	NC	NC	A8	A12
C	A2	A6	A18	NC	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	DQ0	DQ2	DQ5	DQ7	A16
F	CE#	DQ8	DQ10	DQ12	DQ14	NC
G	OE#	DQ9	DQ11	V_{DD}	DQ13	DQ15
H	V_{SS}	DQ1	DQ3	DQ4	DQ6	V_{SS}

SST39VF160

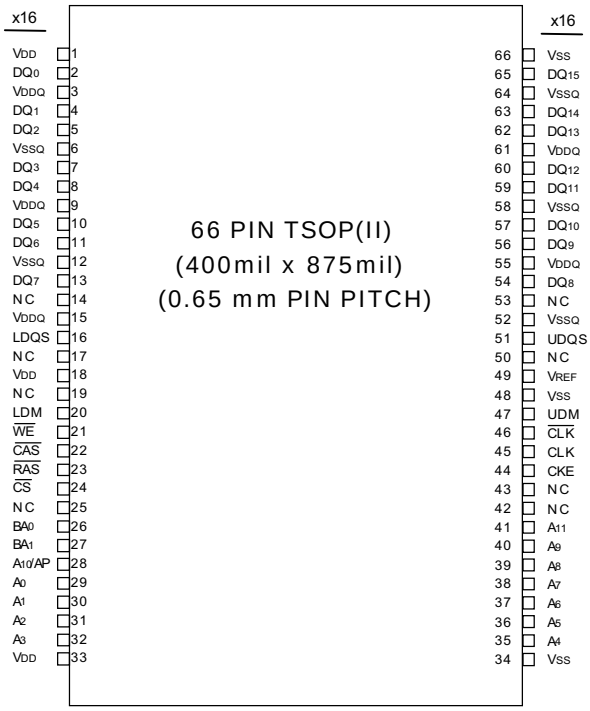
329 ILL F02a.0

FIGURE 2: PIN ASSIGNMENTS FOR 48-PIN TFBGA

Functional Block Diagram



Pin Arrangement



description (continued)

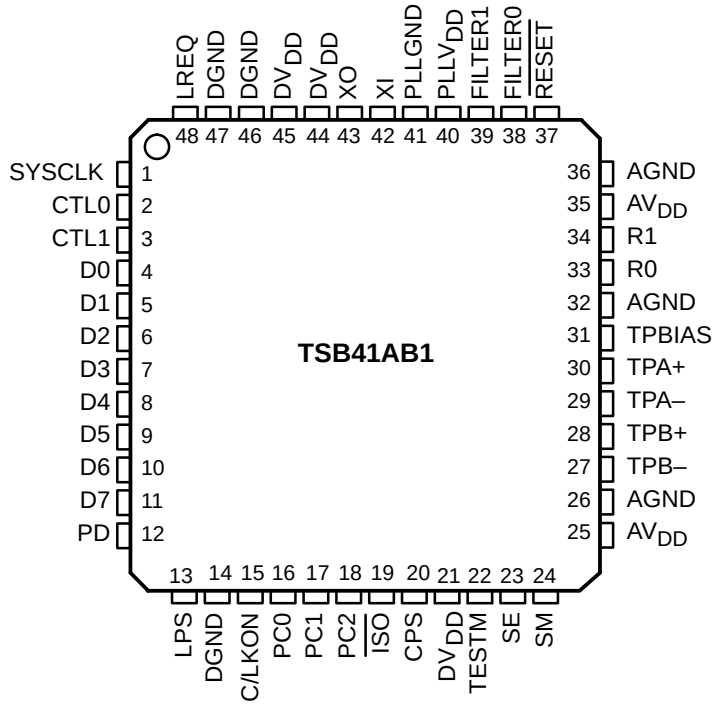
required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY initializes the interface and returns it to normal operation.

When the PHY-LLC interface is in the low-power disabled state, the TSB41AB1 automatically enters a low-power mode if the port is inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB41AB1 disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the port (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the ultralow-power sleep mode) is attained when the port is either disconnected, or disabled with the port interrupt enable bit cleared. The TSB41AB1 exits the low-power mode when the LPS input is asserted high or when a port event occurs which requires that the TSB41AB1 become active in order to respond to the event or to notify the LLC of the event (for example, incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The SYSCLK output becomes active (and the PHY-LLC interface is initialized and becomes operative) within 7.3 ms after LPS is asserted high when the TSB41AB1 is in the low-power mode.

The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163-ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts the C/LKON output when a bus reset occurs unless a PHY interrupt condition exists which would otherwise cause C/LKON to be active.

PHP package terminal diagram

PHP PACKAGE
(TOP VIEW)



1.5 Functional Block Diagram

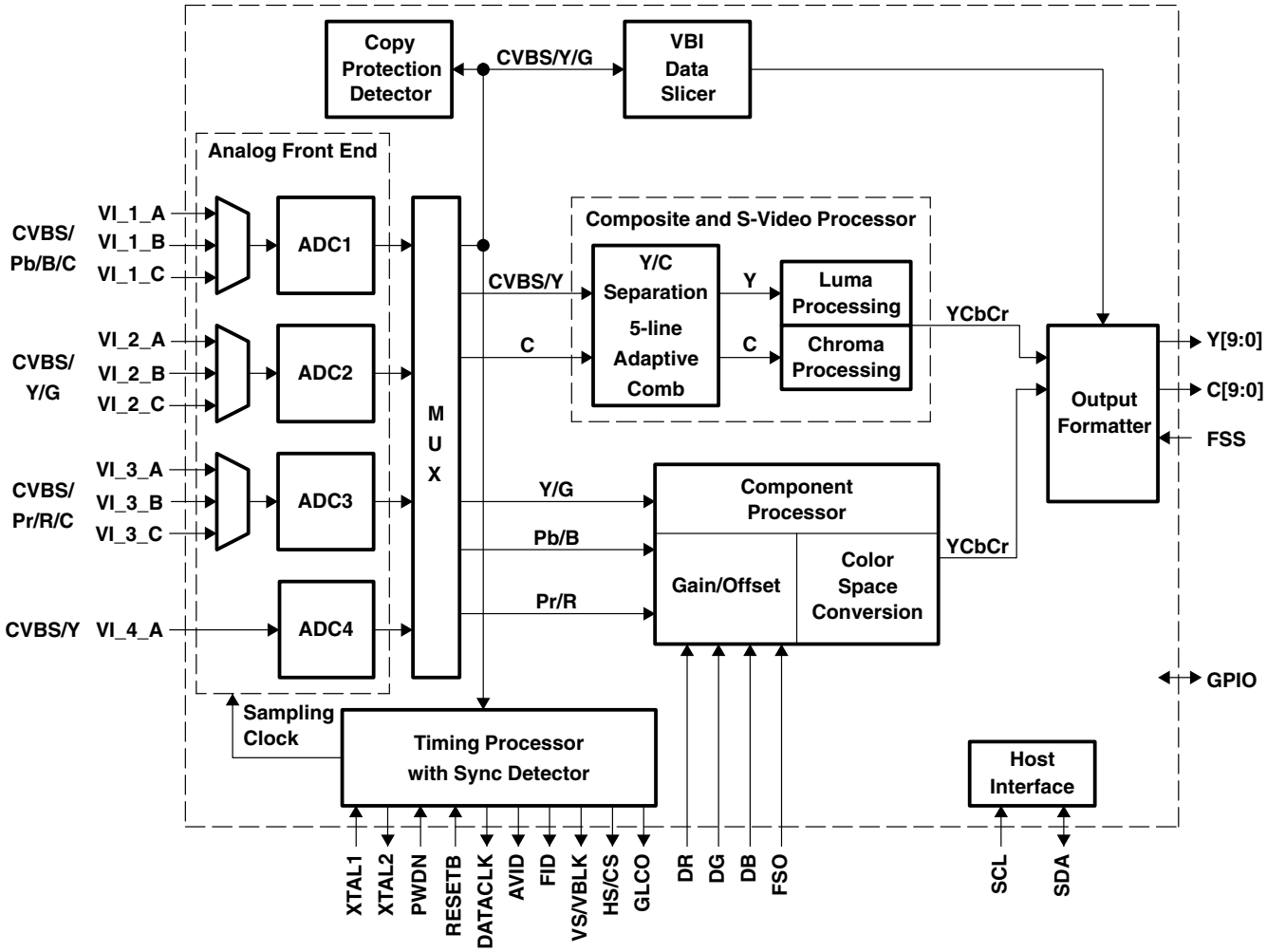


Figure 1–1. Functional Block Diagram

1.6 Terminal Assignments

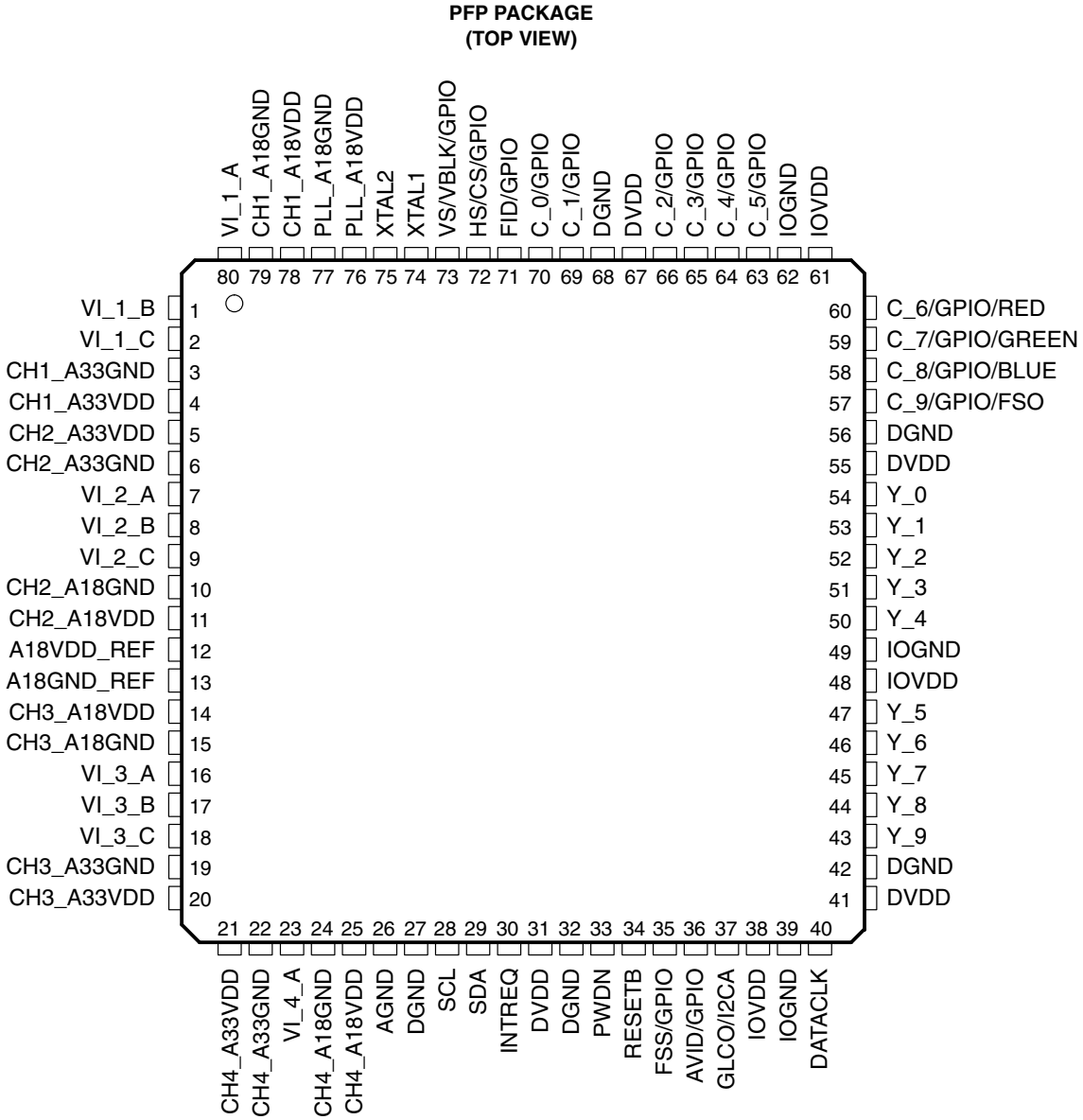


Figure 1–2. Terminal Assignments Diagram

1.7 Terminal Functions

Table 1–1. Terminal Functions

TERMINAL NAME	TERMINAL NUMBER	I/O	DESCRIPTION
Analog Video			
VI_1_A VI_1_B VI_1_C VI_2_A VI_2_B VI_2_C VI_3_A VI_3_B VI_3_C VI_4_A	80 1 2 7 8 9 16 17 18 23	I	VI_1_x: Analog video input for CVBS/Pb/B/C VI_2_x: Analog video input for CVBS/Y/G VI_3_x: Analog video input for CVBS/Pr/R/C VI_4_A: Analog video input for CVBS/Y Up to 10 composite, 4 S-video, and 2 composite or 3 component video inputs (or a combination thereof) can be supported. The inputs must be ac-coupled. The recommended coupling capacitor is 0.1 μF. The possible input configurations are listed in the input select register at I^2C subaddress 00h (see Section 2.11.1).
Clock Signals			
DATACLK	40	O	Line-locked data output clock.
XTAL1	74	I	External clock reference input. It may be connected to an external oscillator with a 1.8-V compatible clock signal or a 14.31818-MHz crystal oscillator.
XTAL2	75	O	External clock reference output. Not connected if XTAL1 is driven by an external single-ended oscillator.
Digital Video			
C[9:0]/ GPIO[9:0]	57, 58, 59, 60, 63, 64, 65, 66, 69, 70	O	Digital video output of CbCr, C[9] is MSB and C[0] is LSB. Unused outputs can be left unconnected. Also, these terminals can be programmable general-purpose I/O. For the 8-bit mode, the two LSBs are ignored.
D_BLUE	58	I	Digital BLUE input from overlay device
D_GREEN	59	I	Digital GREEN input from overlay device
D_RED	60	I	Digital RED input from overlay device
FSO	57	I	Fast-switch overlay between digital RGB and any video
Y[9:0]	43, 44, 45, 46, 47, 50, 51, 52, 53, 54	O	Digital video output of Y/YCbCr, Y[9] is MSB and Y[0] is LSB. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected.
Miscellaneous Signals			
FSS/GPIO	35	I/O	Fast-switch (blanking) input. Switching signal between the synchronous component video (YPbPr/RGB) and the composite video input. Programmable general-purpose I/O
GLCO/I2CA	37	I/O	Genlock control output (GLCO). Two Genlock data formats are available: TI format and real time control (RTC) format. During reset, this terminal is an input used to program the I^2C address LSB.
INTREQ	30	O	Interrupt request
PWDN	33	I	Power down input: 1 = Power down 0 = Normal mode
RESETB	34	I	Reset input, active low

Table 1–1. Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NUMBER	I/O	DESCRIPTION
Host Interface			
SCL	28	I	I^2C clock input
SDA	29	I/O	I^2C data bus
Power Supplies			
AGND	26	I	Analog ground. Connect to analog ground.
A18GND_REF	13	I	Analog 1.8-V return
A18VDD_REF	12	I	Analog power for reference 1.8 V
CH1_A18GND CH2_A18GND CH3_A18GND CH4_A18GND	79 10 15 24	I	Analog 1.8-V return
CH1_A18VDD CH2_A18VDD CH3_A18VDD CH4_A18VDD	78 11 14 25	I	Analog power. Connect to 1.8 V.
CH1_A33GND CH2_A33GND CH3_A33GND CH4_A33GND	3 6 19 22	I	Analog 3.3-V return
CH1_A33VDD CH2_A33VDD CH3_A33VDD CH4_A33VDD	4 5 20 21	I	Analog power. Connect to 3.3 V.
DGND	27, 32, 42, 56, 68	I	Digital return
DVDD	31, 41, 55, 67	I	Digital power. Connect to 1.8 V.
IOGND	39, 49, 62	I	Digital power return
IOVDD	38, 48, 61	I	Digital power. Connect to 3.3 V or less for reduced noise.
PLL_A18GND	77	I	Analog power return
PLL_A18VDD	76	I	Analog power. Connect to 1.8 V.
Sync Signals			
HS/CS/GPIO	72	I/O	Horizontal sync output or digital composite sync output Programmable general-purpose I/O
VS/VBLK/GPIO	73	I/O	Vertical sync output (for modes with dedicated VSYNC) or VBLK output Programmable general-purpose I/O
FID/GPIO	71	I/O	Odd/even field indicator output. This terminal needs a pulldown resistor. Programmable general-purpose I/O
AVID/GPIO	36	I/O	Active video indicator output Programmable general-purpose I/O

2. TYPICAL CONNECTION DIAGRAM

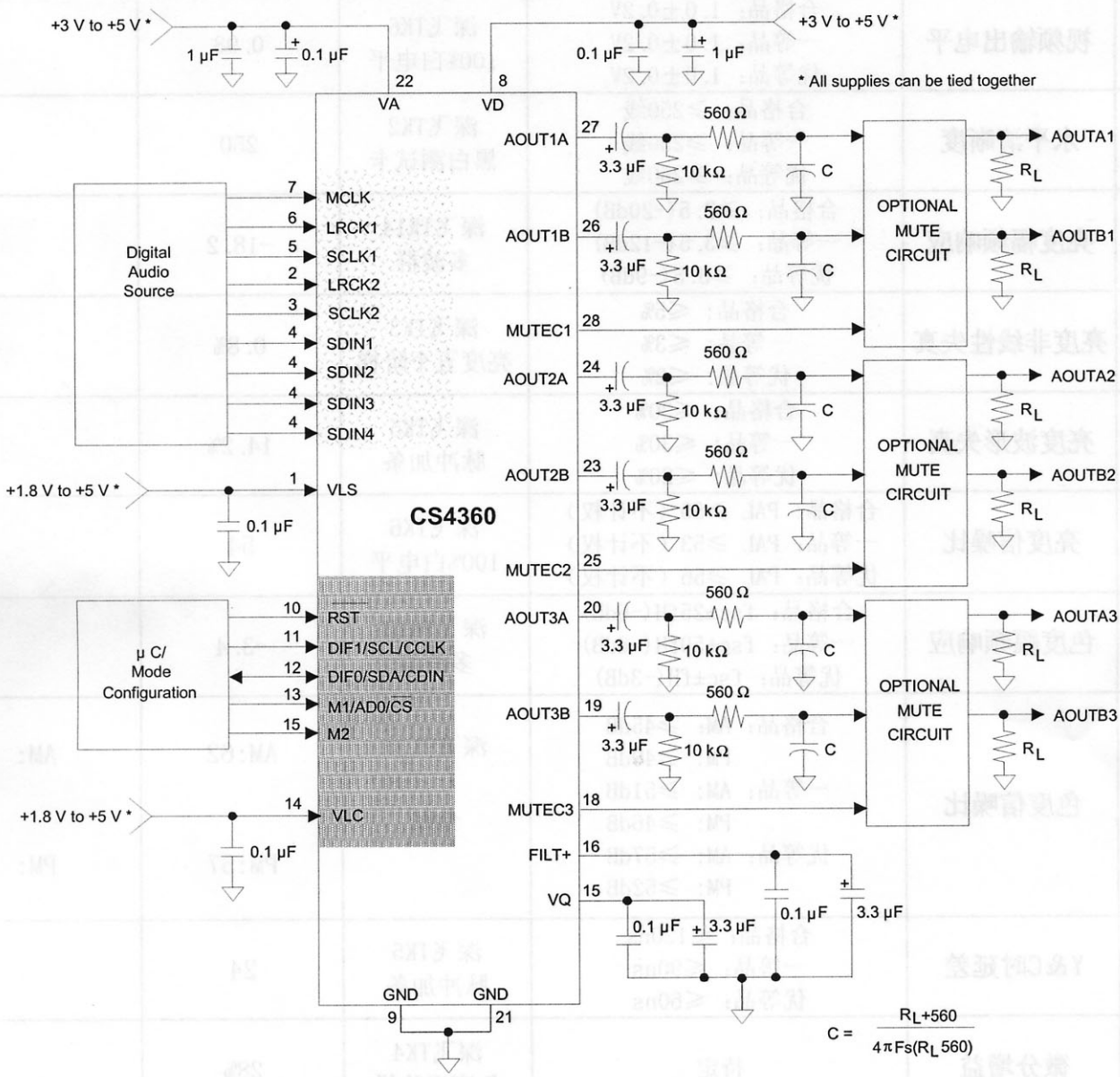
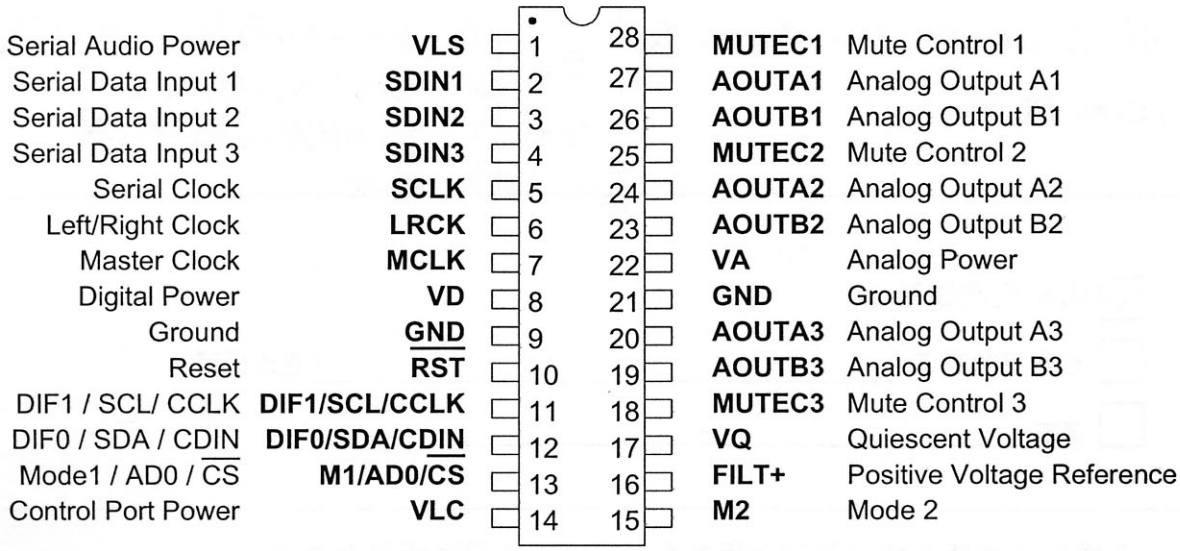


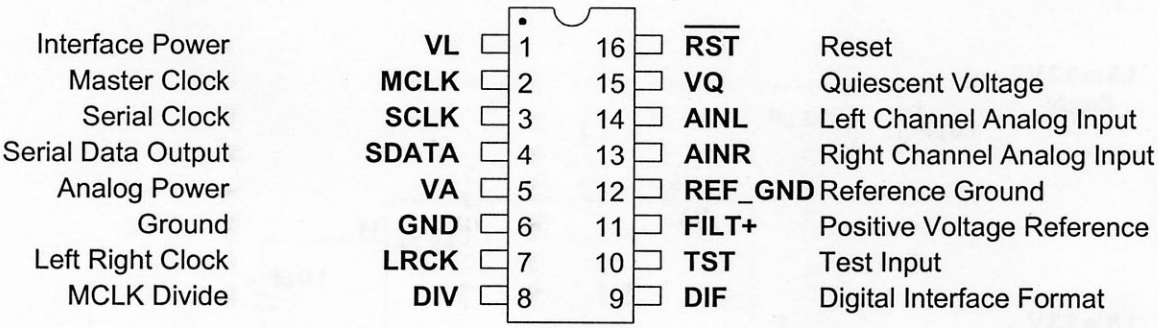
Figure 4. Typical Connection Diagram

5. PIN DESCRIPTION



Pin Name	#	Pin Description
VLS	1	**Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages. Applies to pins 2-7.
SDIN1 SDIN2 SDIN3	2 3 4	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. SDIN1 corresponds to AOUT1x, SDIN2 corresponds to AOUT2x and SDIN3 corresponds to AOUT3x.
SCLK	5	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	6	**Left / Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
MCLK	7	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 6 illustrates several standard audio sample rates and the required master clock frequency.
VD	8	**Digital Power** (*Input*) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	9 21	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
$\overline{\text{RST}}$	10	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low. The control port cannot be accessed when Reset is low.
VLC	14	**Control Port Interface Power** (*Input*) - Determines the required signal level for the control port and provides power for bidirectional control port pins. Refer to the Recommended Operating Conditions for appropriate voltages. Applies to pins 10-13 and 15.
FILT+	16	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to GND as shown in the Typical Connection Diagram.

3. PIN DESCRIPTION



Interface Power	1	**VL** (*Input*) - Digital interface power supply. Typically 1.8 to 3.3 VDC.
Master Clock	2	**MCLK** (*Input*) - The master clock frequency must be either 256x, 384x, 512x, 768x or 1024x the input sample rate in Base Rate Mode (BRM) and 128x, 192x, 256x, 384x the input sample rate in High Rate Mode (HRM). Table 1 illustrates several standard audio sample rates and the required master clock frequencies.
Serial Clock	3	**SCLK** (*Input/Output*) - Clocks the individual bits of the serial data out of the SDOUT pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF pin.
Serial Audio Data Out (M/S select)	4	**SDATA** (*Output*) - This pin serves two functions. First: two's complement MSB-first serial data is output on this pin. The data is clocked out of SDOUT via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF pin. Second: Master/Slave mode selection is determined, at startup, by a 47 kOhm pullup/pull-down on this line. A pullup to VL selects Master mode and a pulldown to GND selects Slave mode.
Analog Power	5	**VA** (*Input*) - Analog power supply. Typically 1.8 to 3.3 VDC.
Ground	6	**GND** (*Input*) - Ground Reference.

Sample Rate (kHz)	MCLK (MHz)								
	HRM				BRM				
	128x	192x	256x*	384x*	256x	384x	512x	768x*	1024x*
32	4.0960	6.1440	8.1920	12.2880	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	5.6448	8.4672	11.2896	16.9344	11.2896	16.9344	22.5792	32.7680	45.1584
48	6.1440	9.2160	12.2880	18.4320	12.2880	18.4320	24.5760	36.8640	49.1520
64	8.1920	12.2880	16.3840	24.5760	-	-	-	-	-
88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	-	-
96	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-

** DIV= Hi*

Table 1. Common Clock Frequencies

2. TYPICAL CONNECTION DIAGRAM

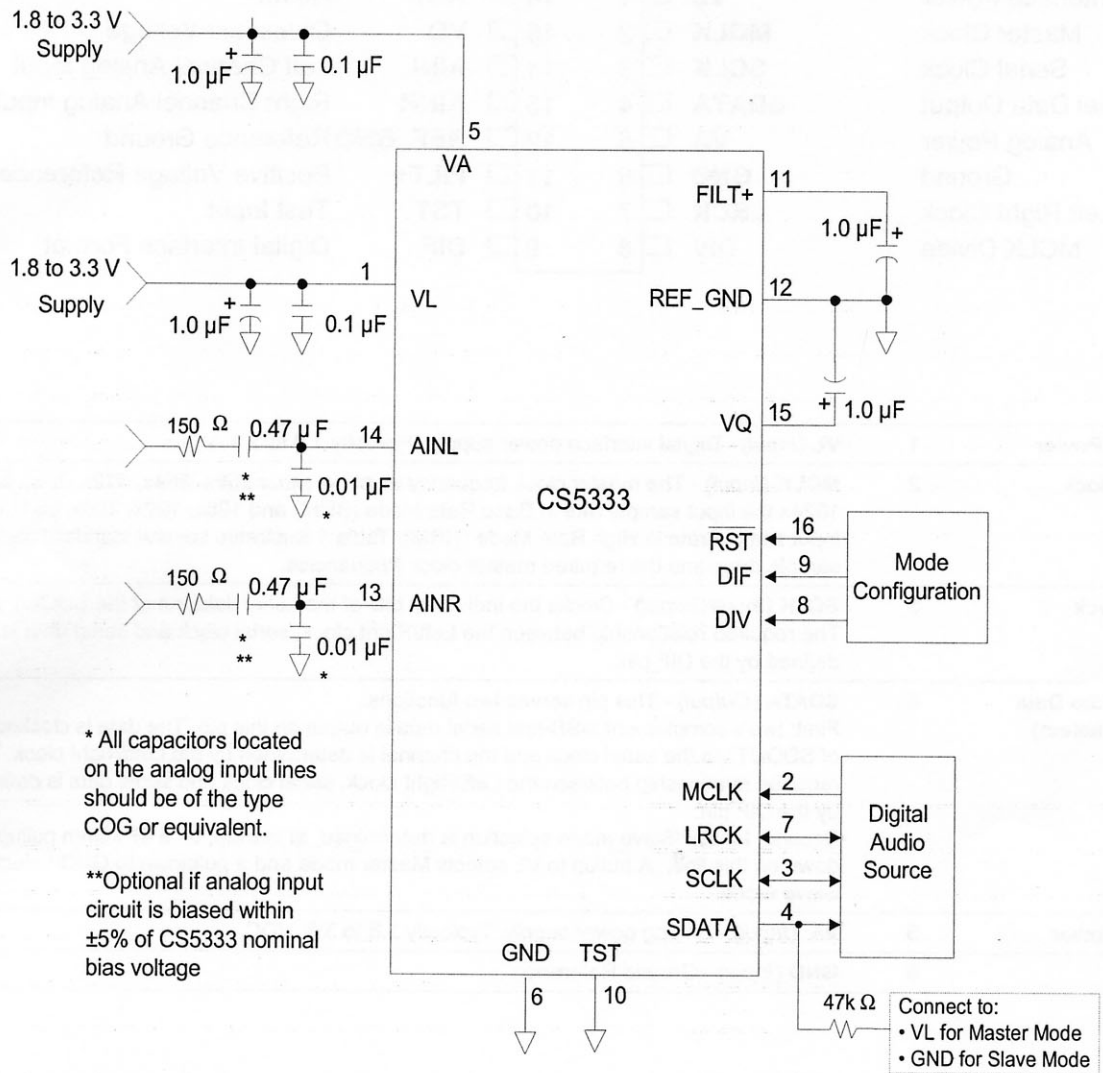


Figure 3. Typical Connection Diagram

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

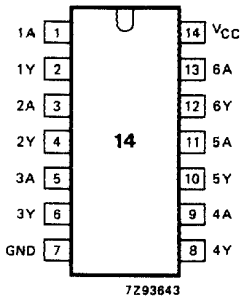


Fig.1 Pin configuration.

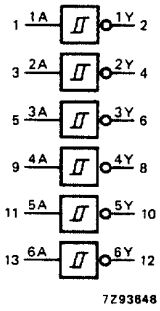


Fig.2 Logic symbol.

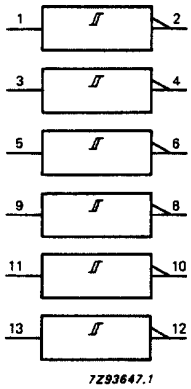


Fig.3 IEC logic symbol.

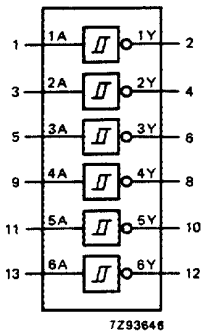


Fig.4 Functional diagram.

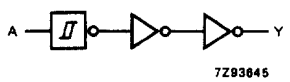


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

Notes

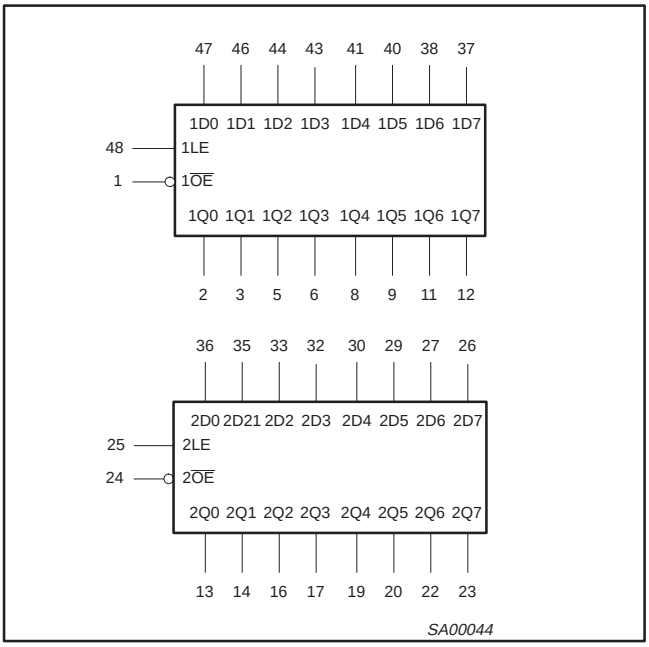
1. H = HIGH voltage level
   L = LOW voltage level

APPLICATIONS

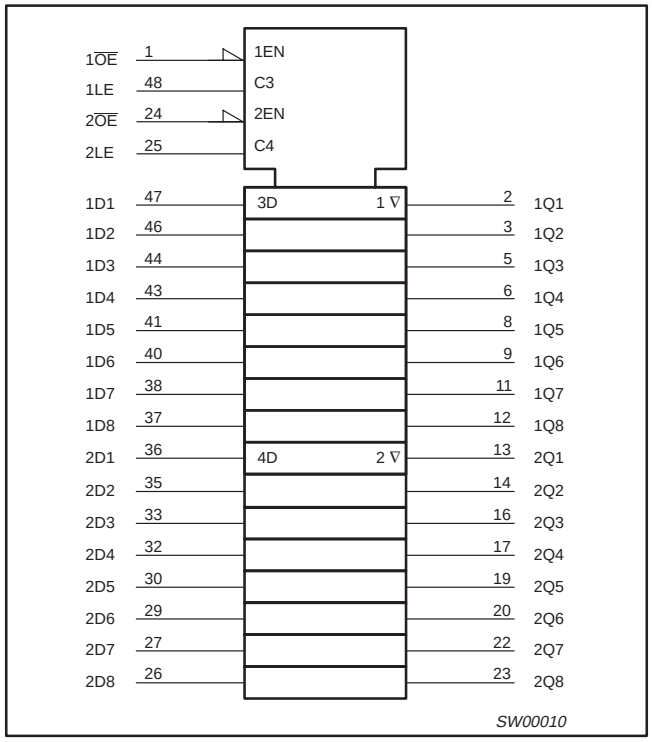
- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

2.5V/3.3V 16-bit transparent D-type latch (3-State) 74ALVT16373

LOGIC SYMBOL



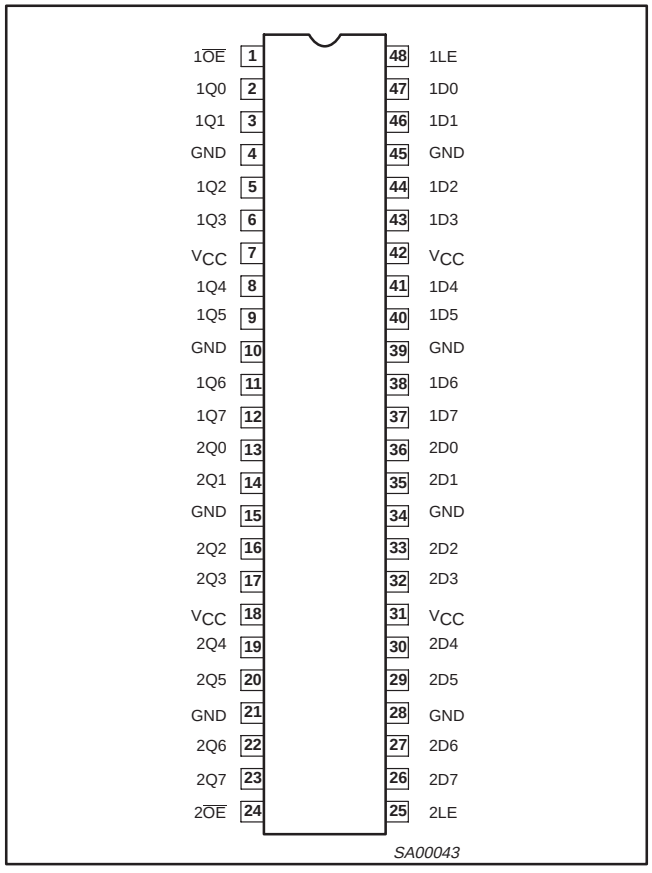
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1LE, 2LE	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

PIN CONFIGURATION



I²C BUS Control 5-Input 2-Output AV Switch
Monolithic IC MM1313

Outline

This IC is a 5-input 2-output AV switch with I²C control, developed for use in televisions. Two outputs enable it to support two screens or "picture-in-picture".

Features

1. Serial control by I²C bus.
2. 5-inputs, 2-outputs.
3. Video and audio system switches can be controlled independently.
4. 6dB amplifier built in to video system.
5. Built-in Y/C MIX circuit.
6. Slave address can be changed : 90H or 92H.
7. Audio muting possible by external pin.
8. Maintains high impedance even when I²C BUS line (SDA, SCL) power supply is off.
9. Built-in 3 value discrimination function.
10. On-chip power ON reset function.
11. Two types of audio input impedance : 60kΩ and 30kΩ.
    MM1313AD : 60kΩ MM1313BD : 30kΩ
12. Supports 2-screen or P-IN-P TV.

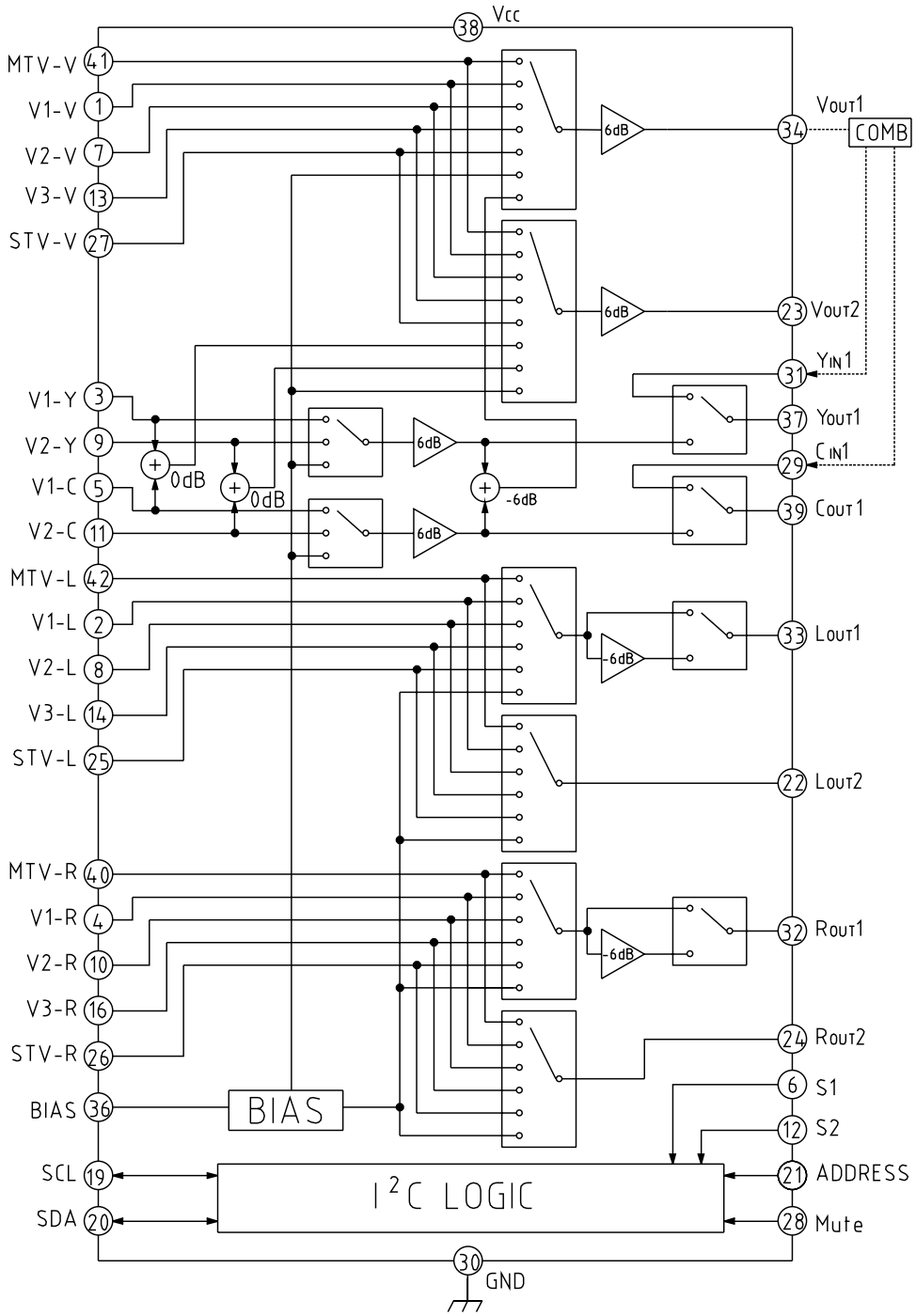
Package

SDIP-42A (MM1313AD, MM1313BD)

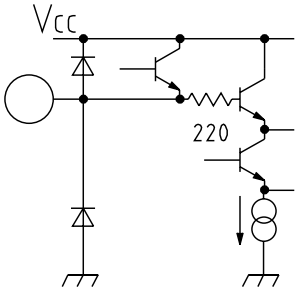
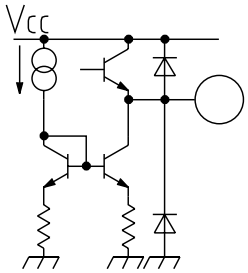
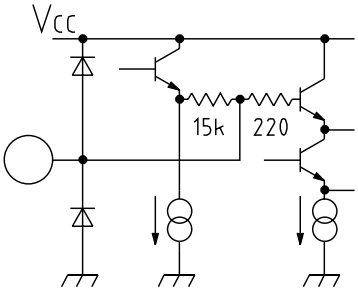
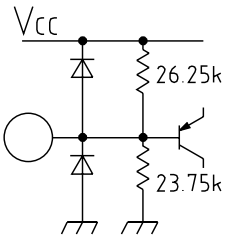
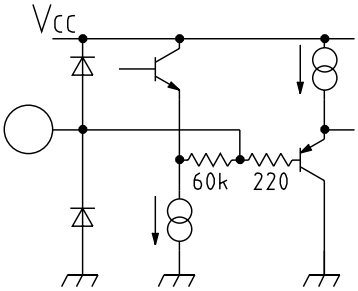
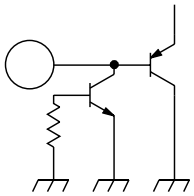
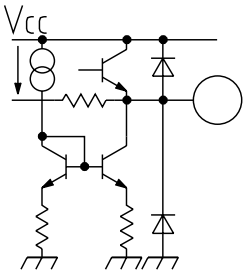
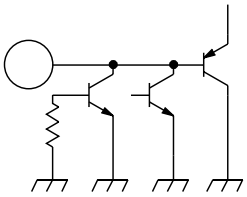
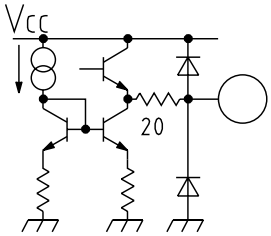
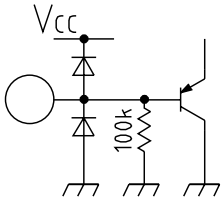
Applications

1. Televisions
2. Other video equipment

Equivalent Block Diagram



Pin Function

Pin No.	Name	Internal equivalent circuit diagram	Pin No.	Name	Internal equivalent circuit diagram
41 1 7 13 27 3 9 31	MTV–V V1–V V2–V V3–V STV–V V1–Y V2–Y YIN1		33 22 32 24	LOUT1 LOUT2 ROUT1 ROUT2	
5 11 29	V1–C V2–C CIN1		36	BIAS	
42 2 8 14 25 40 4 10 16 26	MTV–L V1–L V2–L V3–L STV–L MTV–R V1–R V2–R V3–R STV–R		19	SCL	
34 23	VOUT1 VOUT2		20	SDA	
37 39	YOUT1 COUT1		6 12 21 28	S1 S2 ADR Mute	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−40~+125	°C
Operating temperature	T_{OPR}	−20~+75	°C
Power supply voltage	V_{CC}	12	V
Allowable power dissipation	Pd	850	mW

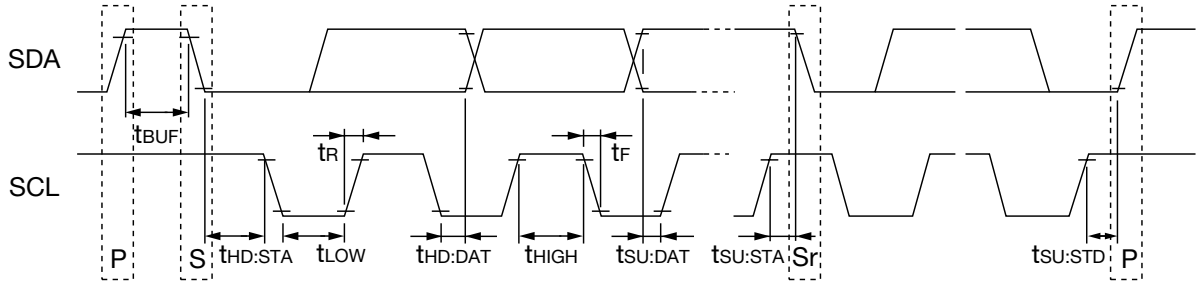
Electrical Characteristics (Ta=25°C, V_{CC}=9V)

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}			8	9	10	V
Current consumption	I_{CC}	38	V_{CC}=9V, no signal, no load		40	52	mA
V_{OUT}1 output							
Voltage gain	G_{V}1	TP1	Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_{V}1	TP1	Sine wave 1.0V_{P-P}, 10MHz/100kHz	−1.0	0	1.0	dB
Differential gain	DG_{V}1	TP1	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	%
Differential phase	DP_{V}1	TP1	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	deg
Input dynamic range	D_{V}1	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
V_{OUT}2 output							
Voltage gain	G_{V}2	TP6	Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_{V}2	TP6	Sine wave 1.0V_{P-P} 10MHz/100kHz	−1.0	0	1.0	dB
Differential gain	DG_{V}2	TP6	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	%
Differential phase	DP_{V}2	TP6	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	deg
Input dynamic range	D_{V}2	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
Y_{OUT}1 output							
Voltage gain	G_{Y}1	TP2	Vn-Y : Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_{Y}2	TP2	Y_{IN}1 : Sine wave 2.0V_{P-P}, 100kHz	−0.5	0	0.5	
Frequency characteristics	F_{Y}1	TP2	Vn−Y : Sine wave 1.0V_{P-P} 10MHz/100kHz	−1.0	0	1.0	dB
	F_{Y}2	TP2	Y_{IN}1 : Staircase 2.0V_{P-P} 10MHz/100kHz	−1.0	0	1.0	
Differential gain	DG_{Y}	TP2	Vn-Y : Staircase 1V_{P-P} APL=10~90% Y_{IN}1: Staircase 2V_{P-P} APL=10~90%	−3	0	3	%
Differential phase	DP_{Y}	TP2	Vn-Y : Staircase 1V_{P-P} APL=10~90% Y_{IN}1 : Staircase 2V_{P-P} APL=10~90%	−3	0	3	deg

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Input dynamic range	D_{Y1}	SG2	Vn-Y : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
	D_{Y2}	SG4	V_{IN1} : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	3.2	3.8		
Output impedance	Z_{OYC1}				50		Ω
C_{OUT1} output							
Voltage gain	G_{C1}	TP3	Vn-C : Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_{C2}	TP3	C_{IN1} : Sine wave 2.0V_{P-P}, 100kHz	–0.5	0	0.5	
Frequency characteristics	F_{C1}	TP3	Vn–C : Sine wave 1.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	dB
	F_{C2}	TP3	C_{IN1} : Sine wave 2.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	
Differential gain	DG_C	TP3	C_{IN1} : Staircase 2V_{P-P} APL=10~90%	–3	0	3	%
Differential phase	DP_C	TP3	C_{IN1} : Staircase 2V_{P-P} APL=10~90%	–3	0	3	deg
Input dynamic range	D_{C1}	SG3	Vn-C : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	2.75	3.25		V_{P-P}
	D_{C2}	SG5	C_{IN1}: Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	5.5	6.5		
Input impedance	Z_{IC}		Vn–C, C_{IN1}	10	15	20	kΩ
Output impedance	Z_{OC1}				50		Ω
L_{OUT1} output							
Voltage gain	G_{L11}	TP4	b7=0, Sine wave 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_{L12}	TP4	b7=1, Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	
Frequency characteristics	F_{L1}	TP4	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_{L1}	TP4	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_{L1}	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFL1}	33	L_{OUT1} pin DC difference during SW switching		0	±15	mV
Input impedance	Z_{IL1}			42	60	78	kΩ
Output impedance	Z_{OL1}				120		Ω
L_{OUT2} output							
Voltage gain	G_{L2}	TP7	Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	dB
Frequency characteristics	F_{L2}	TP7	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_{L2}	TP7	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_{L2}	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFL2}	22	L_{OUT2} pin DC difference during SW switching		0	±15	mV
Output impedance	Z_{OL2}				120		Ω
R_{OUT1} output							
Voltage gain	G_{R11}	TP5	b7=0, Sine wave 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_{R12}	TP5	b7=1, Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	
Frequency characteristics	F_{R1}	TP5	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_{R1}	TP5	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_{R1}	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFR1}	32	R_{OUT1} pin DC difference during SW switching		0	±15	mV
Input impedance	Z_{IR1}			42	60	78	kΩ
Output impedance	Z_{OR1}				120		Ω

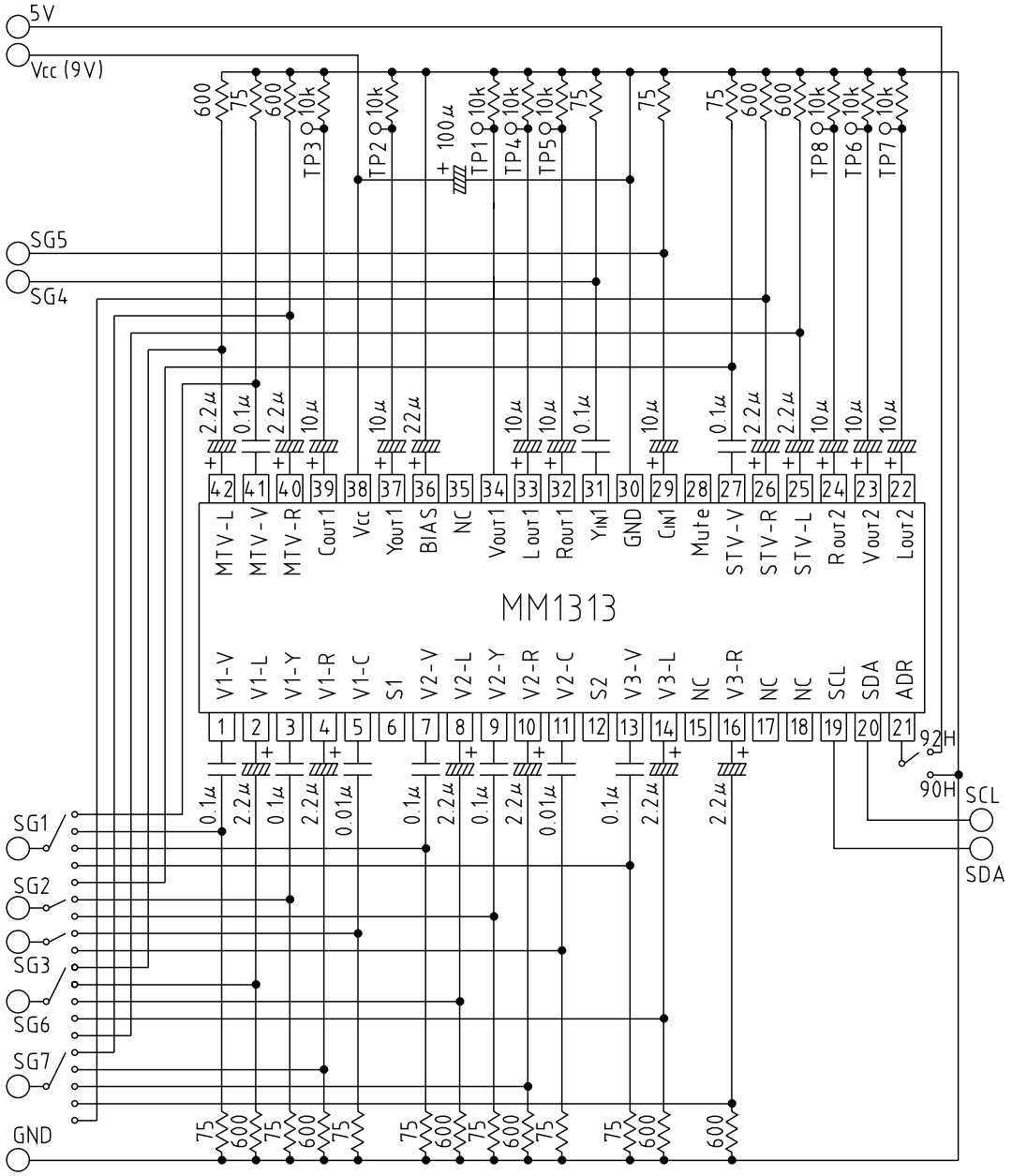
Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
ROUT2 output							
Voltage gain	GR2	TP8	Sine wave 2.5VP-P, 1kHz	–0.5	0.0	0.5	dB
Frequency characteristics	FR2	TP8	Sine wave 2.5VP-P, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THDR2	TP8	Sine wave 2.5VP-P, 1kHz		0.03	0.1	%
Input dynamic range	DR2	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	VOFFR2	24	ROUT2 pin DC difference during switching		0	±15	mV
Output impedance	ZOR2				120		Ω
Crosswalk							
VOUT 1	CTV1	TP1	Measurement Circuit Figure 2 for SG1 input : 4.43MHz, 1VP-P for SG2 input : 4.43MHz, 0.5VP-P		–60	–53	dB
VOUT 2	CTV2	TP2			–60	–53	dB
YOUT 1	CTY1	TP3			–60	–53	dB
COUT 1	CTC1	TP6			–60	–53	dB
LOUT 1	CTL1	TP4	Measurement Circuit Figure 2 1kHz, 2.5VP-P		–90	–80	dB
LOUT 2	CTL2	TP5			–90	–80	dB
ROUT 1	CTR1	TP7			–90	–80	dB
ROUT 2	CTR2	TP8			–90	–80	dB
Video I/O Pin Voltage							
Input pin voltage	VVIP		No signal, no load	4.6	4.9	5.2	V
Output pin voltage	VVOP		VOUT1 pin, VOUT2 pin No signal, no load	4.1	4.4	4.7	V
	VSOP		YOUT1 pin, COUT1 pin No signal, no load	3.3	3.6	3.9	V
Audio I/O Pin Voltage							
Input pin voltage	VAIP		No signal, no load	4.0	4.3	4.6	V
Output pin voltage	VAOP		No signal, no load	3.9	4.2	4.5	V
Logic section (Refer to figure below)							
Input voltage L	VIL		I²C logic low level discrimination value	0.0		1.5	V
Input voltage H	VIH		I²Clogic high level discrimination value	3.0		5.0	V
Low level output voltage (SDA)	VOL		SDA for 3mA inflow	0.0		0.4	V
High level input current	IIH		when SDA, SCL=4.5V impressed	–10		+10	µA
Low level input current	IIL		when SDA, SCL=0.4V impressed	–10		+10	µA
Clock frequency	fSCL					100	kHz
Data transmission waiting time	tBUF			4.7			µS
SCL start hold time	tHD;STA			4.0			µS
SCL low level hold time	tLOW			4.7			µS
SCL high level hold time	tHIGH			4.0			µS
SCL start set-up time	tSU;STA			4.7			µS
SDA data hold time	tHD;DAT			200			nS
SDA data set-up time	tSD;DAT			250			nS
SCL rise time	tR					1000	nS
SCL fall time	tF					300	nS
SCL stop set-up time	tSU;STO			4.0			µS

I²C BUS BUS Control Signal

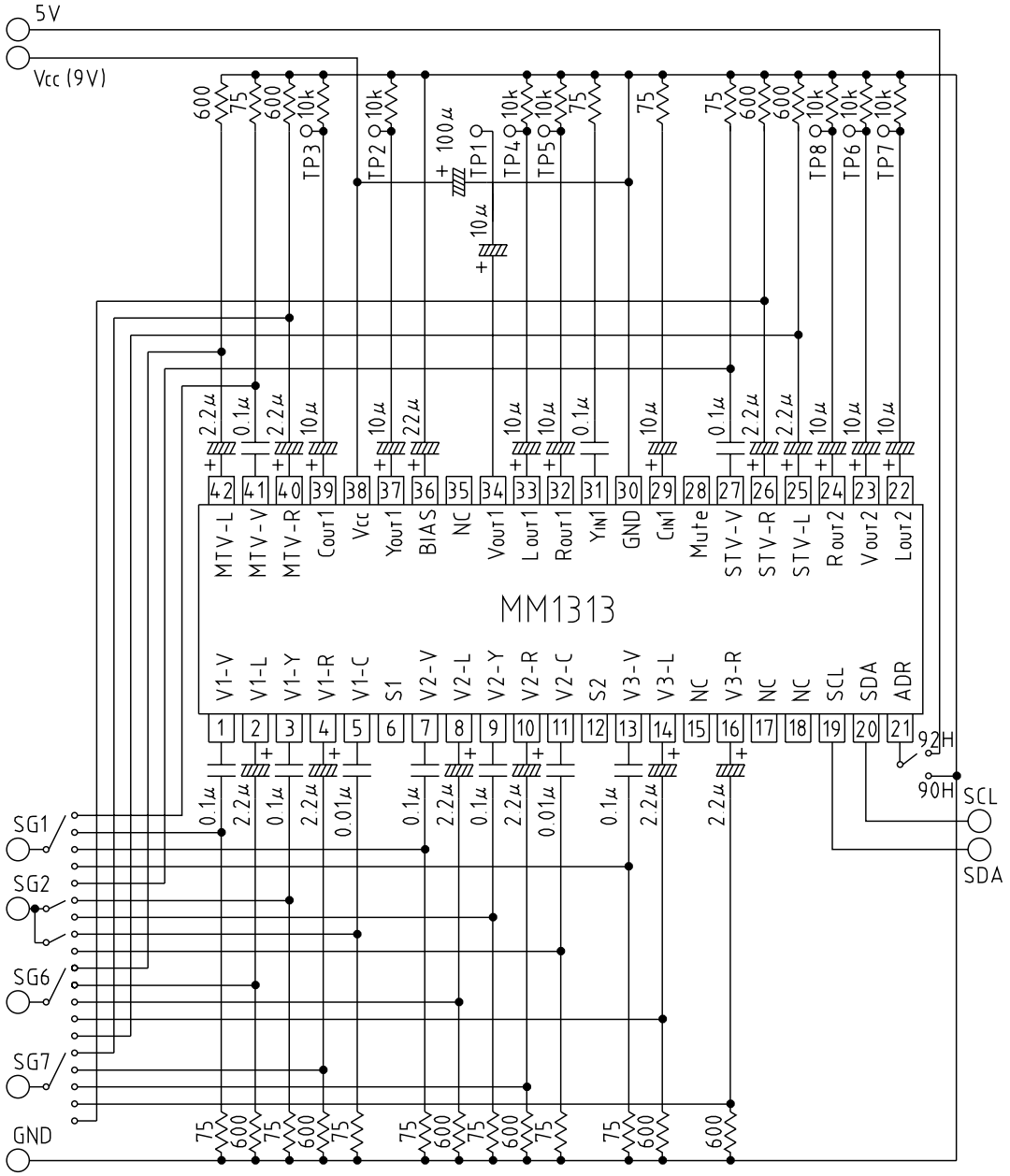


Measurement Circuit

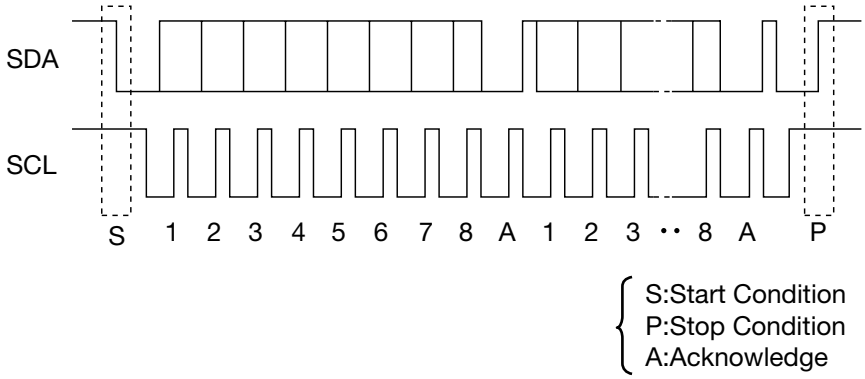
Measurement Circuit 1



Measurement Circuit 2 (Crosstalk measurement)



I²C BUS



The I²C BUS is a BUS system developed by Philips for internal use in equipment. Data transmission is carried out by the two SDA and SCL lines, in byte units, with the MSB first from start condition.

[Control Register]

The control register contains data sent from the master in order to determine the status of each switch.

S	Slave address							R/W	A	Control register 1								A	Control register 2								A	P
	1	0	0	1	0	0	0/1	0		b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Control data																		

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 0 when using as a control register.

The MM1313 slave address can be selected as 90H/92H depending on the status of the ADR pin. When ADR pin is low it is 90H.

The relationship between the control register bits and switch control is as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
Audio Gain	S/Comp Select	Video–Select			Audio–Select		

The control register bits are reset to 0 when power is applied.

MM1313 control is carried out by the 3-byte structure of the 1 address byte and 2 control data bytes. The first byte in the control data is control data for output 1, and the remaining 1 byte is control data for output 2.

All of the remaining data (fourth byte and after) are ignored.

Refer to the separate tables for details on switch control.

[Status Register]

The status register contains data for sending device status to the master.

S	Slave address							R/W	A	Status register								NA	P
	1	0	0	1	0	0	0/1	1		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Status data									

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 1 when using as a status register.

The MM1313 slave address can be selected as 91H/93H depending on the status of the ADR pin. When the ADR pin is low it is 91H. However, the confirmation response after completion of the status register should be non-acknowledge.

The status register output data as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

P-ON RESET : Returns 1 for power on reset. However once data read begins, 0 is returned next.
S1/S2 OPEN : Returns 0 when the S1/S2 pin is not open, and returns 1 when the S1/S2 pin is open
S1/S2 SEL : Returns 0 when the S1/S2 pin is not grounded, and returns 1 when the S1/S2 pin is grounded.

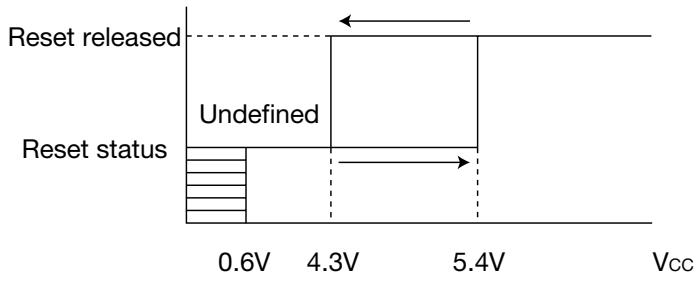
S1/S2 OPEN, SEL have 3-value discrimination, and the combinations are as shown below.

S1/S2 pin DC voltage	S1/S2 OPEN	S1/S2 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

[Power On Reset]

Power on reset is built in to reset each control register to 0 when power is turned on.

Power on reset threshold has hysteresis as shown in the figure below. The IC power on reset status can be discriminated by reading the status register P-ON RESET.



Switch Control Table

1. Video Output 1

b6	b5	b4	b3	VOUT1	YOUT1	COUT1
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV–V	YIN1	CIN1
0	0	1	0	V1–V	YIN1	CIN1
0	0	1	1	V2–V	YIN1	CIN1
0	1	0	0	V3–V	YIN1	CIN1
0	1	0	1	STV–V	YIN1	CIN1
0	1	1	0	Mute	Mute	Mute
		1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV–V	YIN1	CIN1
1	0	1	0	V1–Y+C	V1–Y	V1–C
1	0	1	1	V2–Y+C	V2–Y	V2–C
1	1	0	0	V3–V	YIN1	CIN1
1	1	0	1	STV–V	YIN1	CIN1
1	1	1	0	Mute	Mute	Mute
		1	1			

2. Video Output 2

b6	b5	b4	b3	VOUT2
0	0	0	0	Mute
0	0	0	1	MTV–V
0	0	1	0	V1–V
0	0	1	1	V2–V
0	1	0	0	V3–V
0	1	0	1	STV–V
0	1	1	0	Mute
		1	1	
1	0	0	0	Mute
1	0	0	1	MTV–V
1	0	1	0	V1–Y+C
1	0	1	1	V2–Y+C
1	1	0	0	V3–V
1	1	0	1	STV–V
1	1	1	0	Mute
		1	1	

3. Audio Output 1

Mute pin	b2	b1	b0	LOUT1	ROUT1
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
		1	1		
3.0V or more	–	–	–	Mute	Mute

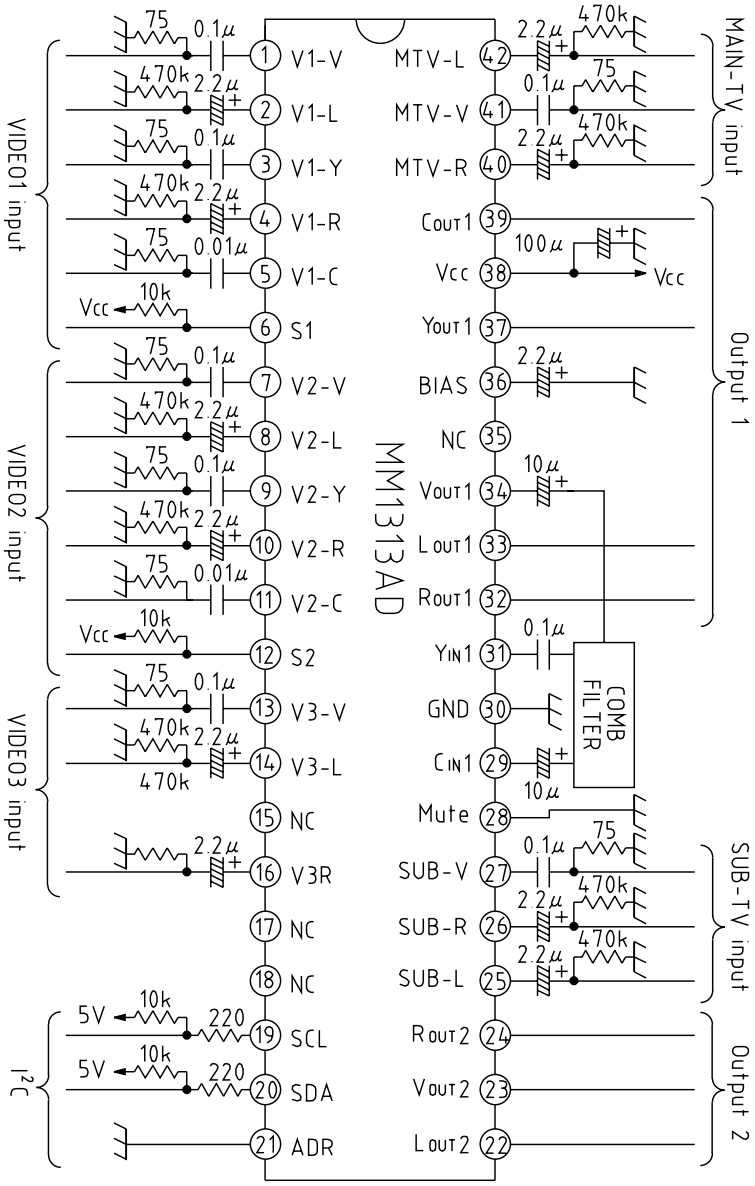
4. Audio Output 1 Gain Switching

b7	Output gain
0	–6dB output
1	0dB output

5. Audio Output 2

Mute pin	b2	b1	b0	LOUT2	ROUT2
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
		1	1		
3.0V or more	–	–	–	Mute	Mute

Application Circuit



Notes

1. VOUT is set at 4.4V and CIN at 4.9V
   Please note that capacitance polarity may vary depending on comb filter bias.
2. Each audio output can be muted by making pin 19 high. Mute is off when it is open or low.

19-0463; Rev 0; 1/96

MAXIM

Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4051/MAX4052/MAX4053 and MAX4051A/MAX4052A/MAX4053A are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4051/A), two 4-channel multiplexers (MAX4052/A), and three single-pole/double-throw (SPDT) switches (MAX4053/A). The A-suffix parts are fully characterized for on-resistance match, on-resistance flatness, and low leakage.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each switch can handle rail-to-rail analog signals. The off leakage current is only 0.1nA at +25°C or 5nA at +85°C (MAX4051A/MAX4052A/4053A).

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

Features

- ♦ **Pin Compatible with Industry-Standard 74HC4051/74HC4052/74HC4053**
- ♦ **Guaranteed On-Resistance: 100Ω with ±5V Supplies**
- ♦ **Guaranteed Match Between Channels: 6Ω (MAX4051A–MAX4053A) 12Ω (MAX4051–MAX4053)**
- ♦ **Guaranteed Low Off Leakage Currents: 0.1nA at +25°C (MAX4051A–MAX4053A) 1nA at +25°C (MAX4051–MAX4053)**
- ♦ **Guaranteed Low On Leakage Currents: 0.1nA at +25°C (MAX4051A–MAX4053A) 1nA at +25°C (MAX4051–MAX4053)**
- ♦ **Single-Supply Operation from +2.0V to +16V Dual-Supply Operation from ±2.7V to ±8V**
- ♦ **TTL/CMOS-Logic Compatible**
- ♦ **Low Distortion: < 0.04% (600Ω)**
- ♦ **Low Crosstalk: < -90dB (50Ω)**
- ♦ **High Off Isolation: < -90dB (50Ω)**

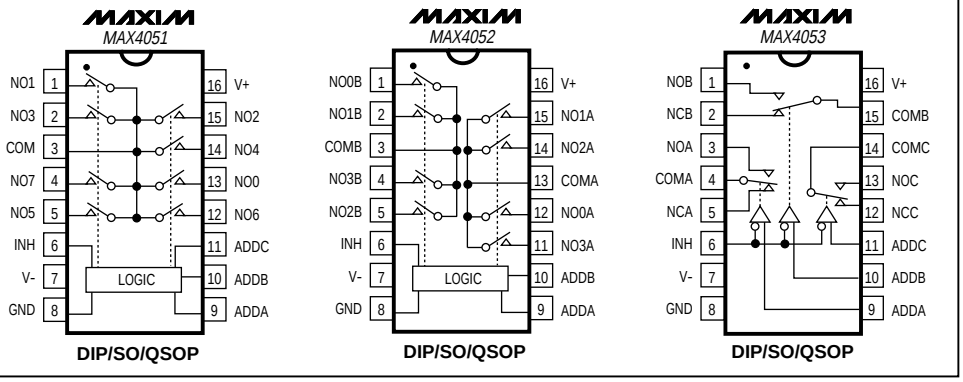
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4051ACPE	0°C to +70°C	16 Plastic DIP
MAX4051ACSE	0°C to +70°C	16 Narrow SO
MAX4051ACEE	0°C to +70°C	16 QSOP

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams

TOP VIEW



DIP/SO/QSOP **DIP/SO/QSOP** **DIP/SO/QSOP**

Low-Voltage, CMOS Analog Multiplexers/Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +17V
V-.....+0.3V to -17V
V+ to V-.....-0.3V to +17V
Voltage into Any Terminal (Note 1) .....(V- - 2V) to (V+ + 2V)
or 30mA (whichever occurs first)
Continuous Current into Any Terminal.....±30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle) .....±100mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C).....842mW
Narrow SO (derate 8.70mW/°C above +70°C).....696mW
QSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX405_C_ E/MAX405_AC_E .....0°C to +70°C
MAX405_E_ E/MAX405_AE_E.....-40°C to +85°C
MAX405_MJE/MAX405_AMJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V		T_A = +25°C		60	100	Ω
				C, E, M			125	
COM–NO On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C			6	Ω
				C, E, M			12	
			MAX4051, MAX4052, MAX4053	T_A = +25°C			12	
				C, E, M			18	
COM–NO On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C			10	Ω
				C, E, M			15	
NO Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{NO} = 4.5V, V_{COM} = -4.5V	MAX4051, MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 5.5V, V- = -5.5V, V_{NO} = -4.5V, V_{COM} = 4.5V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-100		100	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
COM Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{NO} = 4.5V, V_{COM} = -4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-100		100	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V- = -5.5V, V_{NO} = -4.5V, V_{COM} = 4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-50		50	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM} = V_{NO} = \pm 4.5V$	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-50		50	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL I/O							
ADD, INH Input Logic Threshold High	V_{IH}		C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}		C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V	C, E, M	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		50	175	ns
			C, E, M			225	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		40	150	ns
			C, E, M			200	
Transition Time	t_{TRANS}	Figure 2	T_A = +25°C		75	250	ns
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C	2	10		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		2	10	pC
NO Off Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz, Figure 7	T_A = +25°C		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz, Figure 7	T_A = +25°C		2		pF
Switch On Capacitance	$C_{(ON)}$	V_{COM} = V_{NO} = GND, f = 1MHz, Figure 7	T_A = +25°C		8		pF
Off Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	±2.7		±8	V
V+ Supply Current	I+	INH = ADD = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M			10	
V- Supply Current	I-	INH = ADD = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M	-10			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	V+ = 5V, I_{NO} = 1mA, V_{COM} = 3.5V		T_A = +25°C		125	225	Ω
				C, E, M			280	
NO Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{NO} = 4.5V, V_{COM} = 0V		T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 5.5V, V_{NO} = 0V, V_{COM} = 4.5V		T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
COM Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{NO} = 4.5V, V_{COM} = 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V_{NO} = 0V, V_{COM} = 4.5V or 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = 4.5V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
DIGITAL I/O								
ADD, INH Input Logic Threshold High	V_{IH}			C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}			C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V		C, E, M	-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	INH = ADD = 0V or V+		T_A = +25°C	-1		1	µA
				C, E, M			10	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		90	200	ns
			C, E, M			275	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		60	125	ns
			C, E, M			175	
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C		30		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		2	10	pC
Off Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.
Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.
Note 6: Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	I_{NO} = 1mA, V+ = 3V, V_{COM} = 1.5V		T_A = +25°C		250	525	Ω
				C, E, M			700	
NO Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 3.6V, V_{NO} = 3V, V_{COM} = 0V		T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 3.6V, V_{NO} = 0V, V_{COM} = 3V		T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
COM Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{NO} = 3V, V_{COM} = 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 3.6V, V_{NO} = 0V, V_{COM} = 3V	MAX4051/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} = 3V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
DIGITAL I/O								
ADD, INH Input Logic Threshold High	V_{IH}			C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}			C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V		C, E, M	-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	INH = ADD = 0V or V+		T_A = +25°C	-1		1	µA
				C, E, M			10	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

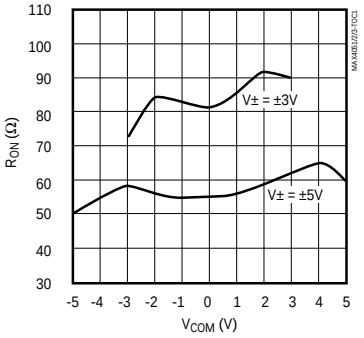
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		180	600	ns
			C, E, M			700	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		100	300	ns
			C, E, M			400	
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C		90		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		1	10	pC
Off Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.
Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.
Note 6: Guaranteed by design, not production tested.

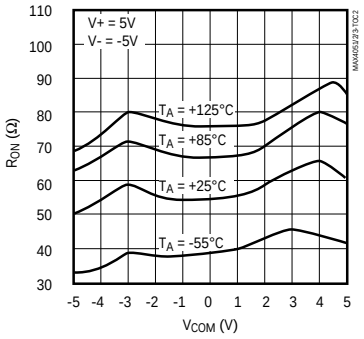
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

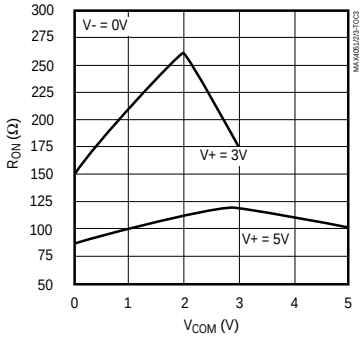
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



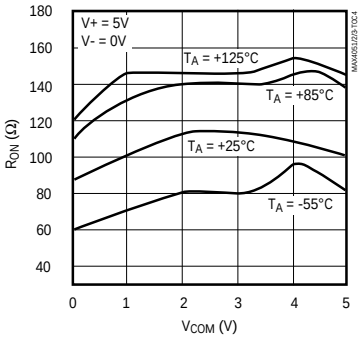
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



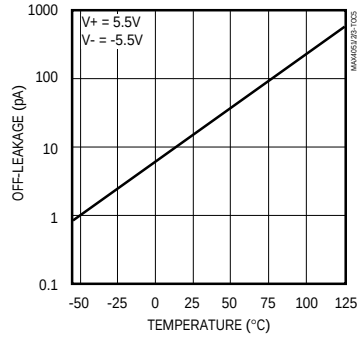
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



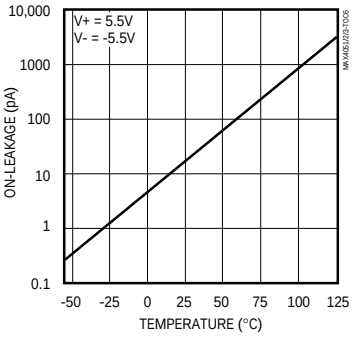
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



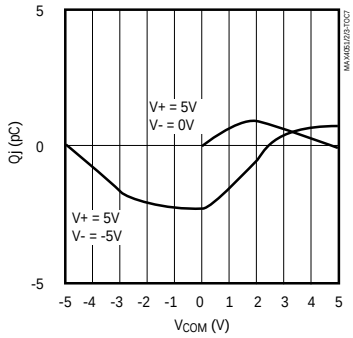
OFF-LEAKAGE vs. TEMPERATURE



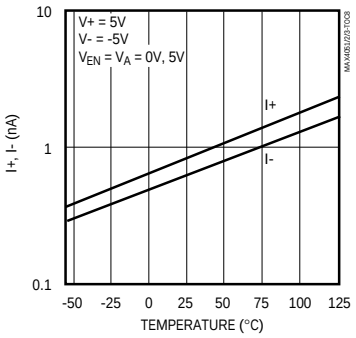
ON-LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE

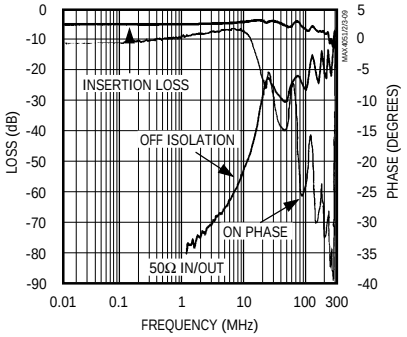


Low-Voltage, CMOS Analog Multiplexers/Switches

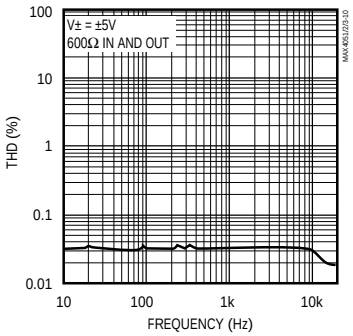
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Descriptions

PIN			NAME	FUNCTION
MAX4051/ MAX4051A	MAX4052/ MAX4052A	MAX4053/ MAX4053A		
13, 1, 15, 2, 14, 5, 12, 4	—	—	NO0–NO7	Analog Switch Inputs 0–7
3	—	—	COM	Analog Switch Common
—	1, 2, 5, 4	—	NO0B–NO3B	Analog Switch “B” Inputs 0–3
—	3	15	COMB	Analog Switch “B” Common
—	—	1	NOB	Analog Switch “B” Normally Open Input
—	—	2	NCB	Analog Switch “B” Normally Closed Input
—	—	3	NOA	Analog Switch “A” Normally Open Input
—	—	5	NCA	Analog Switch “A” Normally Closed Input
6	6	6	INH	Digital Inhibit Input. Normally connect to GND. Can be driven to logic high to set all switches off.
7	7	7	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
8	8	8	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
9	9	9	ADDA	Digital Address “A” Input
10	10	10	ADDB	Digital Address “B” Input
11	—	11	ADDC	Digital Address “C” Input
—	12, 15, 14, 11	—	NO0A–NO3A	Analog Switch “A” Inputs 0–3
—	13	4	COMA	Analog Switch “A” Common
—	—	12	NCC	Analog Switch “C” Normally Closed Input
—	—	13	NOC	Analog Switch “C” Normally Open Input
—	—	14	COMC	Analog Switch “C” Common
16	16	16	V+	Positive Analog and Digital Supply Voltage Input

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

Table 1. Truth Table/Switch Programming

INH	ADDRESS BITS			ON SWITCHES		
	ADDC*	ADDB	ADDA	MAX4051/ MAX4051A	MAX4052/ MAX4052A	MAX4053/ MAX4053A
1	X	X	X	All switches open	All switches open	All switches open
0	0	0	0	COM–NO0	COMB–NO0B, COMC–NO0C	COMA–NCA, COMB–NCB, COMC–NCC
0	0	0	1	COM–NO1	COMB–NO1B, COMC–NO1C	COMA–NOA, COMB–NCB, COMC–NCC
0	0	1	0	COM–NO2	COMB–NO2B, COMC–NO2C	COMA–NCA, COMB–NOB, COMC–NCC
0	0	1	1	COM–NO3	COMB–NO3B, COMC–NO3C	COMA–NOA, COMB–NOB, COMC–NCC
0	1	0	0	COM–NO4	COMB–NO0B, COMC–NO0C	COMA–NCA, COMB–NCB, COMC–NOC
0	1	0	1	COM–NO5	COMB–NO1B, COMC–NO1C	COMA–NOA, COMB–NCB, COMC–NOC
0	1	1	0	COM–NO6	COMB–NO2B, COMC–NO2C	COMA–NCA, COMB–NOB, COMC–NOC
0	1	1	1	COM–NO7	COMB–NO3B, COMC–NO3C	COMA–NOA, COMB–NOB, COMC–NOC

X = Don't care * ADDC not present on MAX4052.

Note: NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

Applications Information

Power-Supply Considerations

Overview

The MAX4051/MAX4052/MAX4053 and MAX4051A/MAX4052A/MAX4053A construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog signal path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and V- signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ and V- have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V+ is +5V. As V+ rises, the threshold increases slightly, so when V+ reaches +12V, the threshold is about 3.1V; above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

These devices operate with bipolar supplies between ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of +17V.

Single Supply

These devices operate from a single supply between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually "work" with a single supply at near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs (NO) and by COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 17V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

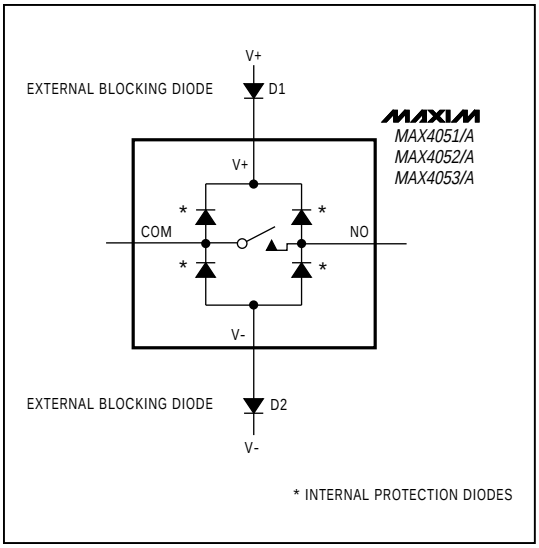
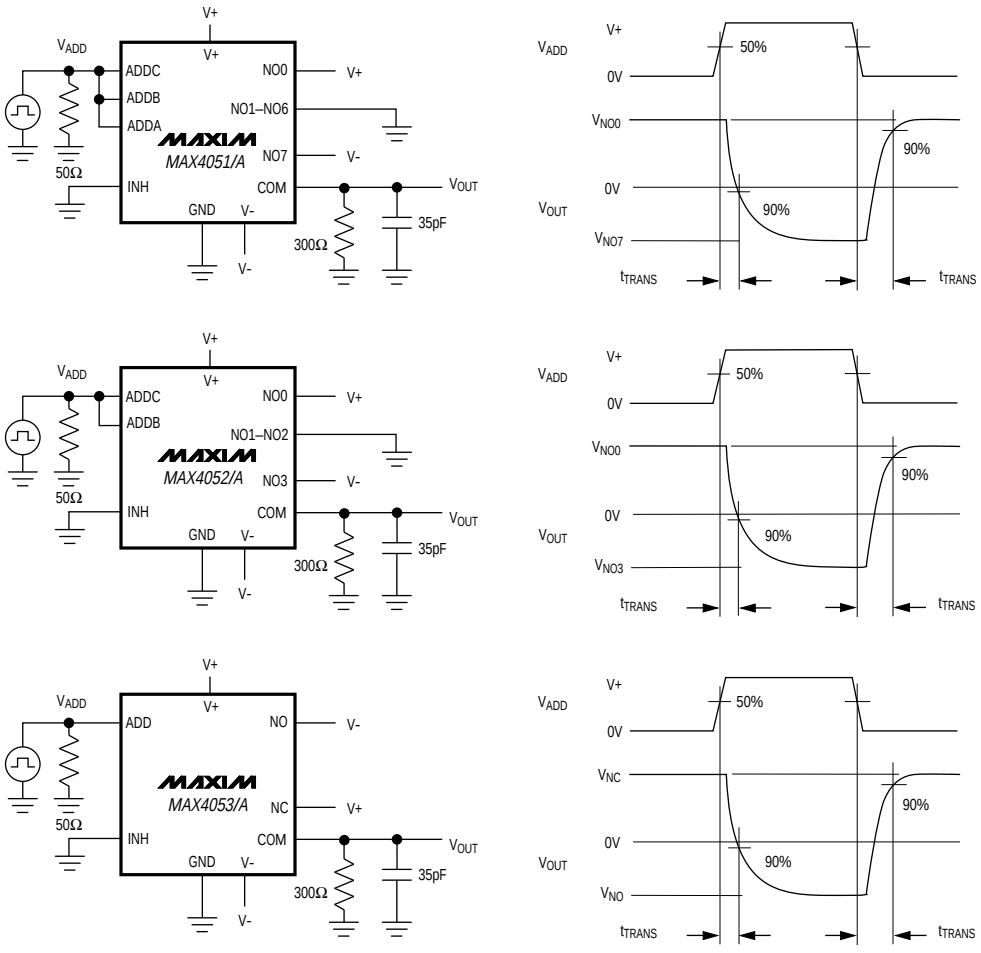


Figure 1. Overvoltage Protection Using External Blocking Diodes

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor, and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is entirely due to capacitive coupling.



V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 2. Address Transition Time

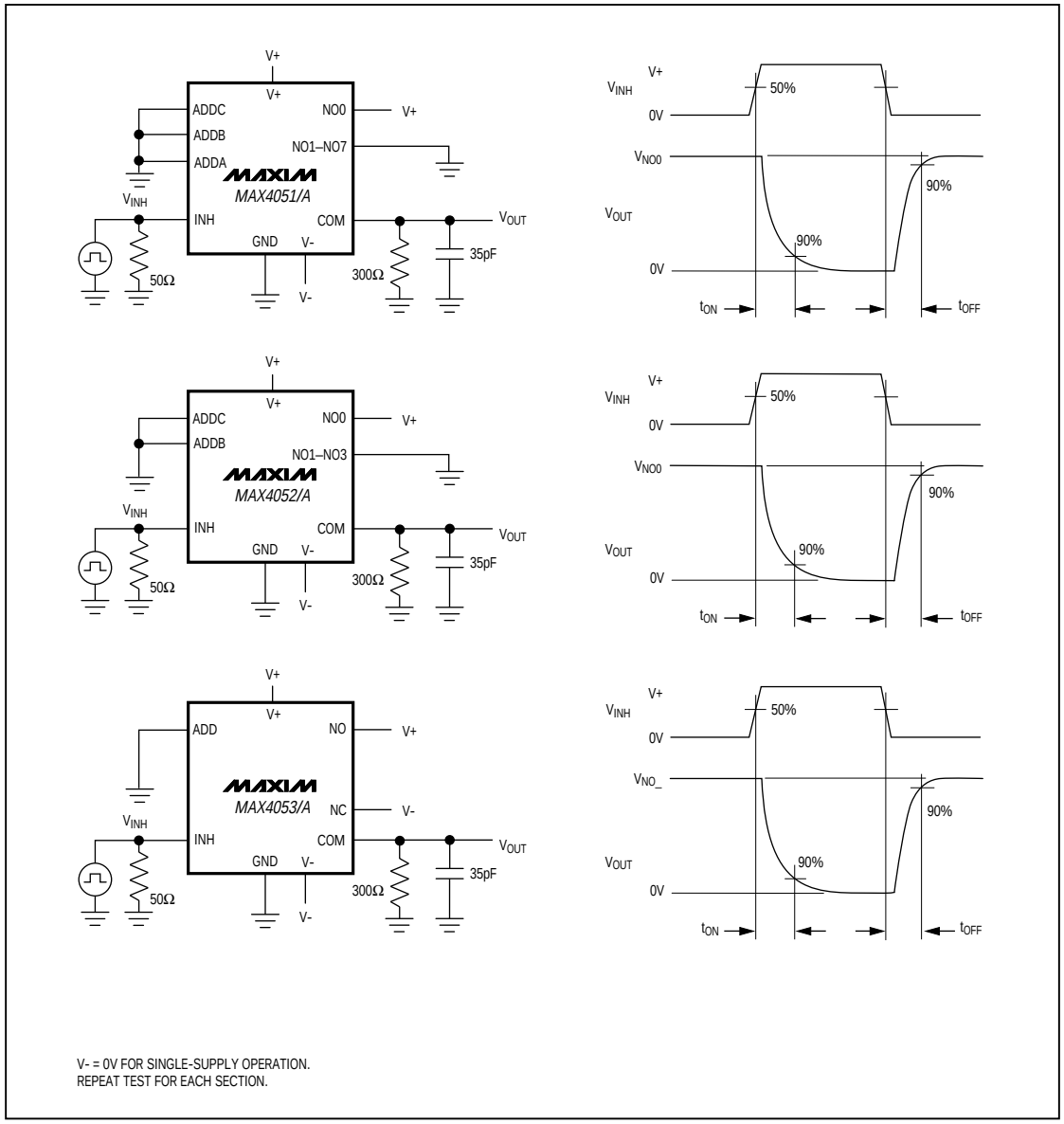


Figure 3. Enable Switching Time

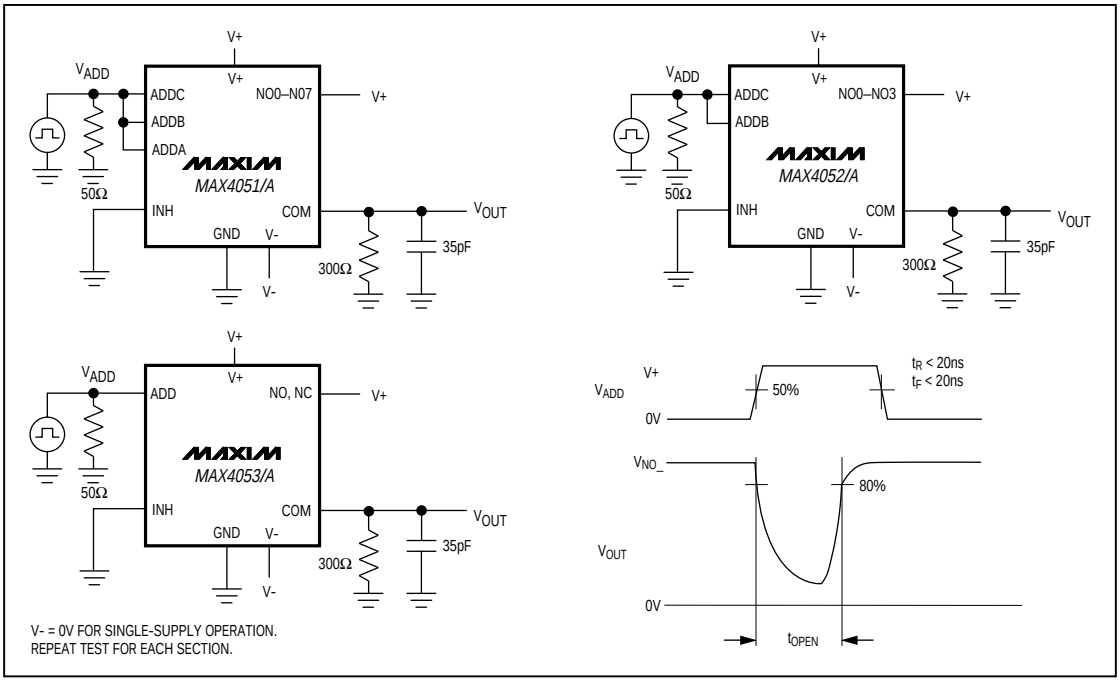


Figure 4. Break-Before-Make Interval

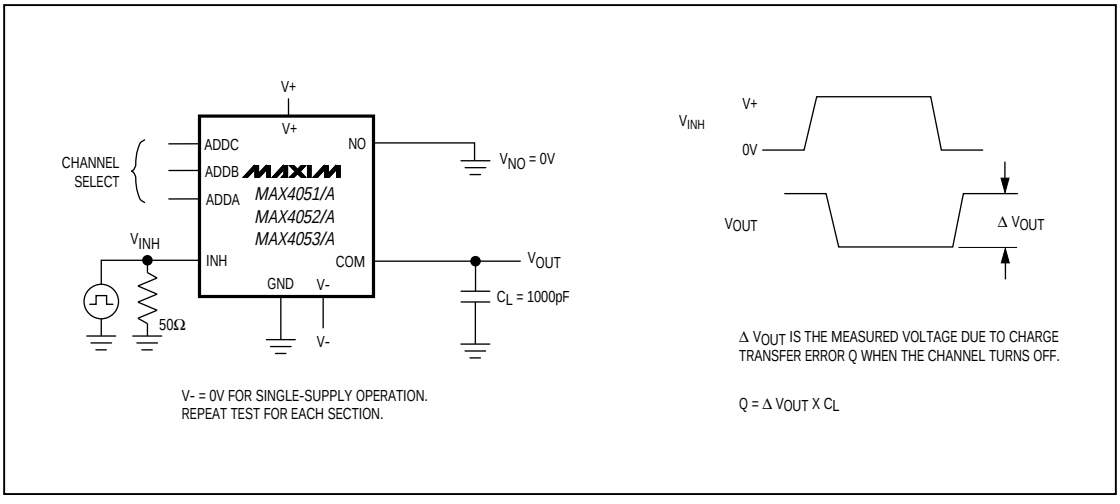


Figure 5. Charge Injection

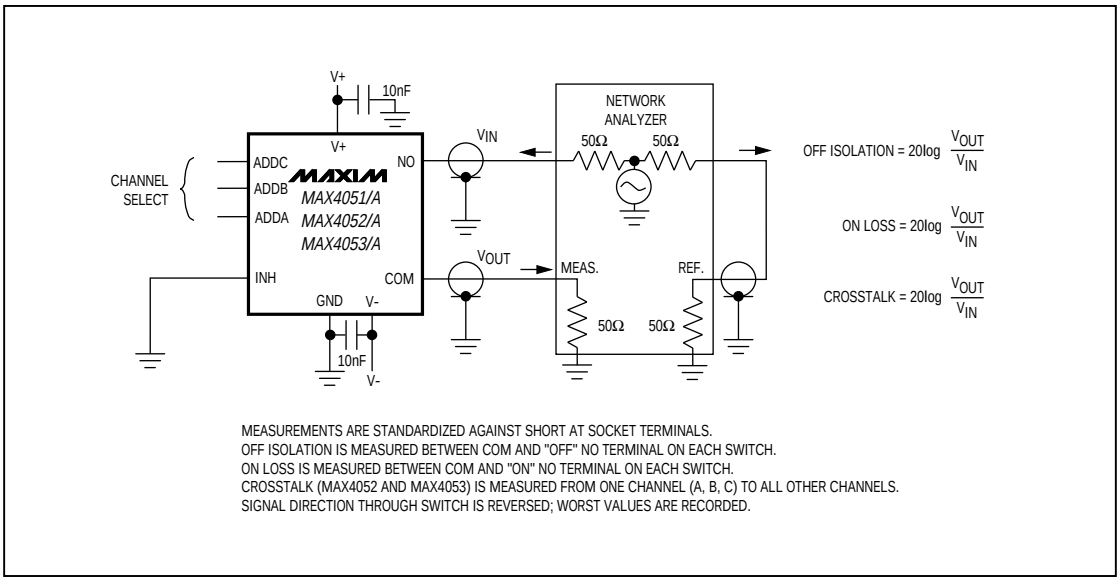


Figure 6. Off Isolation, On Loss, and Crosstalk

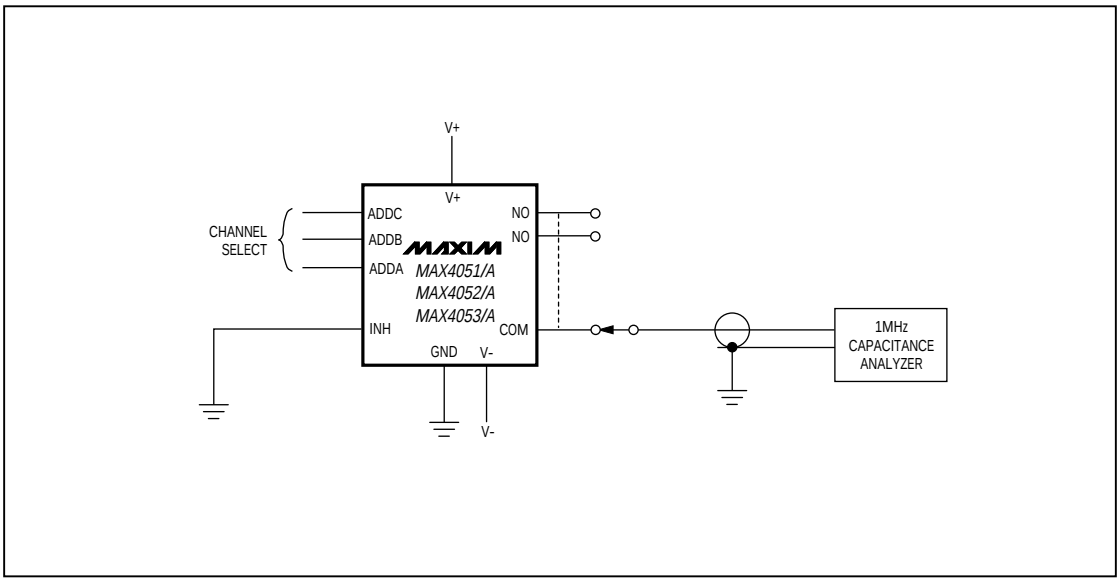


Figure 7. NO/COM Capacitance

Ordering Information (continued)

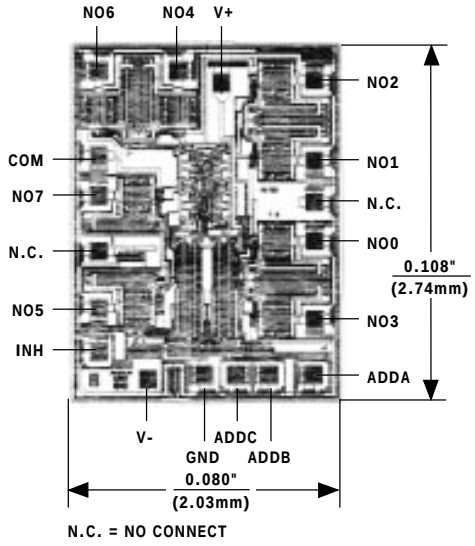
PART	TEMP. RANGE	PIN-PACKAGE
MAX4051AEPE	-40°C to +85°C	16 Plastic DIP
MAX4051AESE	-40°C to +85°C	16 Narrow SO
MAX4051AEEE	-40°C to +85°C	16 QSOP
MAX4051AMJE	-55°C to +125°C	16 CERDIP**
MAX4051CPE	0°C to +70°C	16 Plastic DIP
MAX4051CSE	0°C to +70°C	16 Narrow SO
MAX4051CEE	0°C to +70°C	16 QSOP
MAX4051C/D	0°C to +70°C	Dice*
MAX4051EPE	-40°C to +85°C	16 Plastic DIP
MAX4051ESE	-40°C to +85°C	16 Narrow SO
MAX4051EEE	-40°C to +85°C	16 QSOP
MAX4051MJE	-55°C to +125°C	16 CERDIP**
MAX4052ACPE	0°C to +70°C	16 Plastic DIP
MAX4052ACSE	0°C to +70°C	16 Narrow SO
MAX4052ACEE	0°C to +70°C	16 QSOP
MAX4052AEPE	-40°C to +85°C	16 Plastic DIP
MAX4052AESE	-40°C to +85°C	16 Narrow SO
MAX4052AEEE	-40°C to +85°C	16 QSOP
MAX4052AMJE	-55°C to +125°C	16 CERDIP**
MAX4052CPE	0°C to +70°C	16 Plastic DIP
MAX4052CSE	0°C to +70°C	16 Narrow SO
MAX4052CEE	0°C to +70°C	16 QSOP
MAX4052C/D	0°C to +70°C	Dice*
MAX4052EPE	-40°C to +85°C	16 Plastic DIP
MAX4052ESE	-40°C to +85°C	16 Narrow SO
MAX4052EEE	-40°C to +85°C	16 QSOP
MAX4052MJE	-55°C to +125°C	16 CERDIP**

PART	TEMP. RANGE	PIN-PACKAGE
MAX4053ACPE	0°C to +70°C	16 Plastic DIP
MAX4053ACSE	0°C to +70°C	16 Narrow SO
MAX4053ACEE	0°C to +70°C	16 QSOP
MAX4053AEPE	-40°C to +85°C	16 Plastic DIP
MAX4053AESE	-40°C to +85°C	16 Narrow SO
MAX4053AEEE	-40°C to +85°C	16 QSOP
MAX4053AMJE	-55°C to +125°C	16 CERDIP**
MAX4053CPE	0°C to +70°C	16 Plastic DIP
MAX4053CSE	0°C to +70°C	16 Narrow SO
MAX4053CEE	0°C to +70°C	16 QSOP
MAX4053C/D	0°C to +70°C	Dice*
MAX4053EPE	-40°C to +85°C	16 Plastic DIP
MAX4053ESE	-40°C to +85°C	16 Narrow SO
MAX4053EEE	-40°C to +85°C	16 QSOP
MAX4053MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

Chip Topography

MAX4051/A

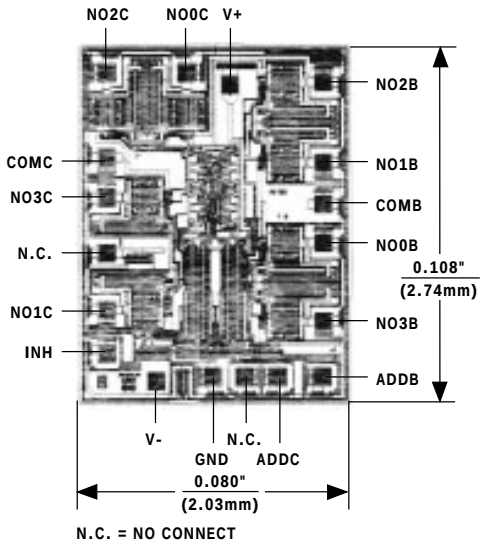


N.C. = NO CONNECT

TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

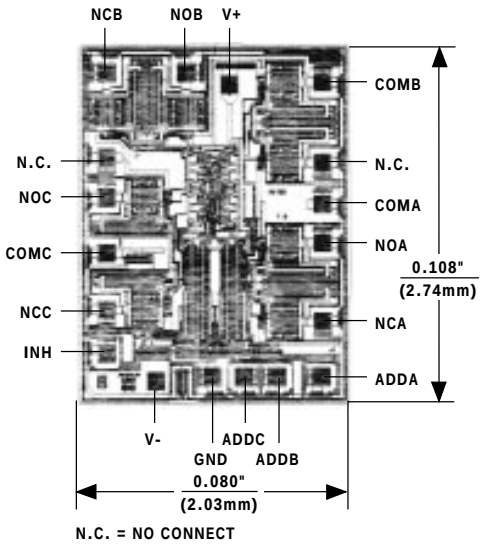
Chip Topographies (continued)

MAX4052/A



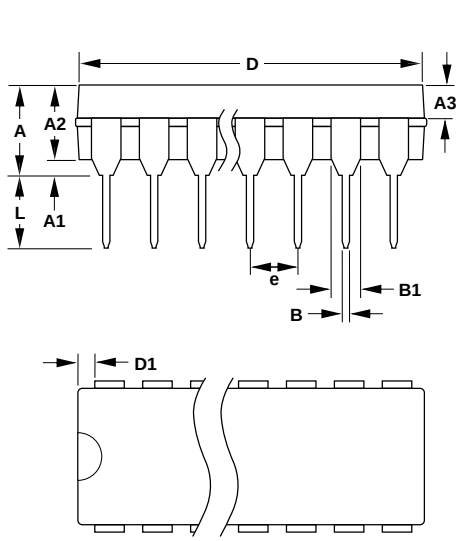
TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

MAX4053/A



TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

Package Information

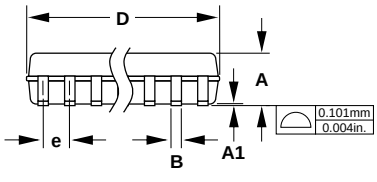


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

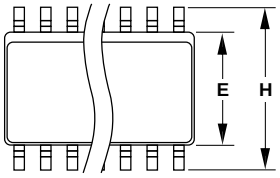
Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

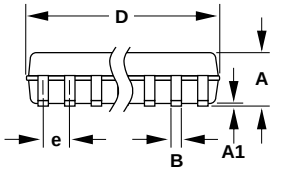


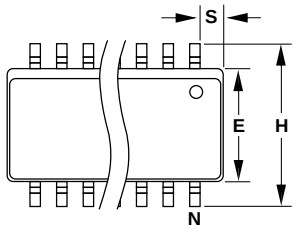
Narrow SO
SMALL-OUTLINE
PACKAGE
(0.150 in.)

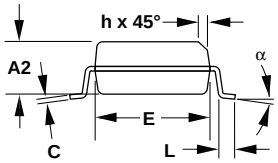
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

Packaging Information (continued)







DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.127	0.25
A2	0.055	0.061	1.40	1.55
B	0.008	0.012	0.20	0.31
C	0.0075	0.0098	0.19	0.25
D	SEE VARIATIONS			
E	0.150	0.157	3.81	3.99
e	0.25 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.189	0.196	4.80	4.98
S	16	0.0020	0.0070	0.05	0.18
D	20	0.337	0.344	8.56	8.74
S	20	0.0500	0.0550	1.27	1.40
D	24	0.337	0.344	8.56	8.74
S	24	0.0250	0.0300	0.64	0.76
D	28	0.386	0.393	9.80	9.98
S	28	0.0250	0.0300	0.64	0.76

21-0055A

QSOP
QUARTER
SMALL-OUTLINE
PACKAGE

FSDM07652RB

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Advanced Burst-Mode operation consumes under 1 W at 240VAC & 0.5W load
- Precision Fixed Operating Frequency (66kHz)
- Internal Start-up Circuit
- Improved Pulse by Pulse Current Limiting
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lock Out (UVLO) with hysteresis
- Low Operating Current (2.5mA)
- Built-in Soft Start

Application

- SMPS for LCD monitor and STB
- Adaptor

Description

The FSDM07652RB is an integrated Pulse Width Modulator (PWM) and Sense FET specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combine an avalanche rugged Sense FET with a current mode PWM control block. The PWM controller includes integrated fixed frequency oscillator, under voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft start, temperature compensated precise current sources for a loop compensation and self protection circuitry. Compared with discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight simultaneously increasing efficiency, productivity, and system reliability. This device is a basic platform well suited for cost effective designs of flyback converters.

OUTPUT POWER TABLE				
PRODUCT	230VAC ±15%(3)		85-265VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
FSDM0565RB	60W	70W	50W	60W
FSDM07652RB	70W	80W	60W	70W

Table 1. Maximum Output Power

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
2. Maximum practical continuous power in an open frame design at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

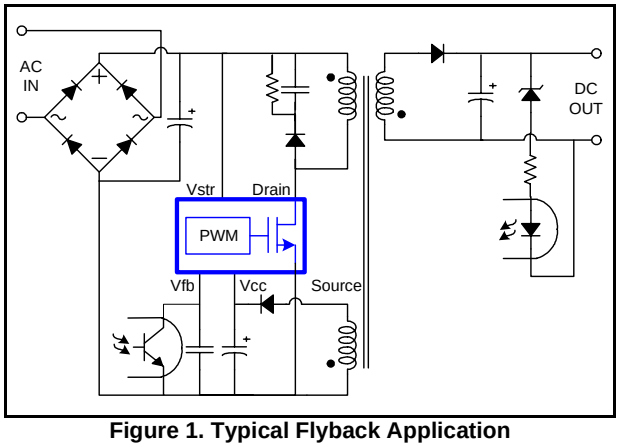


Figure 1. Typical Flyback Application

Internal Block Diagram

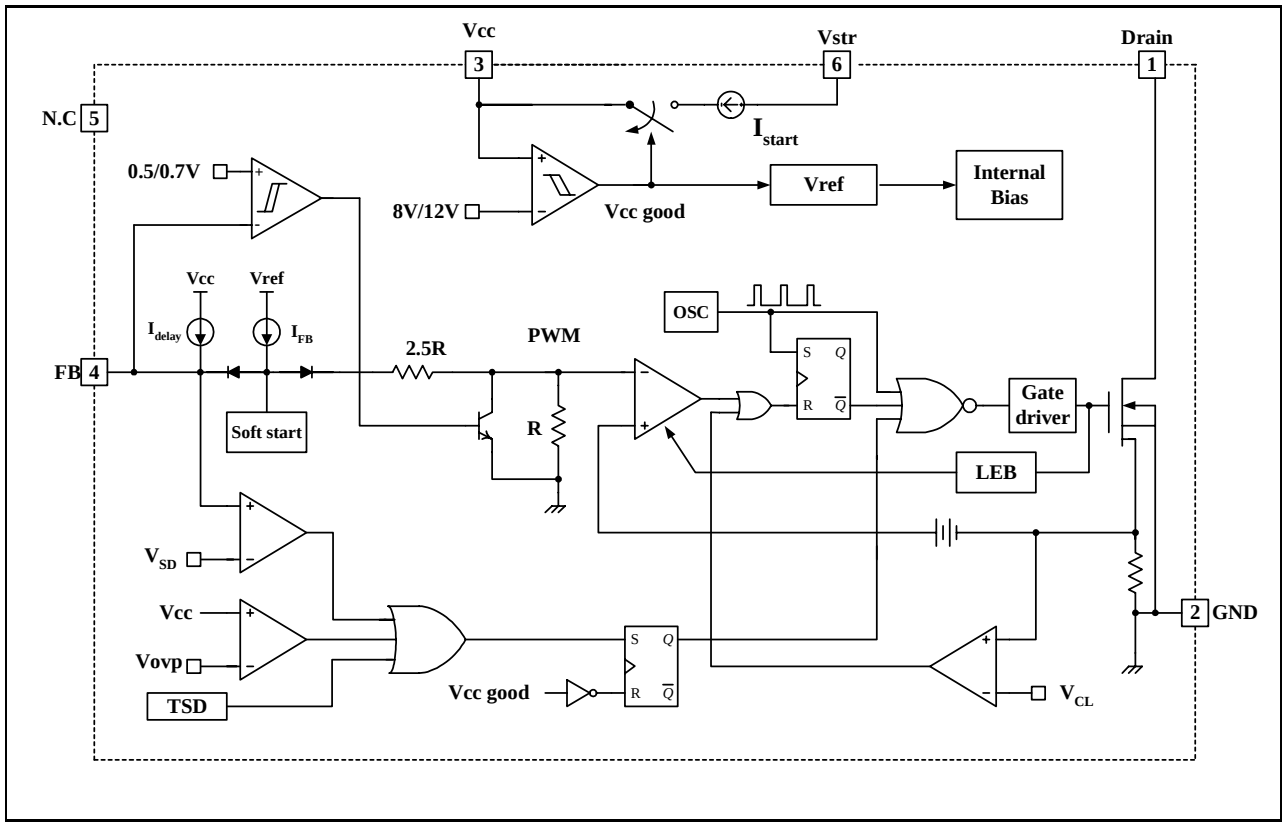


Figure 2. Functional Block Diagram of FSDM07652RB

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power Sense FET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the Sense FET source.
3	Vcc	This pin is the positive supply voltage input. During start up, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 12V, the internal high voltage current source is disabled and the power is supplied from the auxiliary transformer winding.
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6.0V, the over load protection is activated resulting in shutdown of the FPS^{TM}.
5	N.C	-
6	Vstr	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 12V, the internal current source is disabled.

Pin Configuration

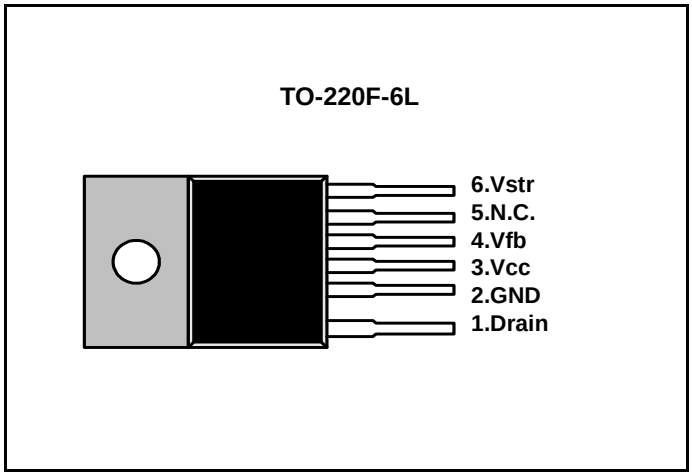


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Vstr Max Voltage	V_{STR}	650	V
Pulsed Drain current (Tc=25°C)(1)	I_{DM}	28	A_{DC}
Continuous Drain Current(Tc=25°C)	I_D	7	A
Continuous Drain Current(Tc=100°C)		4.5	A
Single pulsed avalanche energy (2)	E_{AS}	370	mJ
Single pulsed avalanche current (3)	I_{AS}	-	A
Supply voltage	V_{CC}	19	V
Input voltage range	V_{FB}	-0.3 to V_{CC}	V
Total power dissipation(Tc=25°C)	P_D(Watt H/S)	62	W
Operating junction temperature	T_j	+150	°C
Operating ambient temperature	T_A	-25 to +85	°C
Storage temperature range	T_{STG}	-55 to +150	°C

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L=14mH, starting Tj=25°C
3. L=13uH, starting Tj=25°C

Thermal Impedance

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal	θ_{JA}(1)	46.40	°C/W
Junction-to-Case Thermal	θ_{JC}(2)	2.49	°C/W

Notes:

1. Free standing with no heat-sink under natural convection.
2. Infinite cooling condition - Refer to the SEMI G30-88.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V	-	-	50	μA
		V_{DS}= 520V V_{GS} = 0V, T_C = 125°C	-	-	200	μA
Static drain source on resistance (1)	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	-	1.4	1.6	Ω
Output capacitance	C_{OSS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	100	-	pF
Turn on delay time	$T_{D(ON)}$	V_{DD}= 325V, I_D= 5A (MOSFET switching time is essentially independent of operating temperature)	-	22	-	ns
Rise time	T_R		-	60	-	
Turn off delay time	$T_{D(OFF)}$		-	115	-	
Fall time	T_F		-	65	-	
CONTROL SECTION						
Initial frequency	F_{OSC}	V_{FB} = 3V	60	66	72	kHz
Voltage stability	F_{STABLE}	13V ≤ Vcc ≤ 18V	0	1	3	%
Temperature stability (2)	ΔF_{OSC}	-25°C ≤ Ta ≤ 85°C	0	±5	±10	%
Maximum duty cycle	D_{MAX}	-	75	80	85	%
Minimum duty cycle	D_{MIN}	-	-	-	0	%
Start threshold voltage	V_{START}	V_{FB}=GND	11	12	13	V
Stop threshold voltage	V_{STOP}	V_{FB}=GND	7	8	9	V
Feedback source current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Soft-start time	T_S	Vfb=3	-	10	15	ms
Leading Edge Blanking time	T_{LEB}	-	-	250	-	ns
BURST MODE SECTION						
Burst Mode Voltages (2)	V_{BURH}	Vcc=14V	-	0.7	-	V
	V_{BURL}	Vcc=14V	-	0.5	-	V
PROTECTION SECTION						
Peak current limit (4)	I_{OVER}	V_{FB}=5V, V_{CC}=14V	2.2	2.5	2.8	A
Over voltage protection	V_{OVP}	-	18	19	20	V
Thermal shutdown temperature (2)	T_{SD}		130	145	160	°C
Shutdown feedback voltage	V_{SD}	V_{FB} ≥ 5.5V	5.5	6.0	6.5	V
Shutdown delay current	I_{DELAY}	V_{FB}=5V	2.8	3.5	4.2	μA

TOTAL DEVICE SECTION						
Operating supply current (5)	I_{OP}	V_{FB}=GND, V_{CC}=14V	-	2.5	5	mA
	$I_{OP(MIN)}$	V_{FB}=GND, V_{CC}=10V				
	$I_{OP(MAX)}$	V_{FB}=GND, V_{CC}=18V				

Notes:

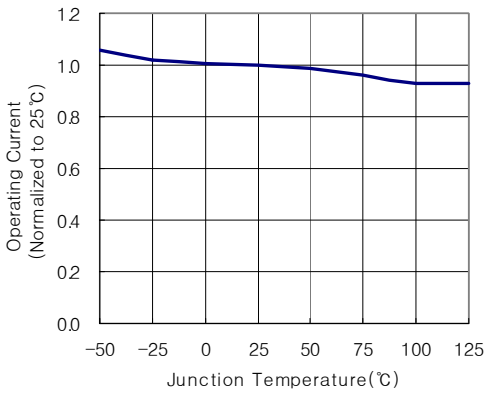
1. Pulse test : Pulse width ≤ 300μS, duty ≤ 2%
2. These parameters, although guaranteed at the design, are not tested in mass production.
3. These parameters, although guaranteed, are tested only in EDS(wafer test) process.
4. These parameters indicate the inductor current.
5. This parameter is the current flowing into the control IC.

Comparison Between FS6M07652RTC and FSDM07652RB

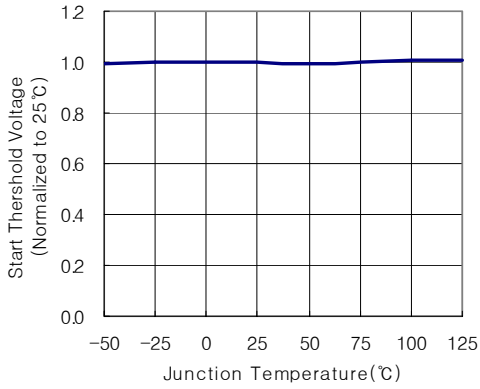
Function	FS6M07652RTC	FSDM07652RB	FSDM07652RB Advantages
Soft-Start	Adjustable soft-start time using an external capacitor	Internal soft-start with typically 10ms (fixed)	• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	• Built into controller • Output voltage drops to around half	• Built into controller • Output voltage fixed	• Improve light load efficiency • Reduces no-load consumption

Typical Performance Characteristics

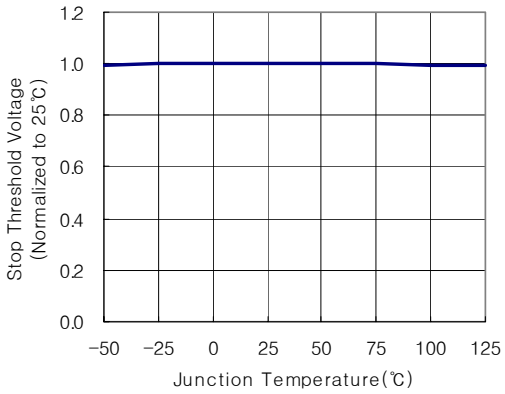
(These Characteristic Graphs are Normalized at Ta= 25°C)



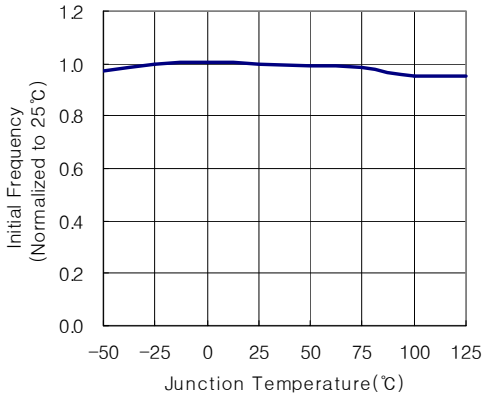
Operating Current vs. Temp



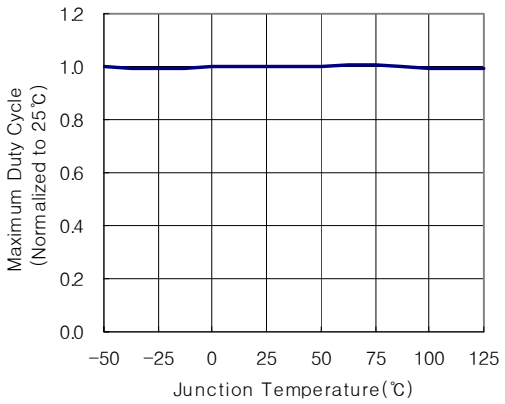
Start Threshold Voltage vs. Temp



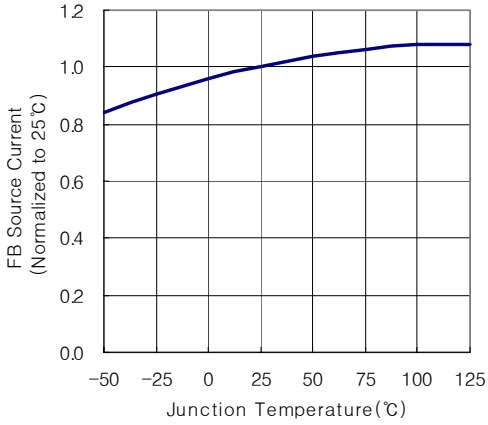
Stop Threshold Voltage vs. Temp



Operating Freqency vs. Temp



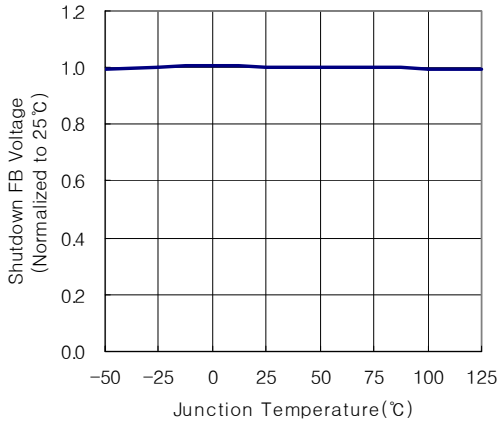
Maximum Duty vs. Temp



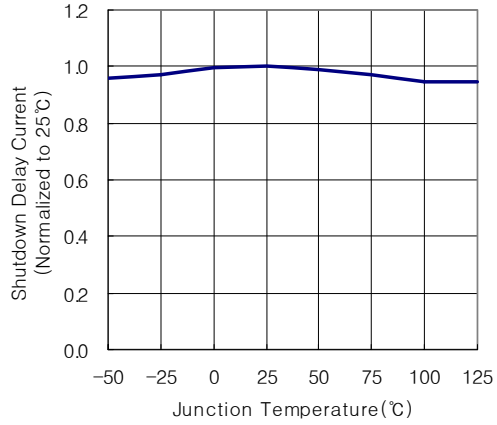
Feedback Source Current vs. Temp

Typical Performance Characteristics (Continued)

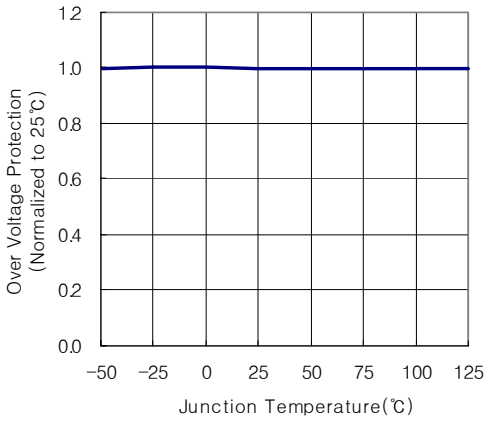
(These Characteristic Graphs are Normalized at Ta= 25°C)



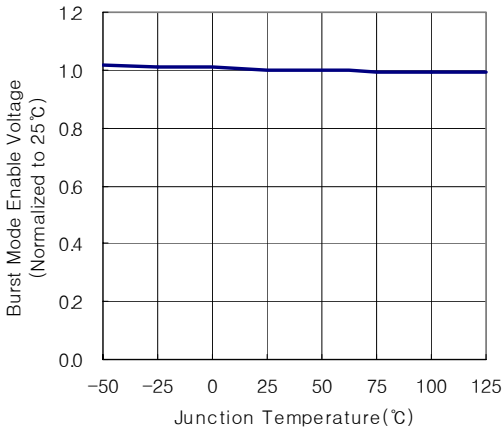
ShutDown Feedback Voltage vs. Temp



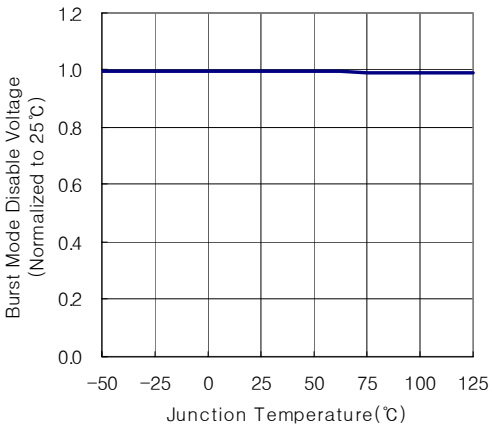
ShutDown Delay Current vs. Temp



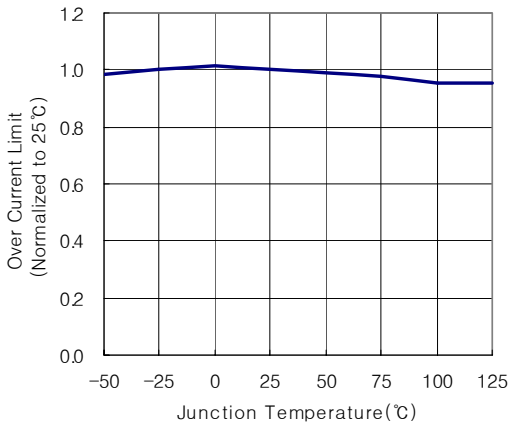
Over Voltage Protection vs. Temp



Burst Mode Enable Voltage vs. Temp



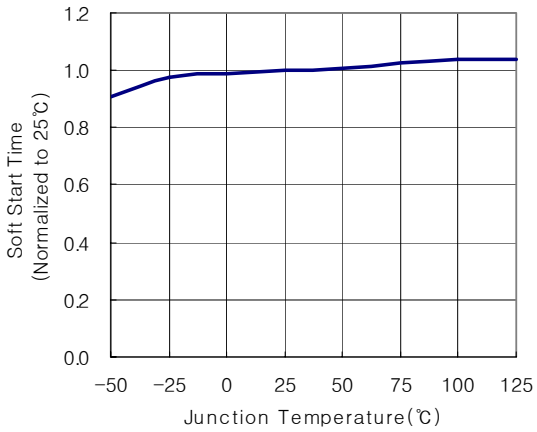
Burst Mode Disable Voltage vs. Temp



Current Limit vs. Temp

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)



Soft Start Time vs. Temp

Functional Description

1. Startup : In previous generations of Fairchild Power Switches (FPS^{TM}) the Vcc pin had an external start-up resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source. At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (C_{Vcc}) that is connected to the Vcc pin as illustrated in Figure 4. When Vcc reaches 12V, the FSDM07652RB begins switching and the internal high voltage current source is disabled. Then, the FSDM07652RB continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless Vcc goes below the stop voltage of 8V.

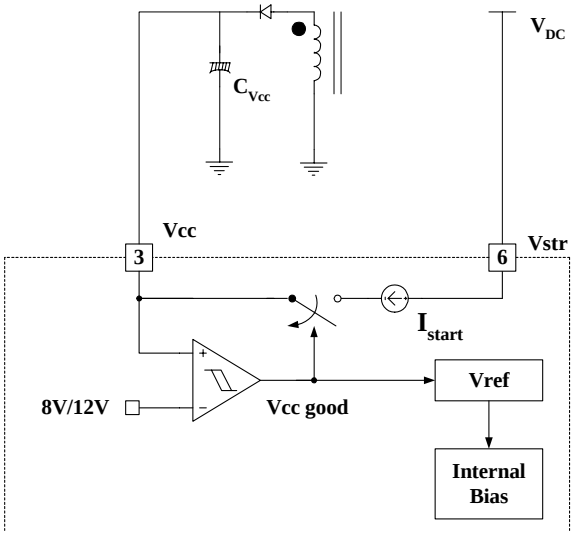


Figure 4. Internal startup circuit

2. Feedback Control : FSDM07652RB employs current mode control, as shown in Figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-pulse current limit: Because current mode control is employed, the peak current through the Sense FET is limited by the inverting input of PWM comparator (Vfb*) as shown in Figure 5. Assuming that the 0.9mA current source flows only through the internal resistor (2.5R +R= 2.8 kΩ), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (Vfb) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the current through the Sense FET is limited.

2.2 Leading edge blanking (LEB) : At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the Rsense resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSDM07652RB employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

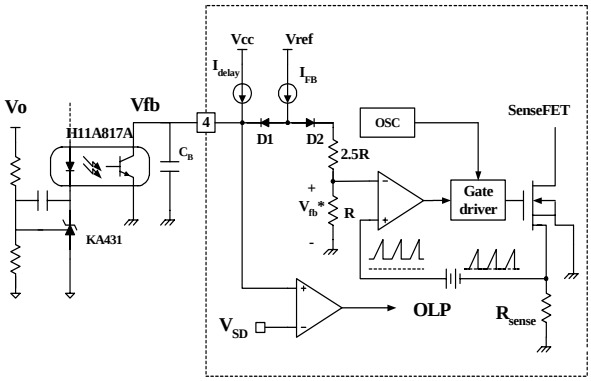


Figure 5. Pulse width modulation (PWM) circuit

3. Protection Circuit : The FSDM07652RB has several self protective functions such as over load protection (OLP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost. Once the fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage, 8V, the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage,12V, the FSDM07652RB resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated (see Figure 6).

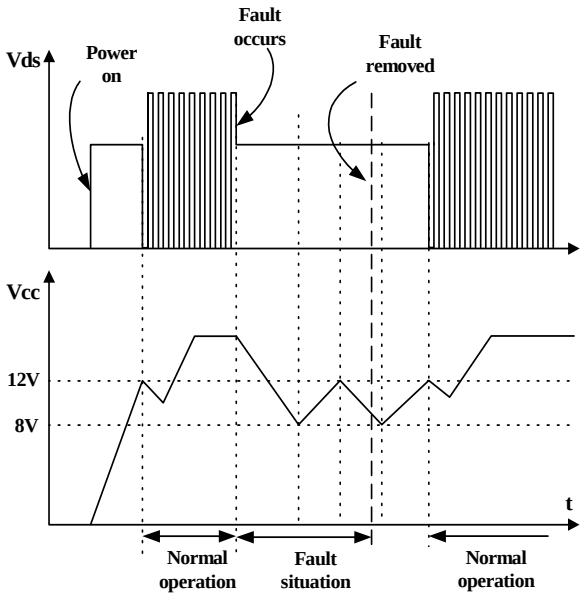


Figure 6. Auto restart operation

3.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be activated during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 3.5uA current source starts to charge C_B slowly up to Vcc. In this condition, Vfb continues increasing until it reaches 6V, when the switching operation is terminated as shown in Figure 7. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 3.5uA. In general, a 10 ~ 50 ms delay time is typical for most applications.

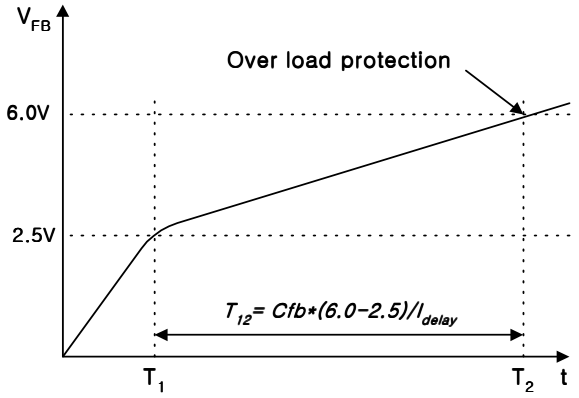


Figure 7. Over load protection

3.2 Over voltage Protection (OVP) : If the secondary side feedback circuit were to malfunction or a solder defect caused an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FSDM07652RB uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

3.3 Thermal Shutdown (TSD) : The Sense FET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the Sense FET. When the temperature exceeds approximately 150°C, the thermal shutdown is activated.

4. Soft Start : The FSDM07652RB has an internal soft start circuit that increases PWM comparator inverting input voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 10msec, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

5. Burst operation : In order to minimize power dissipation in standby mode, the FSDM07652RB enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(500mV). At this point switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}(700mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

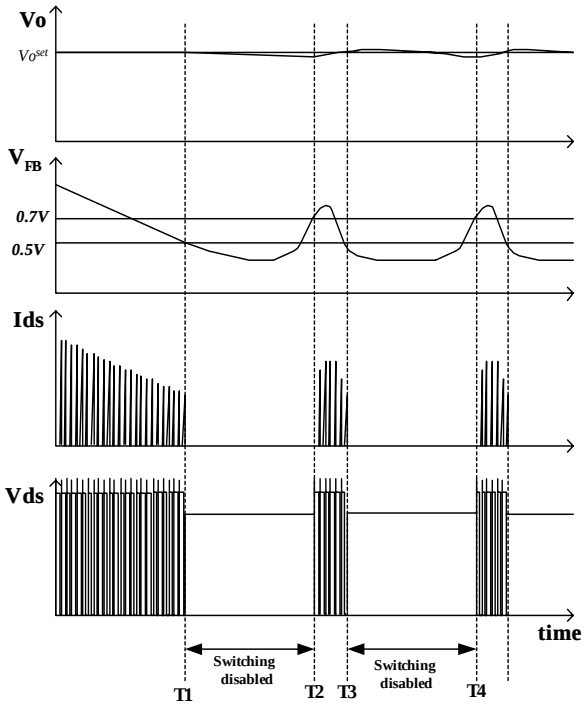


Figure 8. Waveforms of burst operation

Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
LCD Monitor	40W	Universal input (85-265Vac)	5V (2.0A) 12V (2.5A)

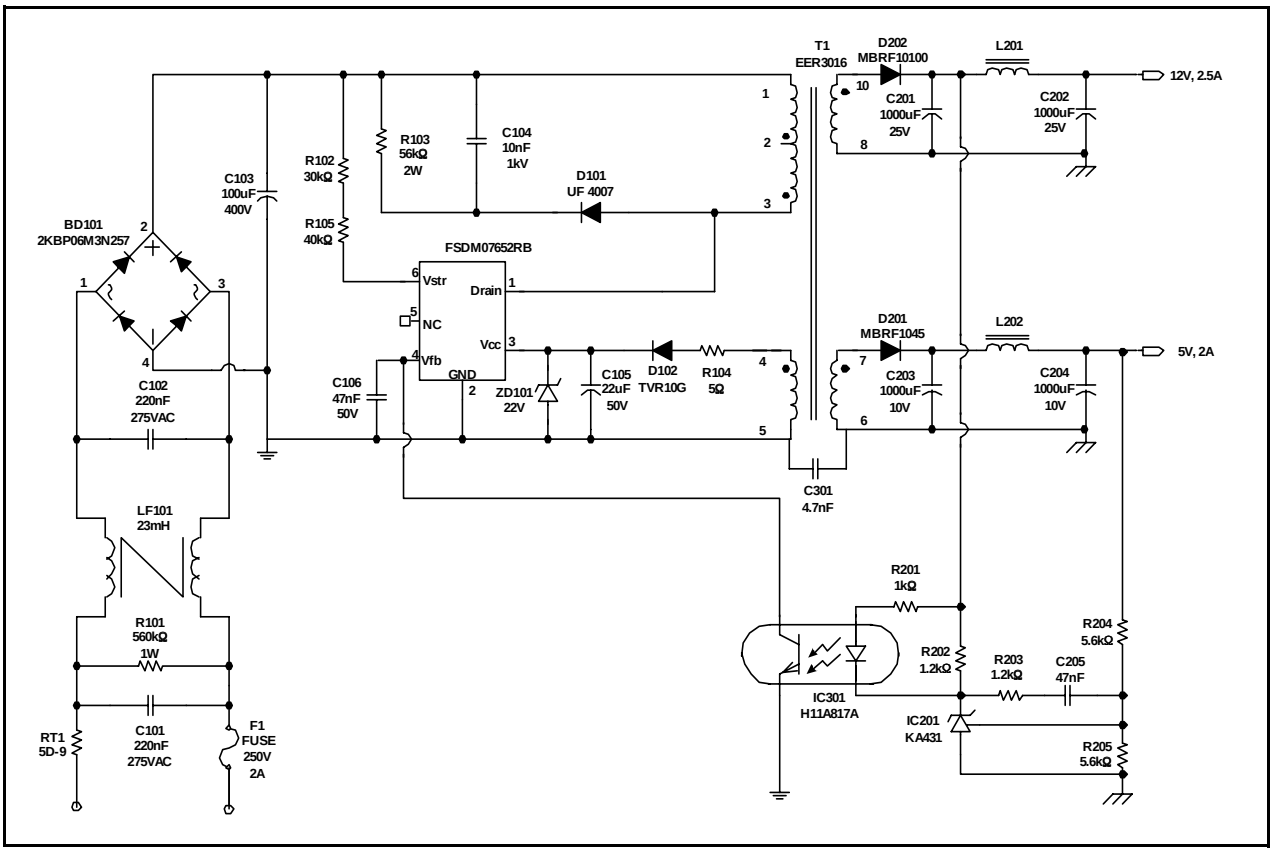
Features

- High efficiency (>81% at 85Vac input)
- Low zero load power consumption (<300mW at 240Vac input)
- Low standby mode power consumption (<800mW at 240Vac input and 0.3W load)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (10ms)

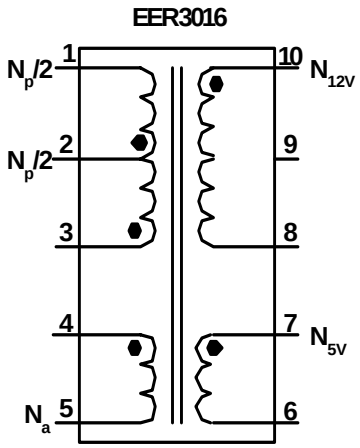
Key Design Notes

- Resistors R102 and R105 are employed to prevent start-up at low input voltage
- The delay time for over load protection is designed to be about 50ms with C106 of 47nF. If a faster triggering of OLP is required, C106 can be reduced to 10nF.

1. Schematic



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	4 → 5	$0.2^{\phi} \times 1$	8	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	2 → 1	$0.4^{\phi} \times 1$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N_{12V}	10 → 8	$0.3^{\phi} \times 3$	7	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N5V	7 → 6	$0.3^{\phi} \times 3$	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	3 → 2	$0.4^{\phi} \times 1$	18	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	520uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max	2^{nd} all short

5. Core & Bobbin

Core : EER 3016
Bobbin : EER3016
Ae(mm2) : 96

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Fuse			C301	4.7nF	Polyester Film Cap.
F101	2A/250V				
NTC			**Inductor**		
RT101	5D-9		L201	5uH	Wire 1.2mm
Resistor			L202	5uH	Wire 1.2mm
R101	560K	1W			
R102	30K	1/4W			
R103	56K	2W			
R104	5	1/4W	**Diode**		
R105	40K	1/4W	D101	UF4007	
R201	1K	1/4W	D102	TVR10G	
R202	1.2K	1/4W	D201	MBRF1045	
R203	1.2K	1/4W	D202	MBRF10100	
R204	5.6K	1/4W	ZD101	Zener Diode	22V
R205	5.6K	1/4W			
			Bridge Diode		
			BD101	2KBP06M 3N257	Bridge Diode
Capacitor					
C101	220nF/275VAC	Box Capacitor	**Line Filter**		
C102	220nF/275VAC	Box Capacitor	LF101	23mH	Wire 0.4mm
C103	100uF/400V	Electrolytic Capacitor	**IC**		
C104	10nF/1kV	Ceramic Capacitor	IC101	FSDM07652RB	FPS^{TM}(5A,650V)
C105	22uF/50V	Electrolytic Capacitor	IC201	KA431(TL431)	Voltage reference
C106	47nF/50V	Ceramic Capacitor	IC301	H11A817A	Opto-coupler
C201	1000uF/25V	Electrolytic Capacitor			
C202	1000uF/25V	Electrolytic Capacitor			
C203	1000uF/10V	Electrolytic Capacitor			
C204	1000uF/10V	Electrolytic Capacitor			
C205	47nF/50V	Ceramic Capacitor			

7. Layout

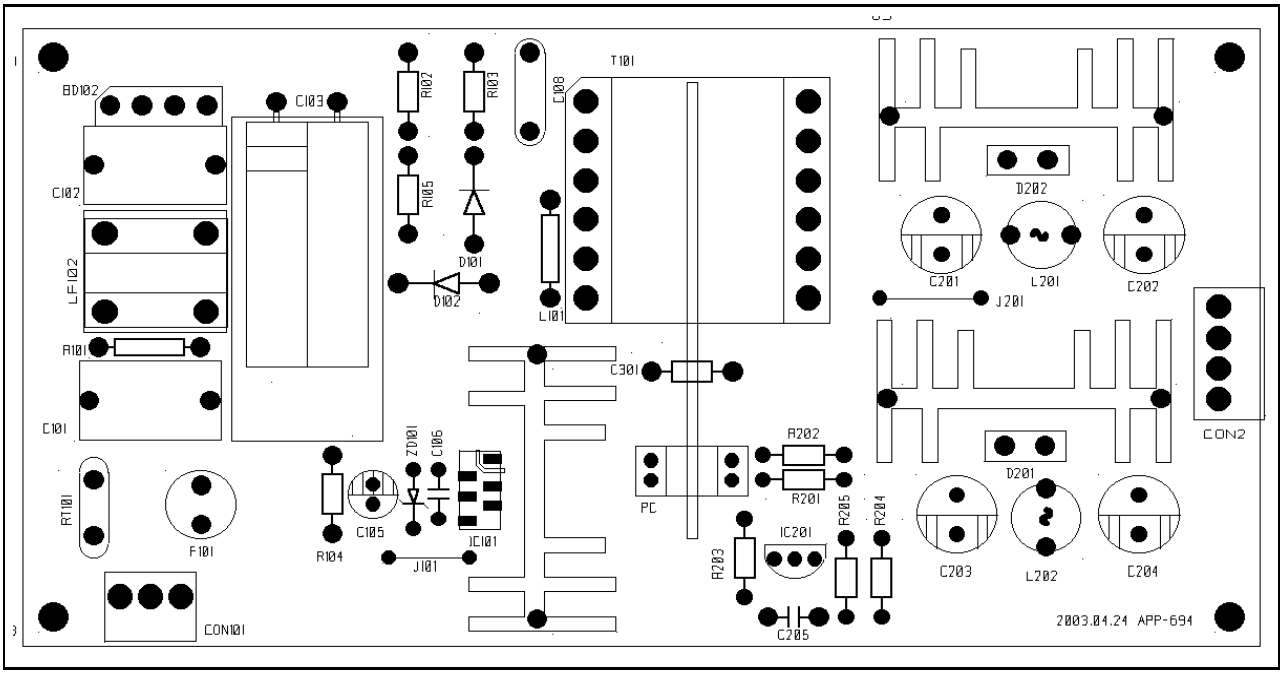


Figure 9. Layout Considerations for FSDM07652RB

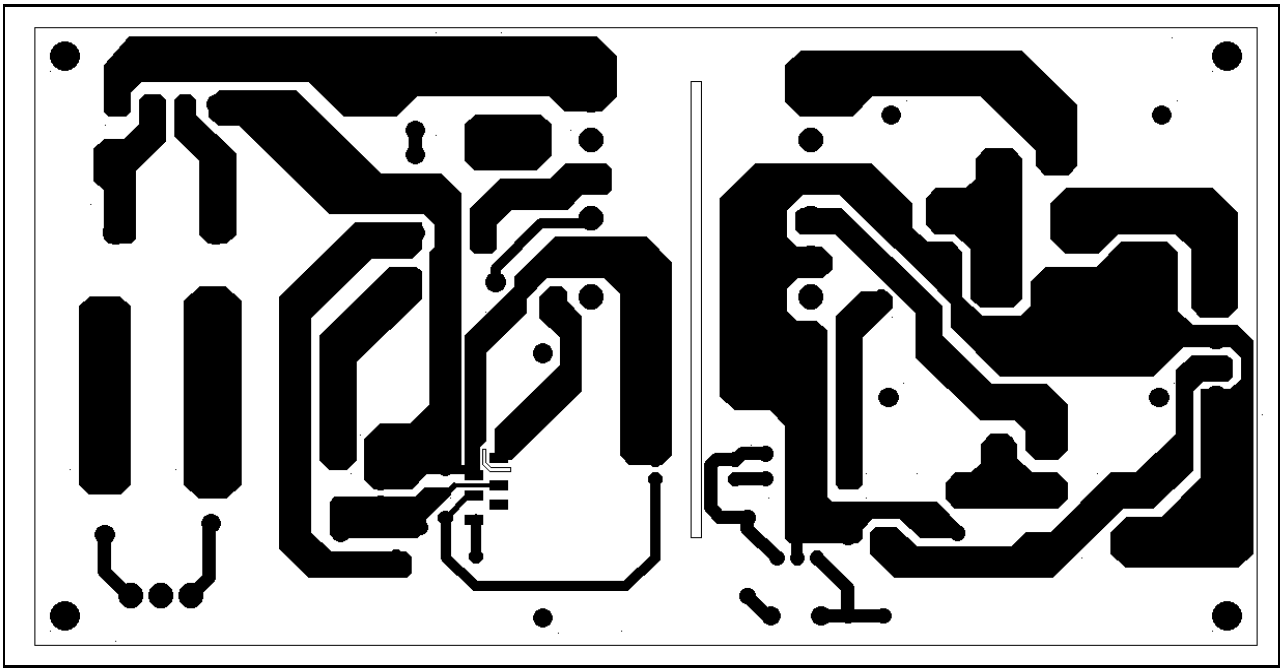
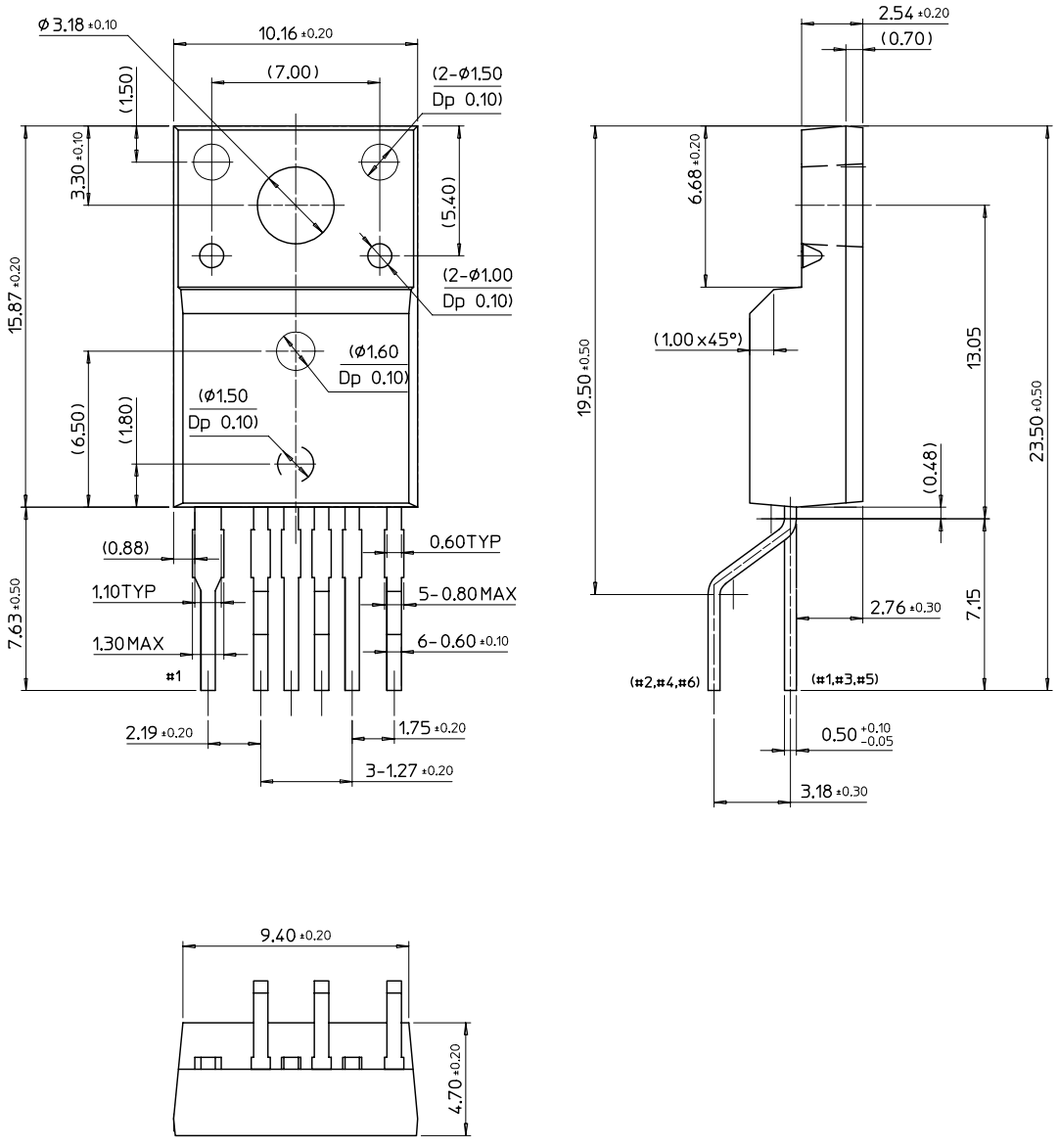


Figure 10. Layout Considerations for FSDM07652RB

Package Dimensions

TO-220F-6L(Forming)



Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FSDM07652RBWDTU	TO-220F-6L(Forming)	DM07652R	650V	1.6 Ω

WDTU : Forming Type

National Semiconductor

July 2003

LP2995
DDR Termination Regulator

General Description

The LP2995 linear regulator is designed to meet the JEDEC SSTL-2 and SSTL-3 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2995 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DDR DIMMS.

Patents Pending

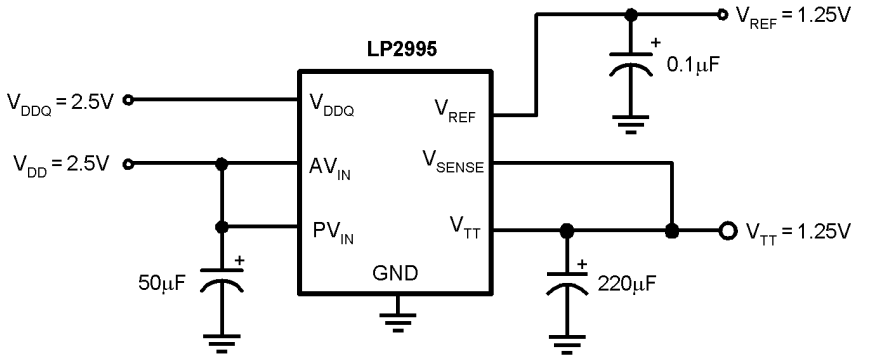
Features

- Low output voltage offset
- Works with +5v, +3.3v and 2.5v rails
- Source and sink current
- Low external component count
- No external resistors required
- Linear topology
- Available in SO-8, PSOP-8 or LLP-16 packages
- Low cost and easy to use

Applications

- DDR Termination Voltage
- SSTL-2
- SSTL-3

Typical Application Circuit



20039302

PQxxxEZ02Z Series

Low Voltage Operation Low Power-loss Voltage Regulator

■ Features

- Low voltage operation (Minimum operating voltage: 2.35V)
  2.5V input → available 1.5 to 1.8V output
- Low dissipation current
  Dissipation current at no load: MAX.2mA
  Output OFF-state dissipation current: MAX.5μA
- Low power-loss
- Built-in overcurrent and overheat protection functions

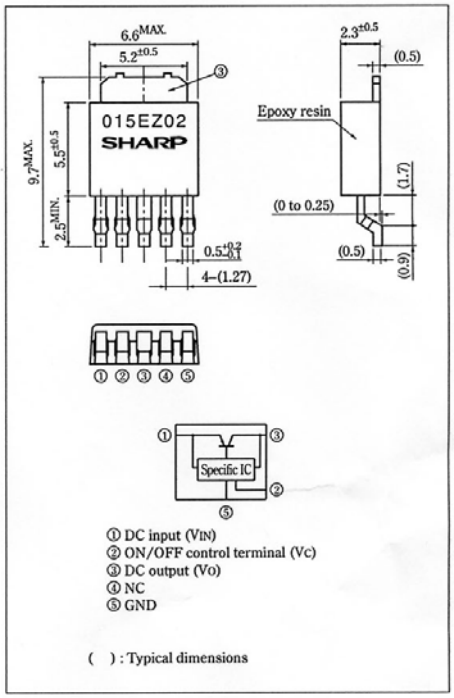
■ Applications

- Power supplies for personal computers and peripheral equipment
- Power supplies for various electronic equipment such as DVD player or STB

■ Model Line-up

Output current (Io)	Output Voltage (Vo)		
	1.5V	1.8V	2.5V
2.0A	PQ015EZ02Z	PQ018EZ02Z	PQ025EZ02Z

■ Outline Dimensions (Unit : mm)



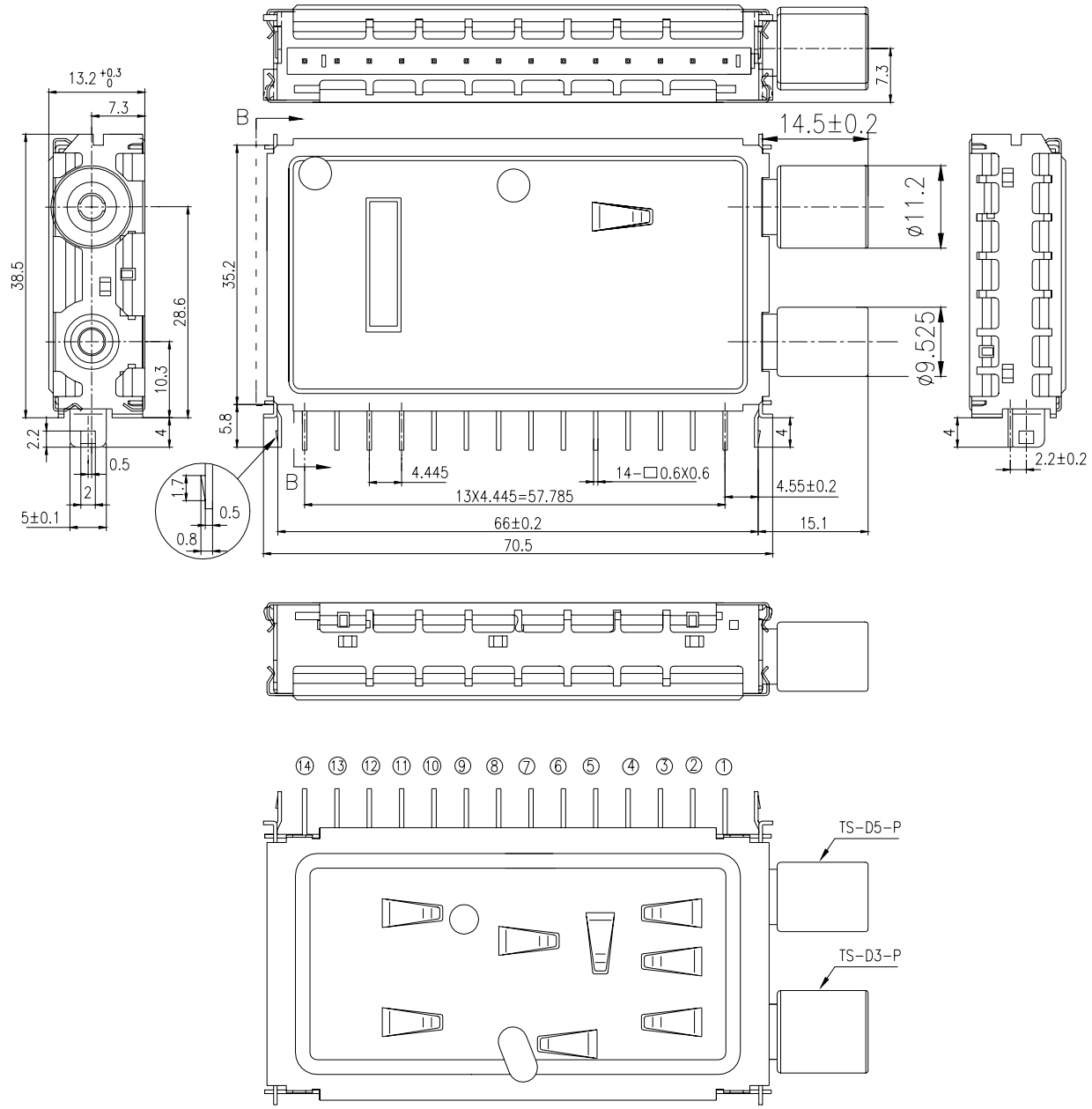
■ Absolute Maximum Ratings (Ta=25°C)

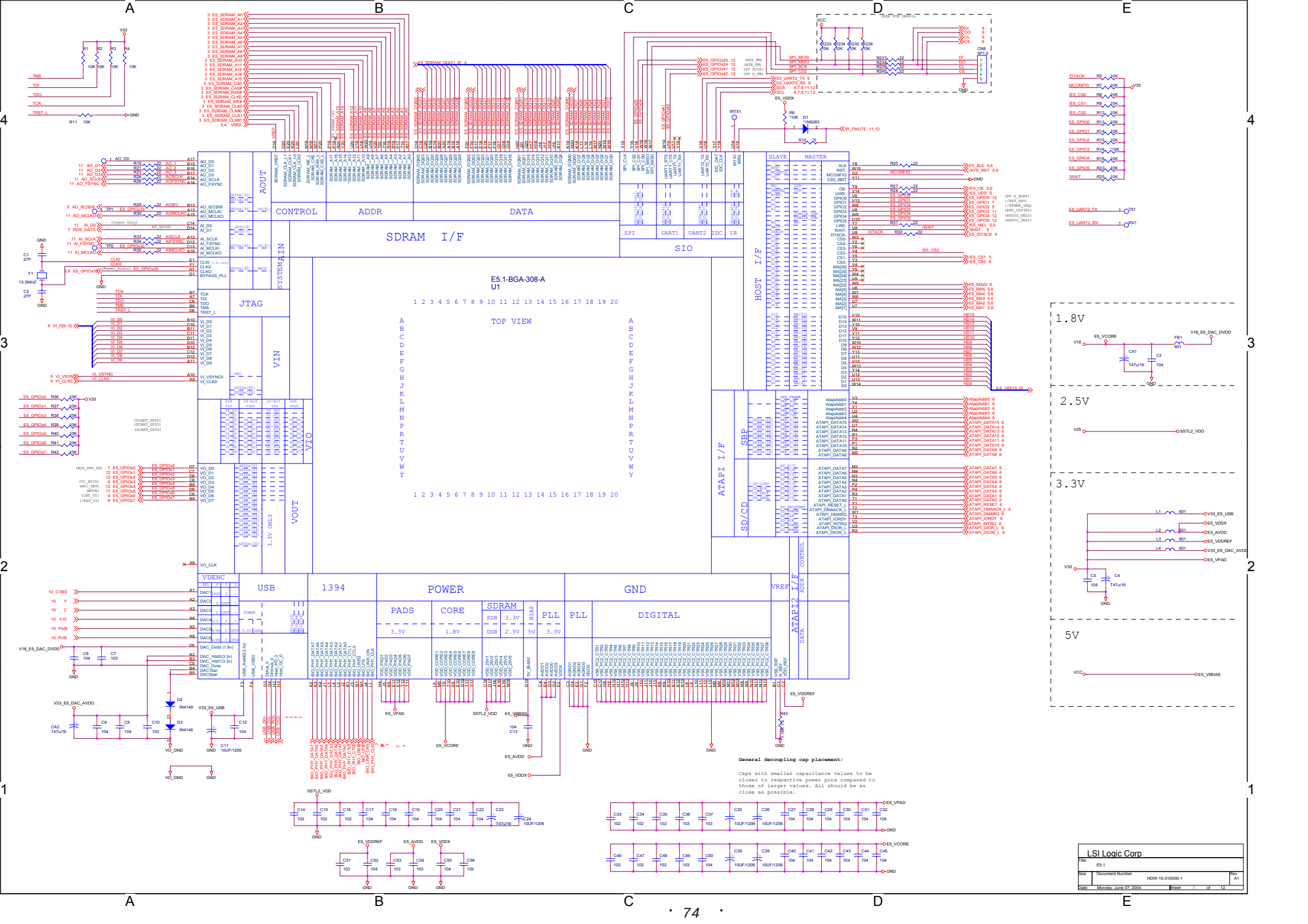
Parameter	Symbol	Rating	Unit
*1 Input voltage	V_{IN}	10	V
*1 ON/OFF control terminal voltage	V_C	10	V
Output current	Io	2	A
*2 Power dissipation	P_D	8	W
*3 Junction temperature	T_j	150	°C
Operating temperature	T_{opr}	−40 to + 85	°C
Storage temperature	T_{stg}	−40 to +150	°C
Soldering temperature	T_{sol}	260 (10s)	°C

*1 All are open except GND and applicable terminals
*2 P_D:With infinite heat sink
*3 Overheat protection may operate at 125 <=Tj<=150°C

•Please refer to the chapter " Handling Precautions ".

11.Terminal for External Connection & Outline Drawing

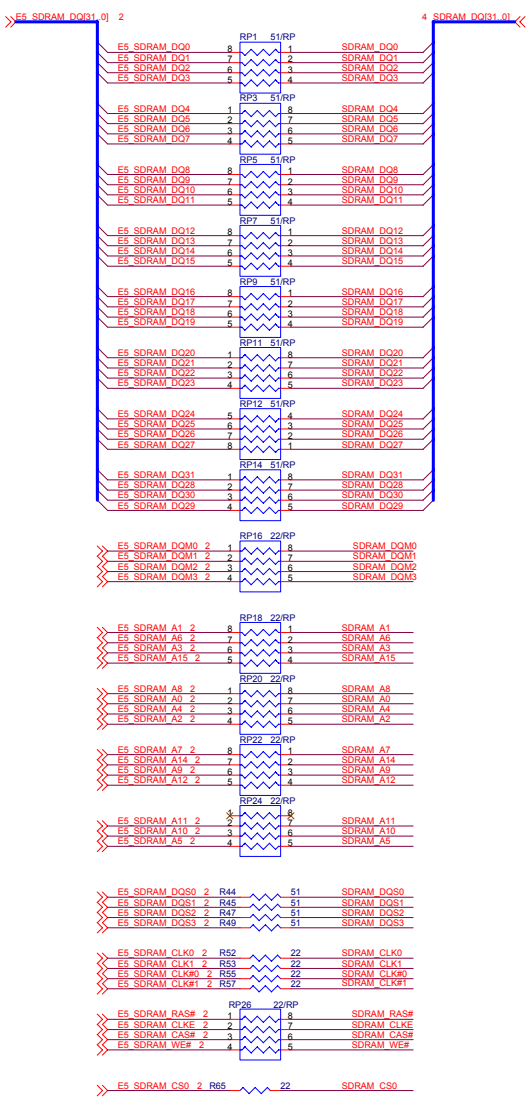


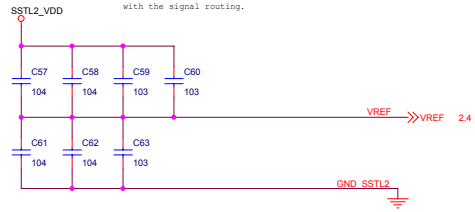

SDRAM I/F
SYSTEMAIN
AOUT
CONTROL
ADDR
DATA
SPI
UART1
UART2
IDC
IR
SIO
HOST I/F
SLAVE
MASTER
ATAPI I/F
SBP
SD/CD
JTAG
VIN
VOUT
VI/O
USB
1394
POWER
PADS
CORE
SDRAM
PLL
DIGITAL
GND
VREF
E5.1-BGA-308-A
U1
TOP VIEW
1.8V
2.5V
3.3V
5V
General decoupling cap placement:
Caps with smaller capacitance values to be closer to respective power pins compared to those of larger values. All should be as close as possible.
LSI Logic Corp
E5.1
HDW-10-310000-1
Monday, June 07, 2004

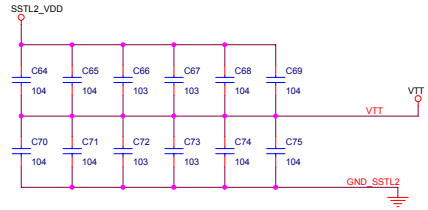
TERMINATION AT E5.1

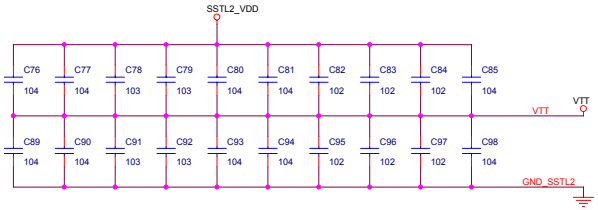
TERMINATION AT DDR

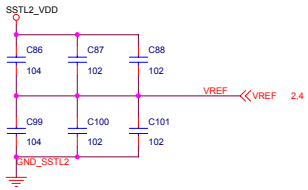
The VTT side of the terminaton resistors should be placed on a wide VTT island on the surface layer. The island is located at each end of the bus, so it does not interfere with the signal routing.







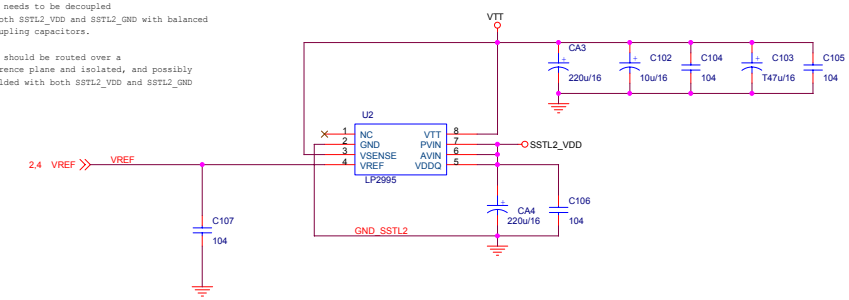




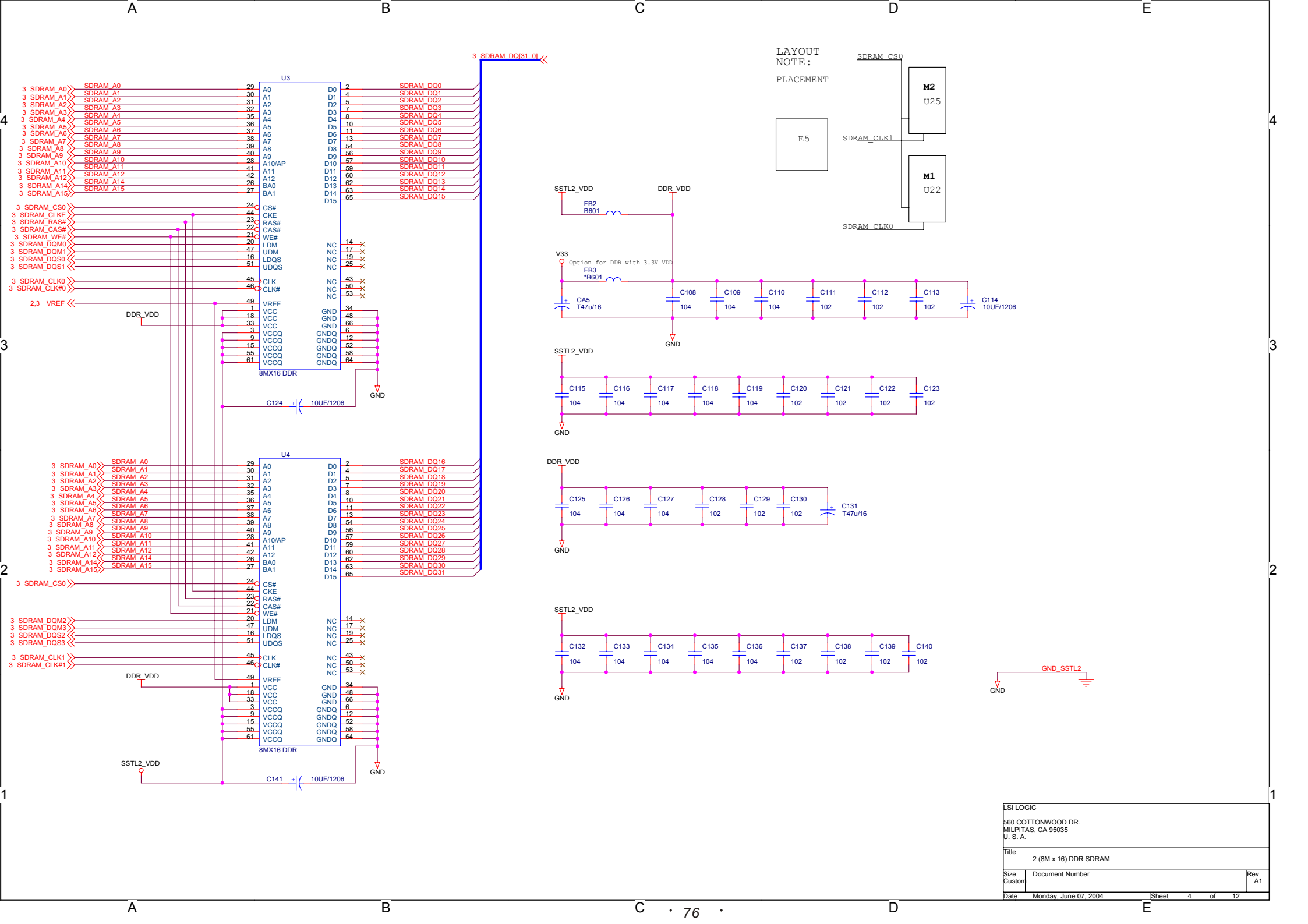
DDR TERMINATION VOLTAGE REGULATOR

VREF needs to be decoupled to both SSTL2_VDD and SSTL2_GND with balanced decoupling capacitors.

VREF should be routed over a reference plane and isolated, and possibly shielded with both SSTL2_VDD and SSTL2_GND

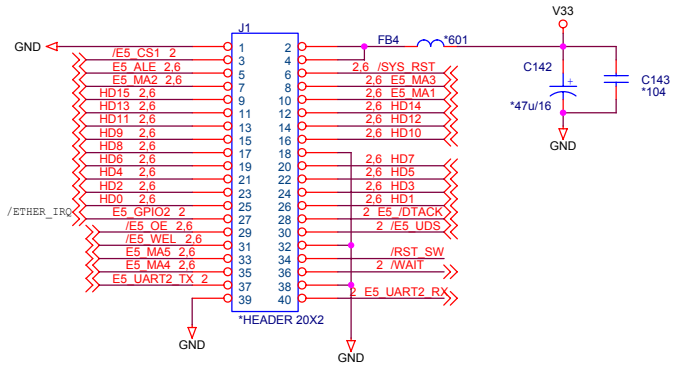


LSI LOGIC			
560 COTTONWOOD DR. MILPITAS, CA 95035 U. S. A.			
Title: TERM AT E5			
Size: C	Document Number		Rev: D0
Date: Monday, June 07, 2004	Sheet 3 of 12		

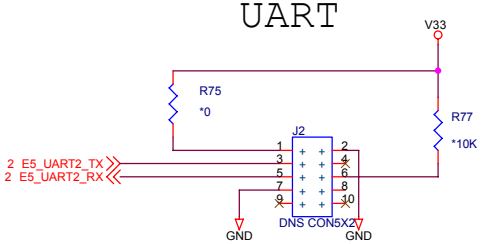


LSI LOGIC	
560 COTTONWOOD DR. MILPITAS, CA 95035 U. S. A.	
Title	2 (8M x 16) DDR SDRAM
Size: Custom	Document Number:
Rev: A1	
Date: Monday, June 07, 2004	Sheet 4 of 12

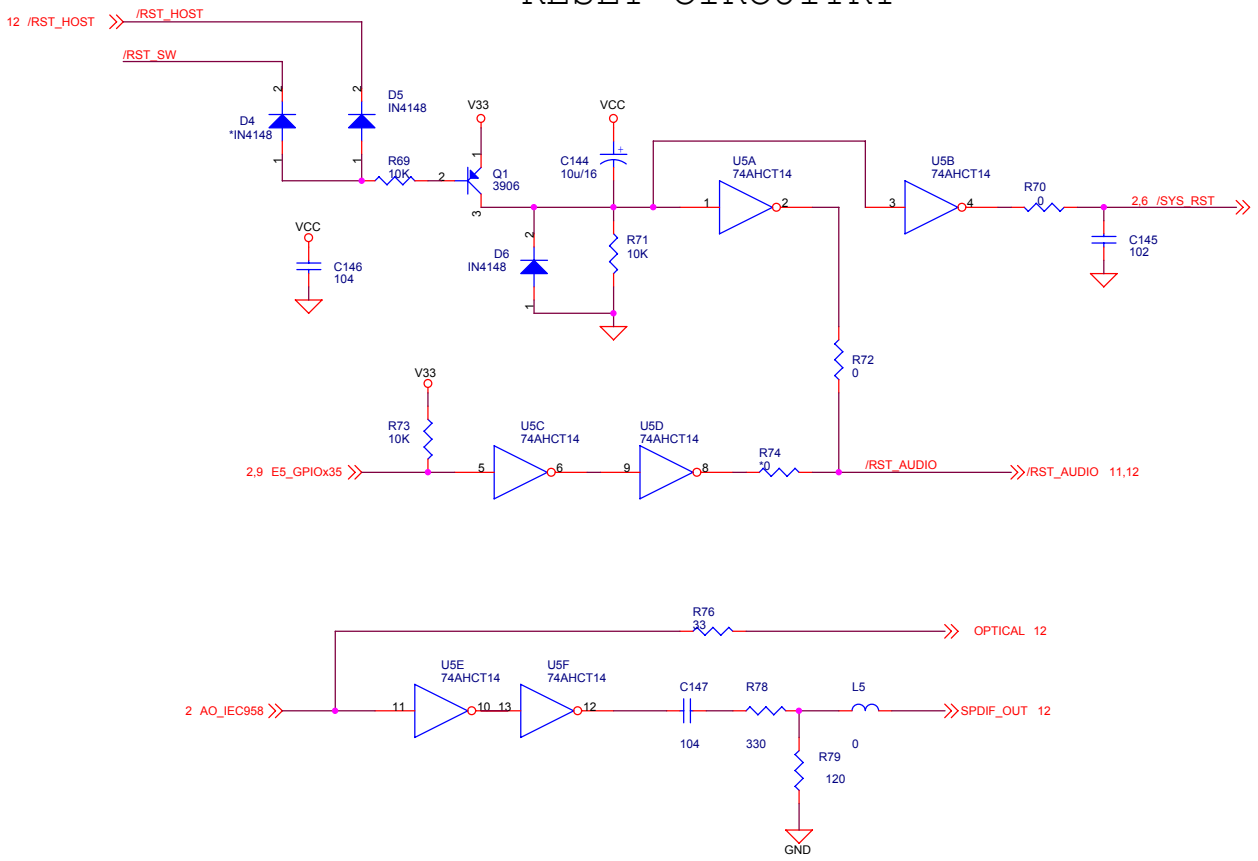
E-Link III Connector



UART

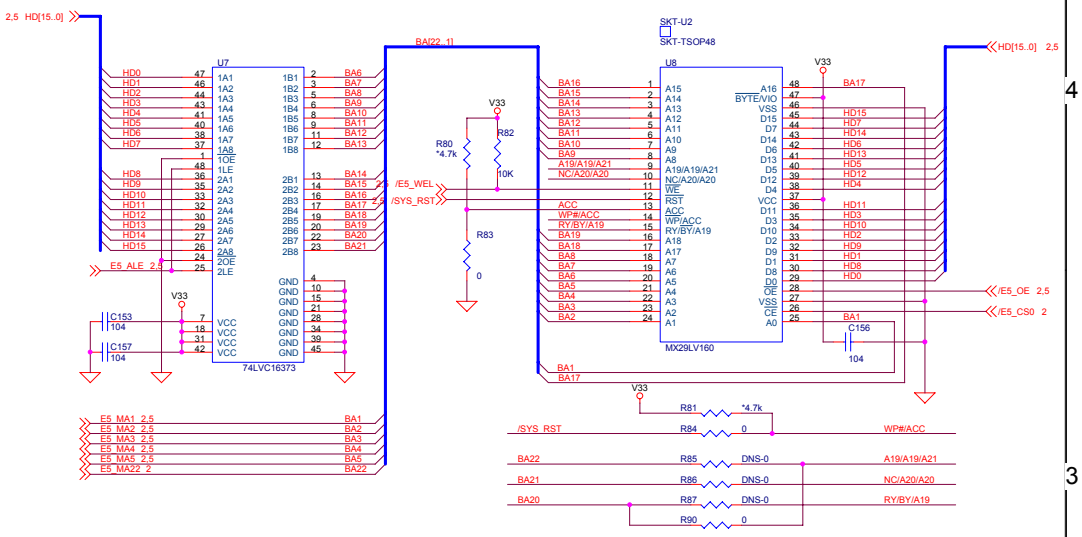


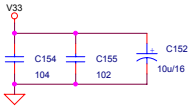
RESET CIRCUITRY

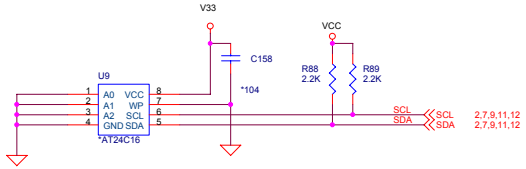


LSI LOGIC 560 COTTONWOOD DR. MILPITAS, CA 95035 U. S. A.		
Title: FP, RST, IR, AV IO/ELink-3 CON, UART		
Size: A3	Document Number	Rev: A1
Date: Monday, June 07, 2004	Sheet 5 of 12	

FLASH MEMORY(2 or 4 or 8 Mb)

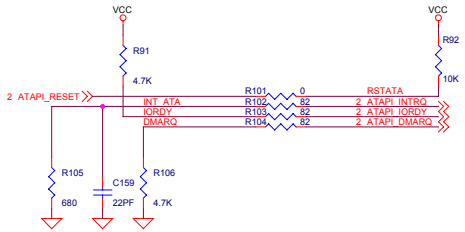


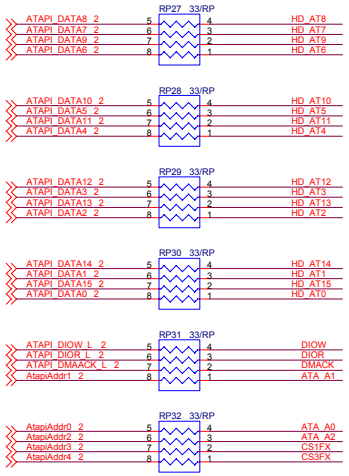




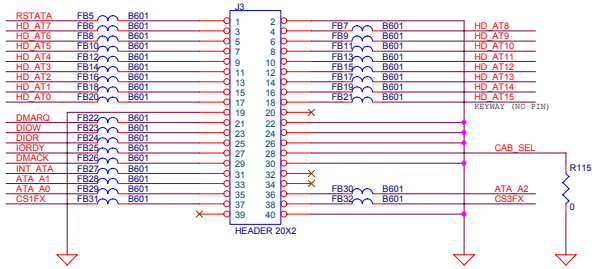
Size	Stuff	Not Stuff
1MB		R85,R86,R87,R90
2MB(Default)	R90	R85,R86,R87
4MB	R86,R90	R85,R87
8MB	R85,R86,R87	R90

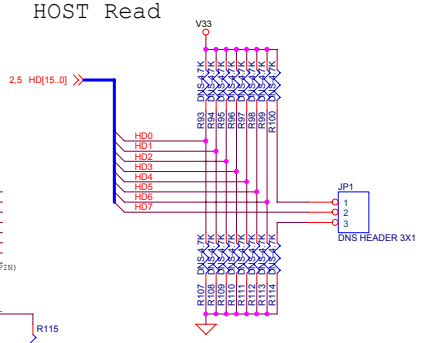
DEDICATED ATAPI INTERFACE





HOST Read





HD[1:0]	00	Samsung - K4H2816 38D-TCB3
	01	Micron - MT46V8M16-55
	10	ESMT - M13S128168A-6T
	11	Nanya
HD[3:2]	10	64Mb DDR SDRAM
	00	128Mb DDR SDRAM
	01	256Mb DDR SDRAM
	11	Reserve
HD[7]	0	Normal Mode (Jumper 1-2)
	1	Debuge Mode (Jumper 2-3)

LSI LOGIC

560 COTTONWOOD DR.
MILPITAS, CA 95035
U. S. A.

Title: FLASH, ATA, EEPROM

Size: C | Document Number | Rev: A1

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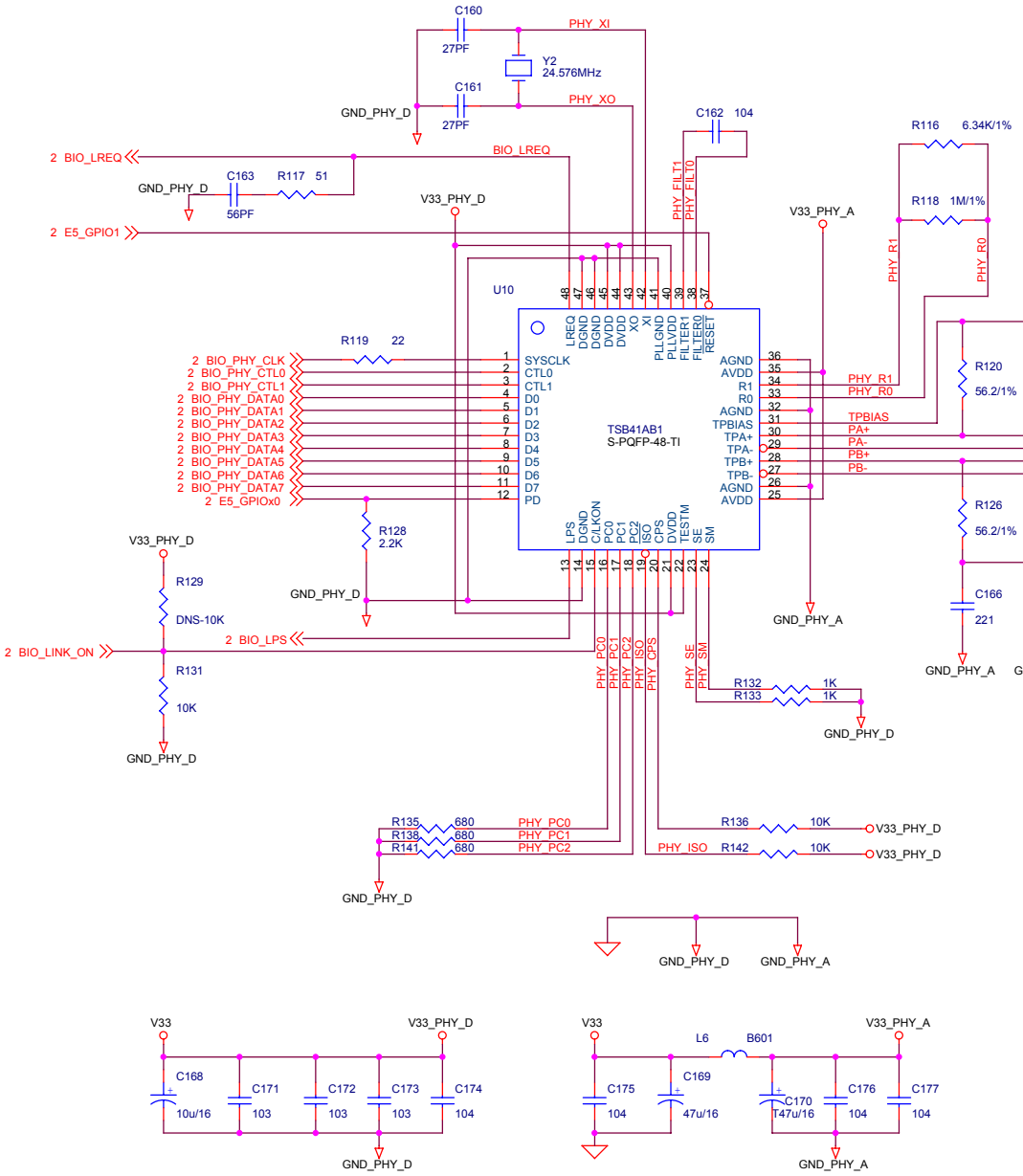
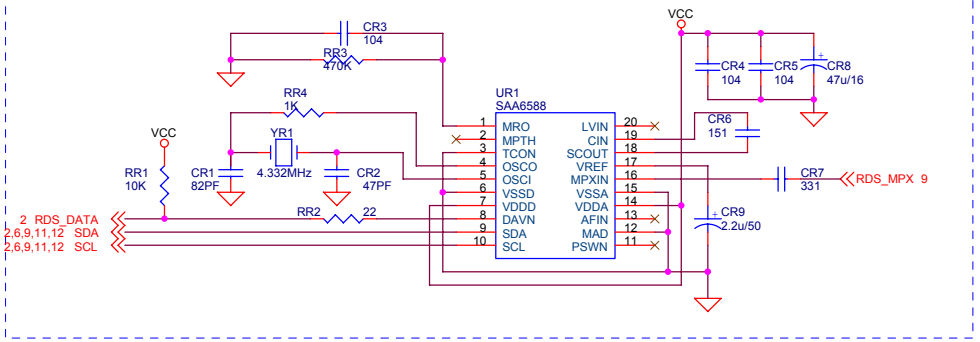
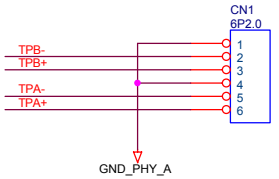
1394 FIREWIRE PHY

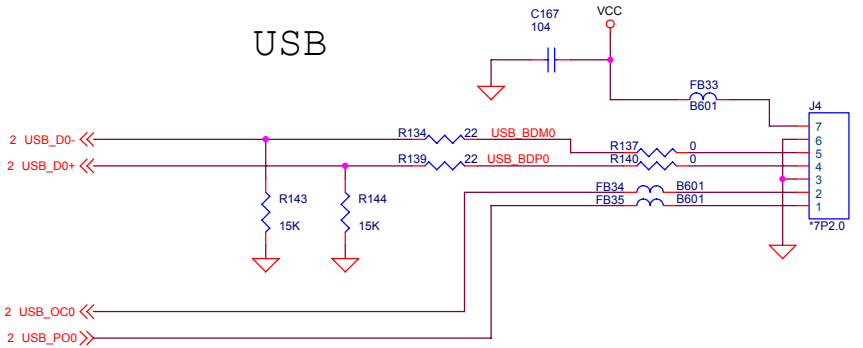


RDS /RBDS PRE-PROCESSOR





USB



LSI LOGIC	560 COTTONWOOD DR. MILPITAS, CA 95035 U. S. A.
Title	1394 PHY &USB
Size A3	Document Number
Rev A1	
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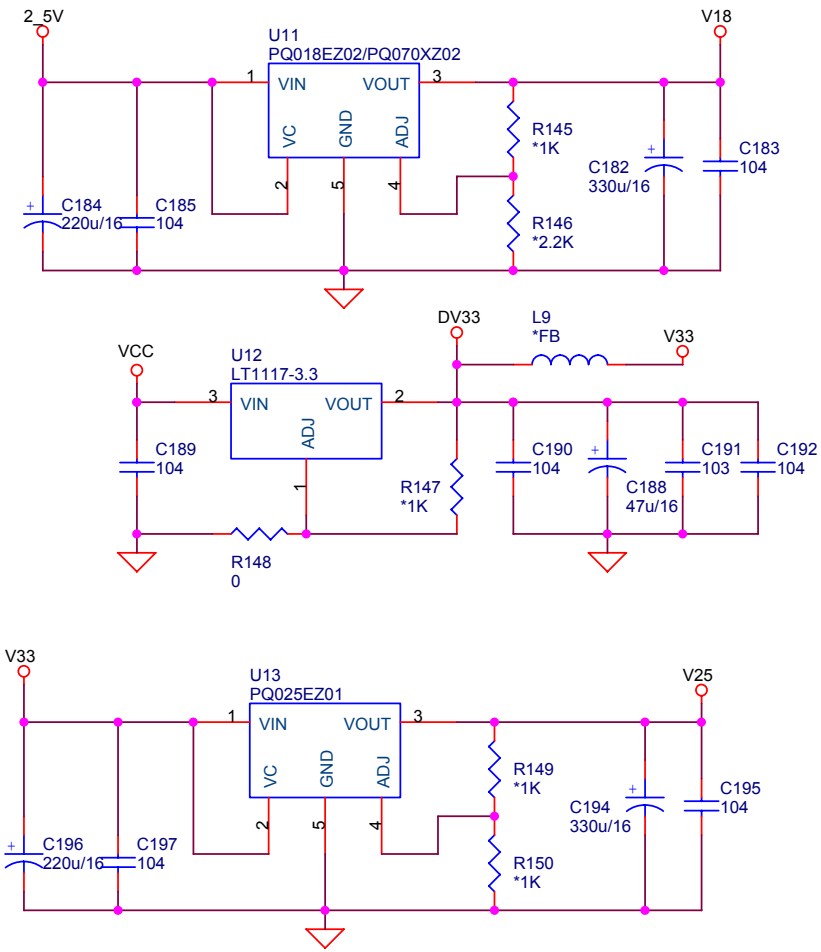
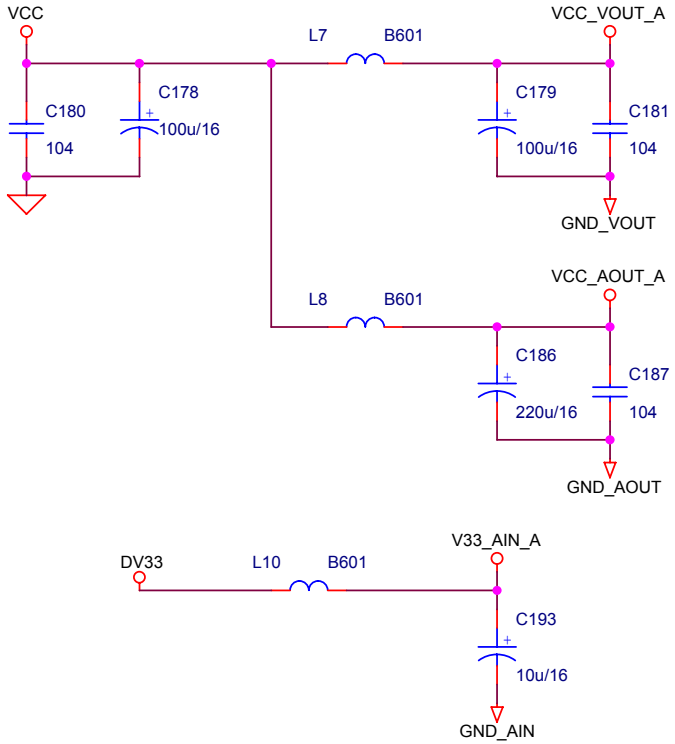
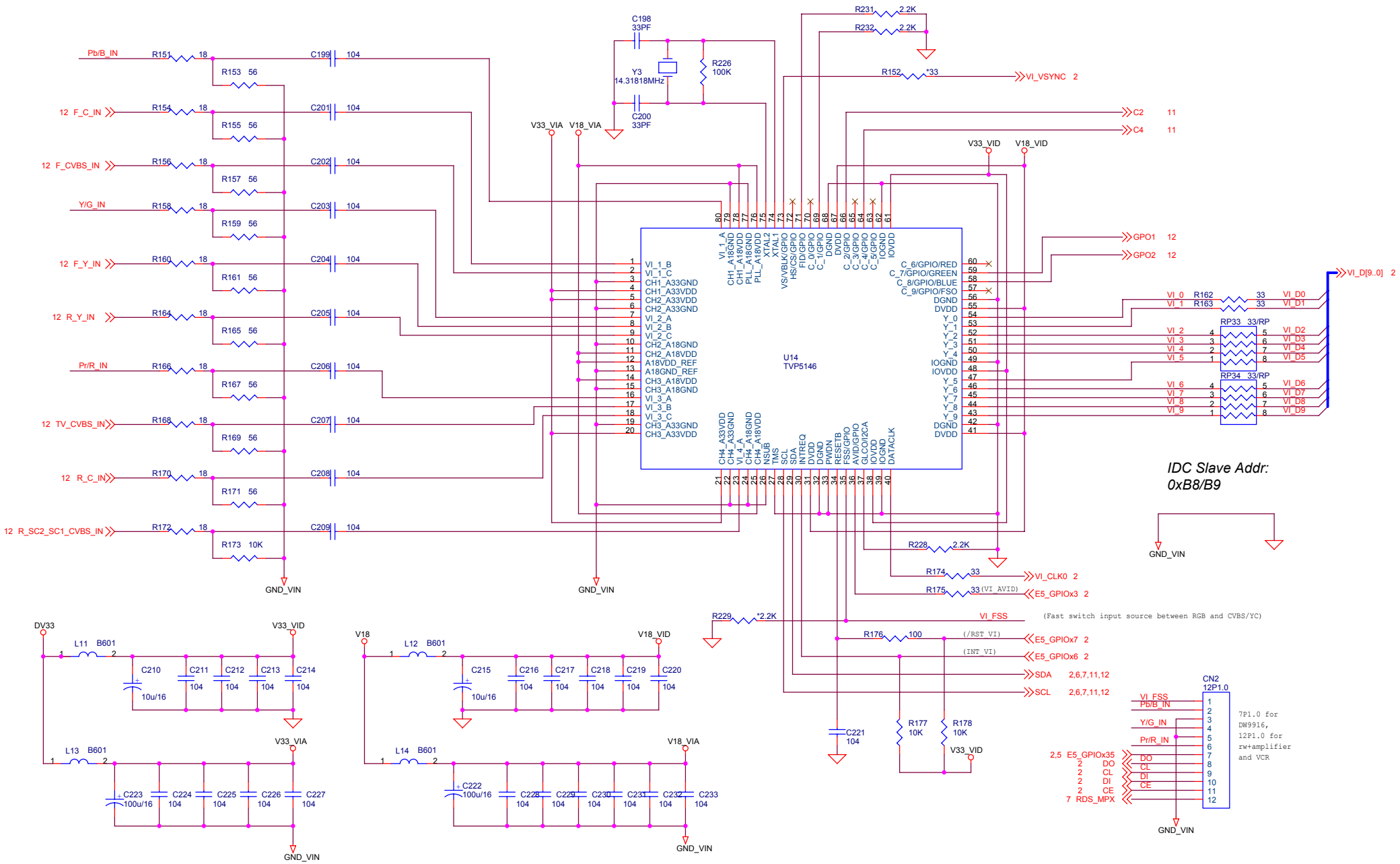
MAIN POWER REG





LSI LOGIC 560 COTTONWOOD DR. MILPITAS, CA 95035 U. S. A.		
Title: POWER CONN		
Size: A4	Document Number	Rev: A1
Date: Monday, June 07, 2004	Sheet 8 of 12	



LSI LOGIC	
560 COTTONWOOD DR. MILPITAS, CA 95035 U. S. A.	
Title	VIDEO IN
Size A3	Document Number
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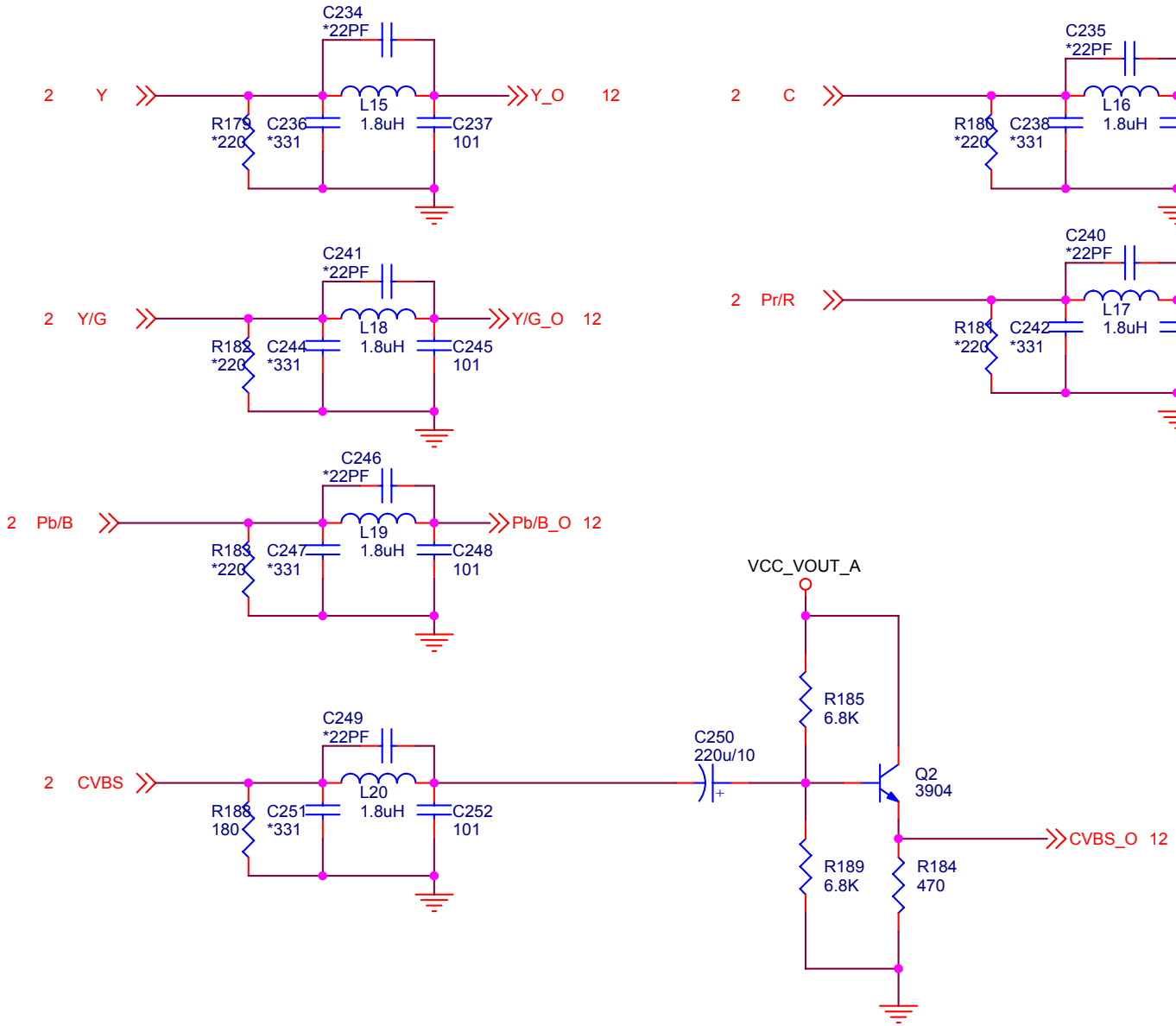
Date: Monday, June 07, 2004	Sheet 9 of 12



Title	<Title>	
Size A	Document Number <Doc>	Rev A1
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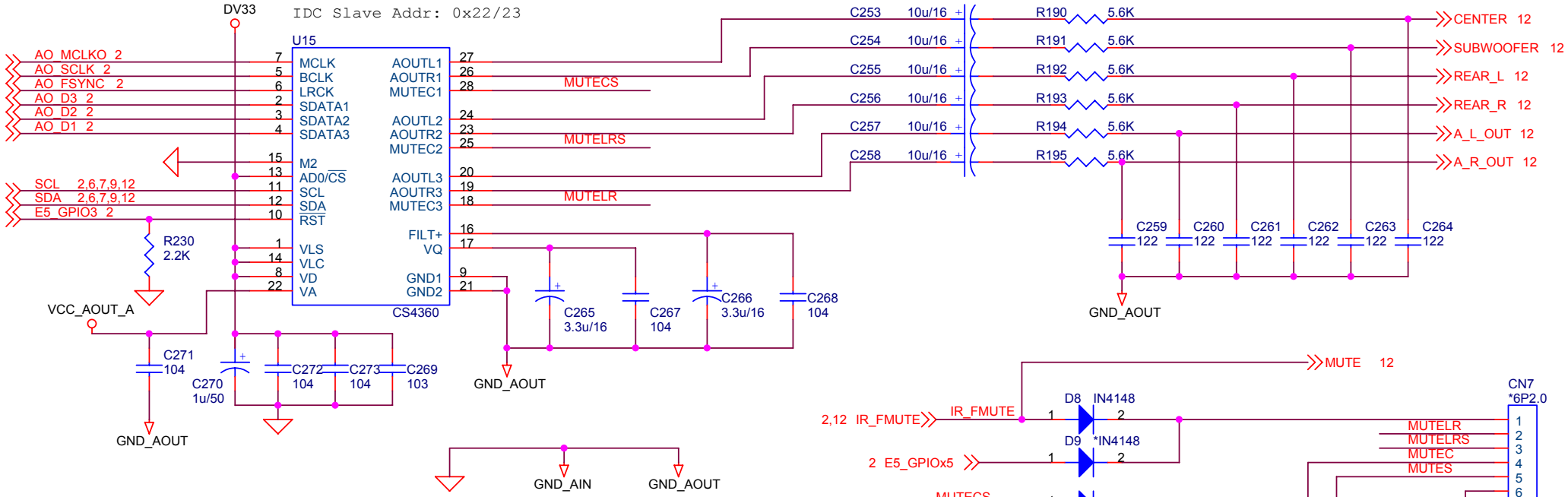
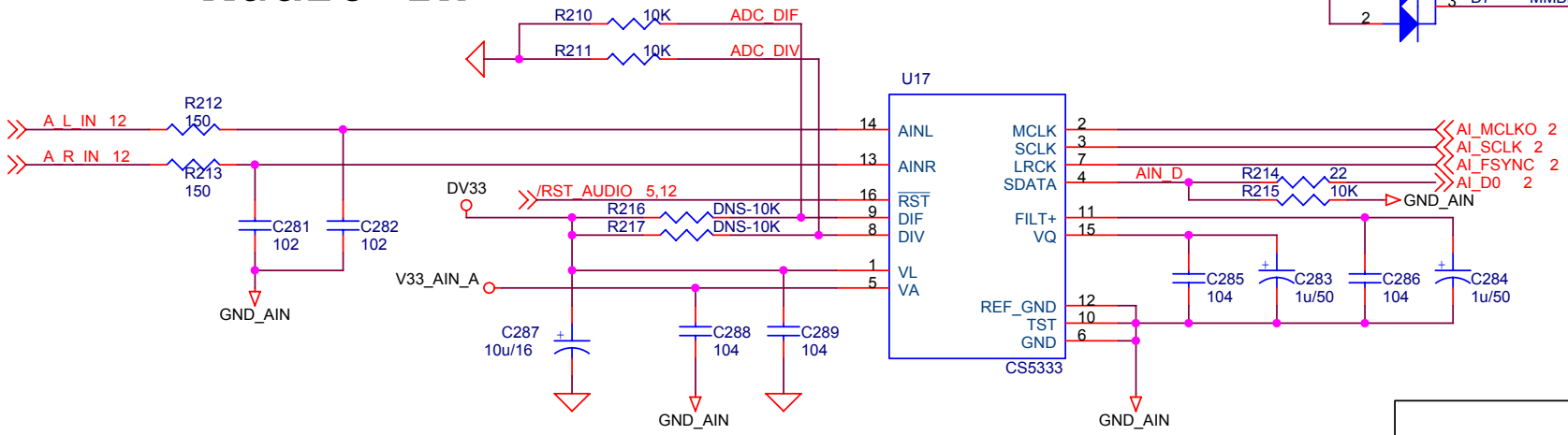
Audio Out (2 & 6 ch)



Audio In



Title <Title>		
Size A4	Document Number <Doc>	Rev <RevCode>
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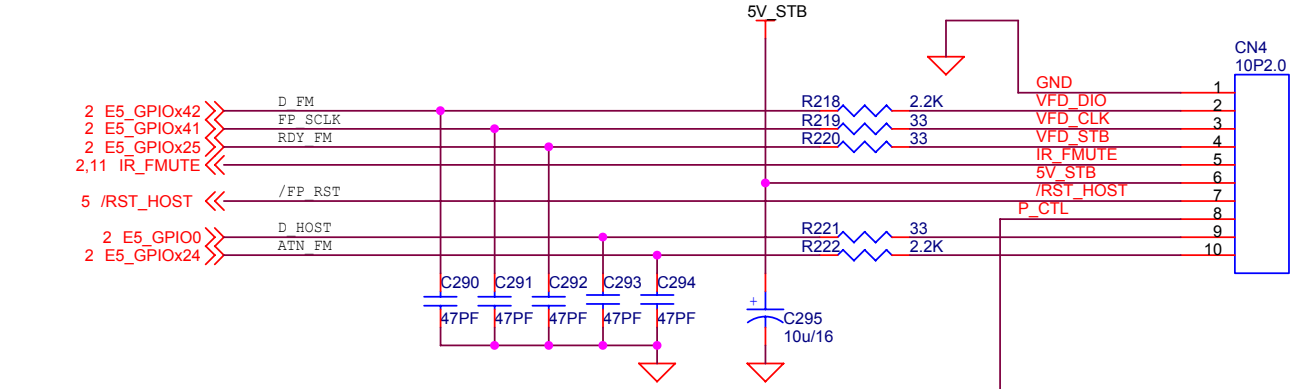
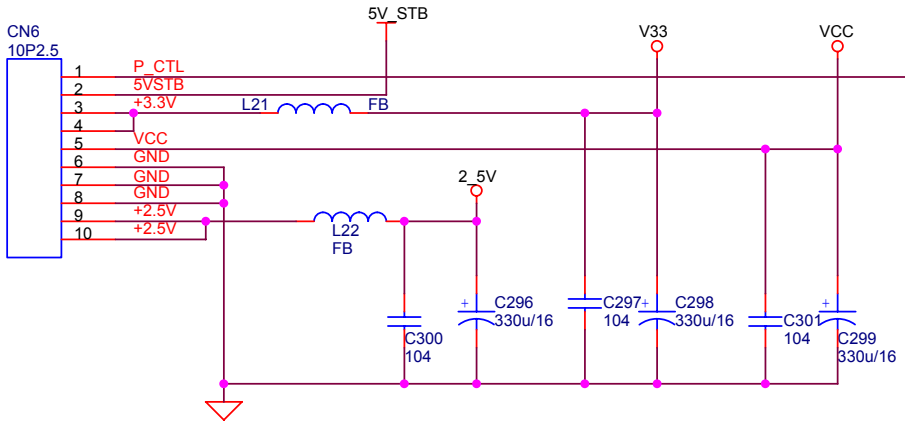
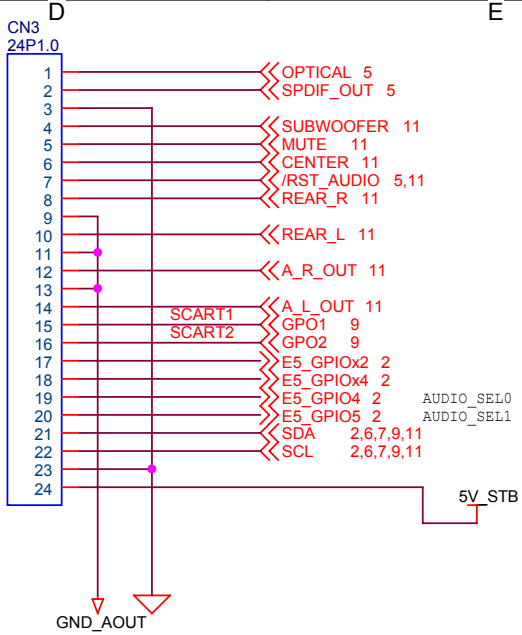
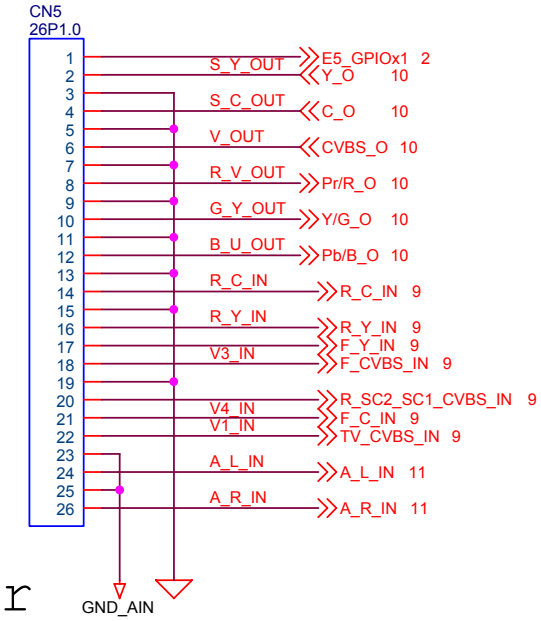
FRONT PANEL INTERFACE









A/V I/O Connector

Title <Title>		
Size Custom	Document Number <Doc>	Rev 0.0
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Modify Notes:

2005.01.08

P1 U1 Supply voltage from +6.2V to +5V

P8 Del Net E5_C

P8 Add C166,C167,C168 when in mtk scart and out scart(rgb) ,exist interference.

P7. add gcode ic

P9. add r210,r211,r213,r214 amend the sound distortion when playing vcd,stero out,connect KONGJA tv

P8 add c169,c176 amend log picture distortion

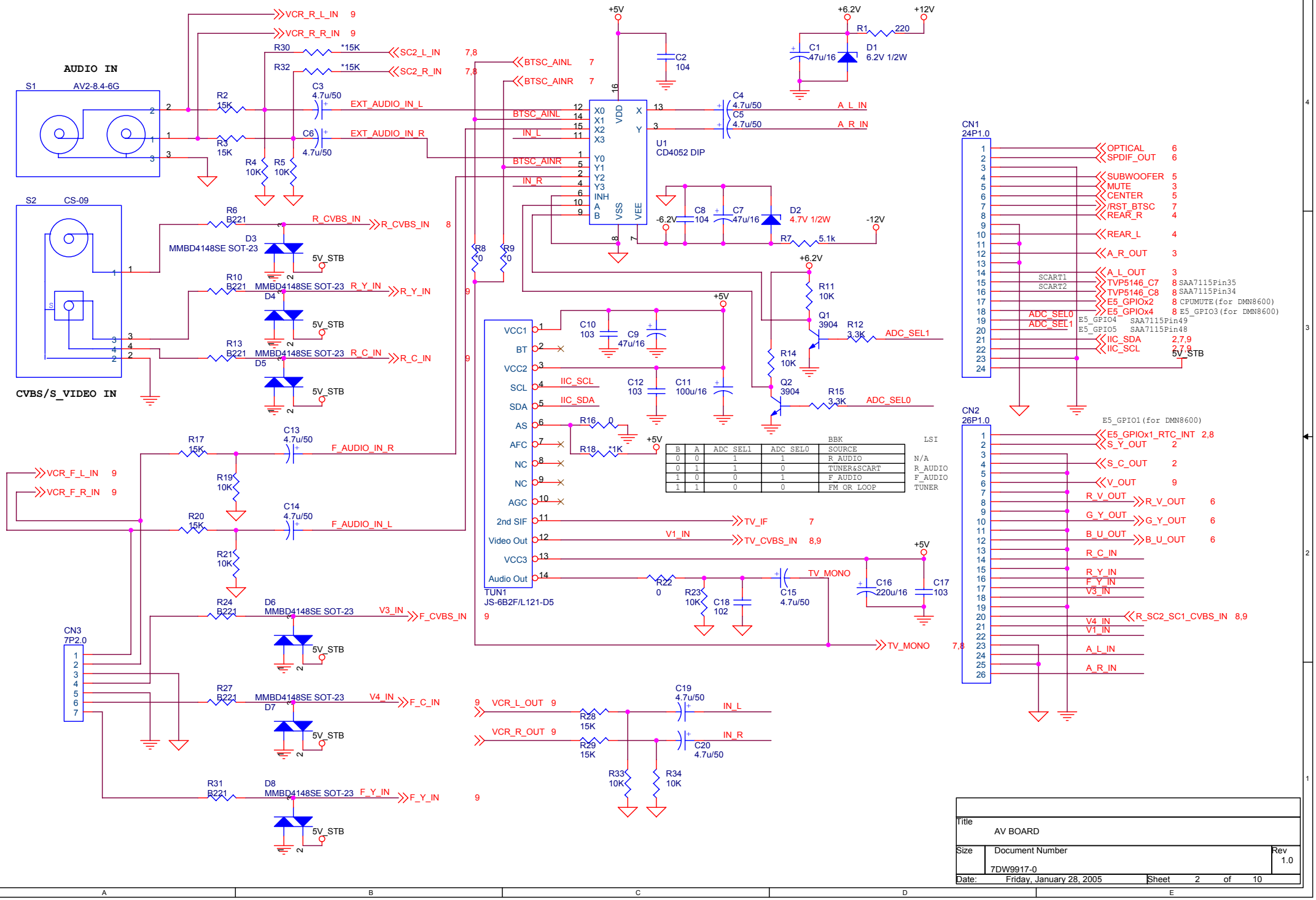
2005.01.12

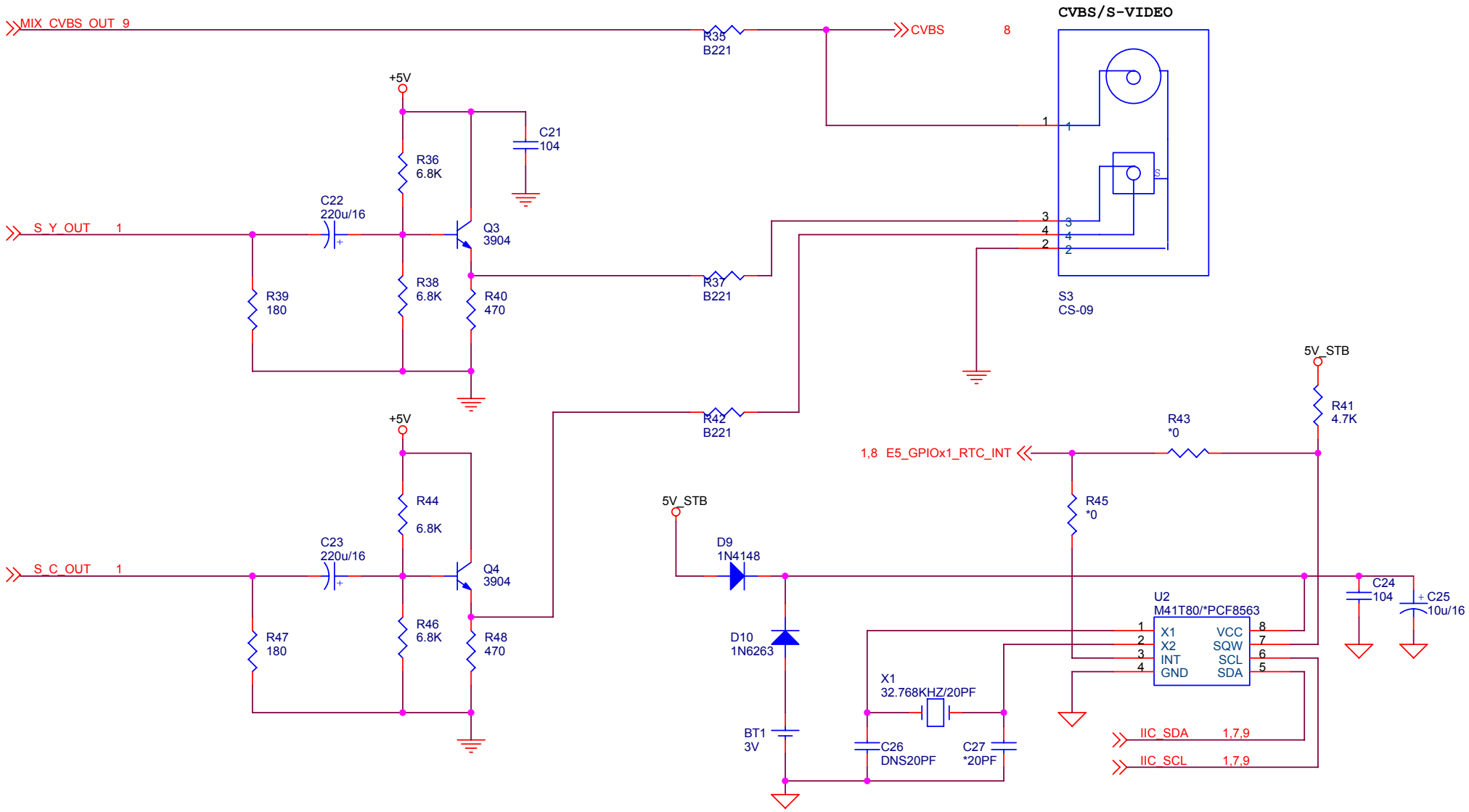
P8 add Q39,Q40,r218,r219,r220 etc. switch RGB/CVBS select votage level,when SCART in

2005.01.28

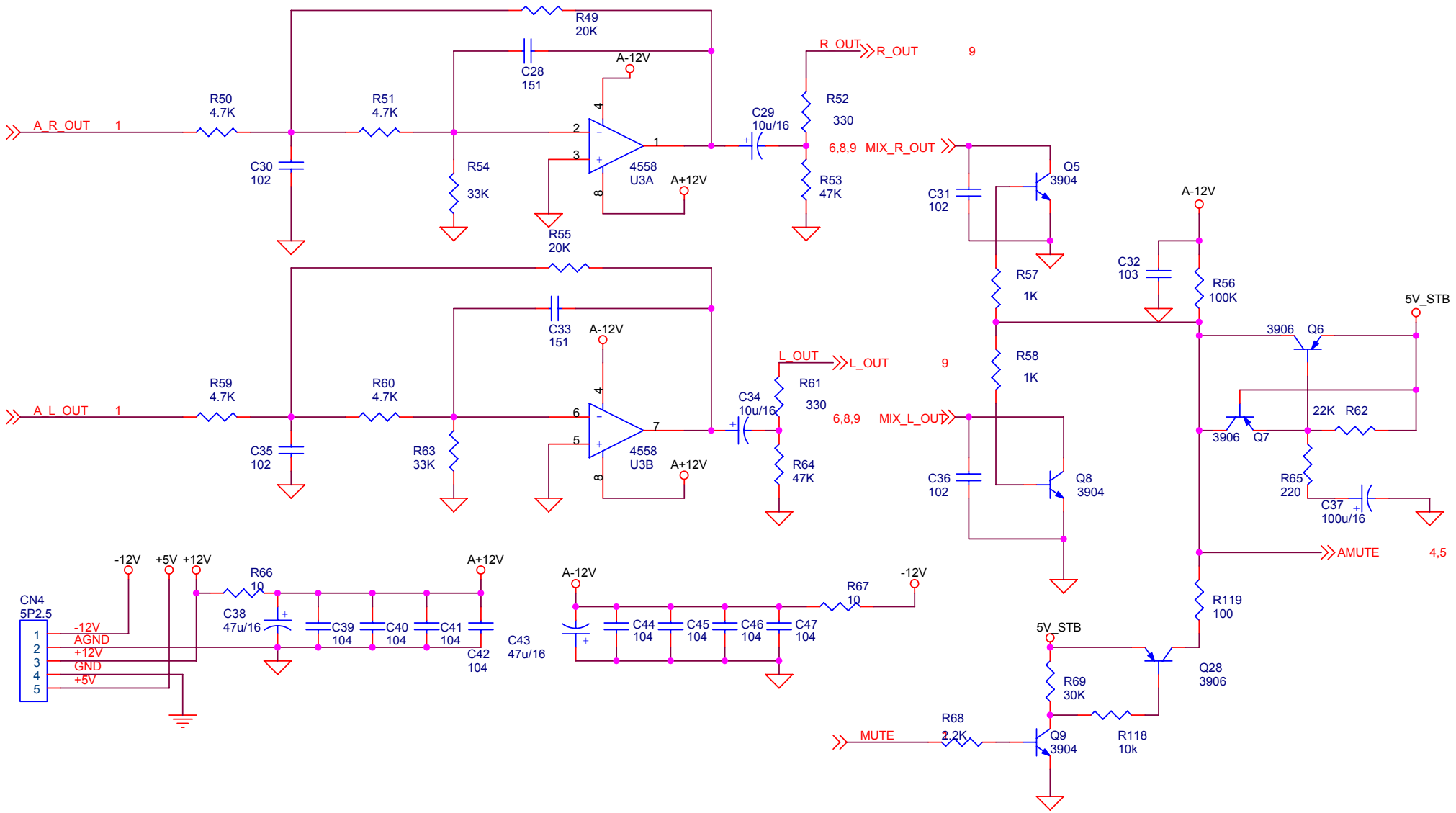
change c136,c145 to 220u

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, January 28, 2005	Sheet 1 of 10	

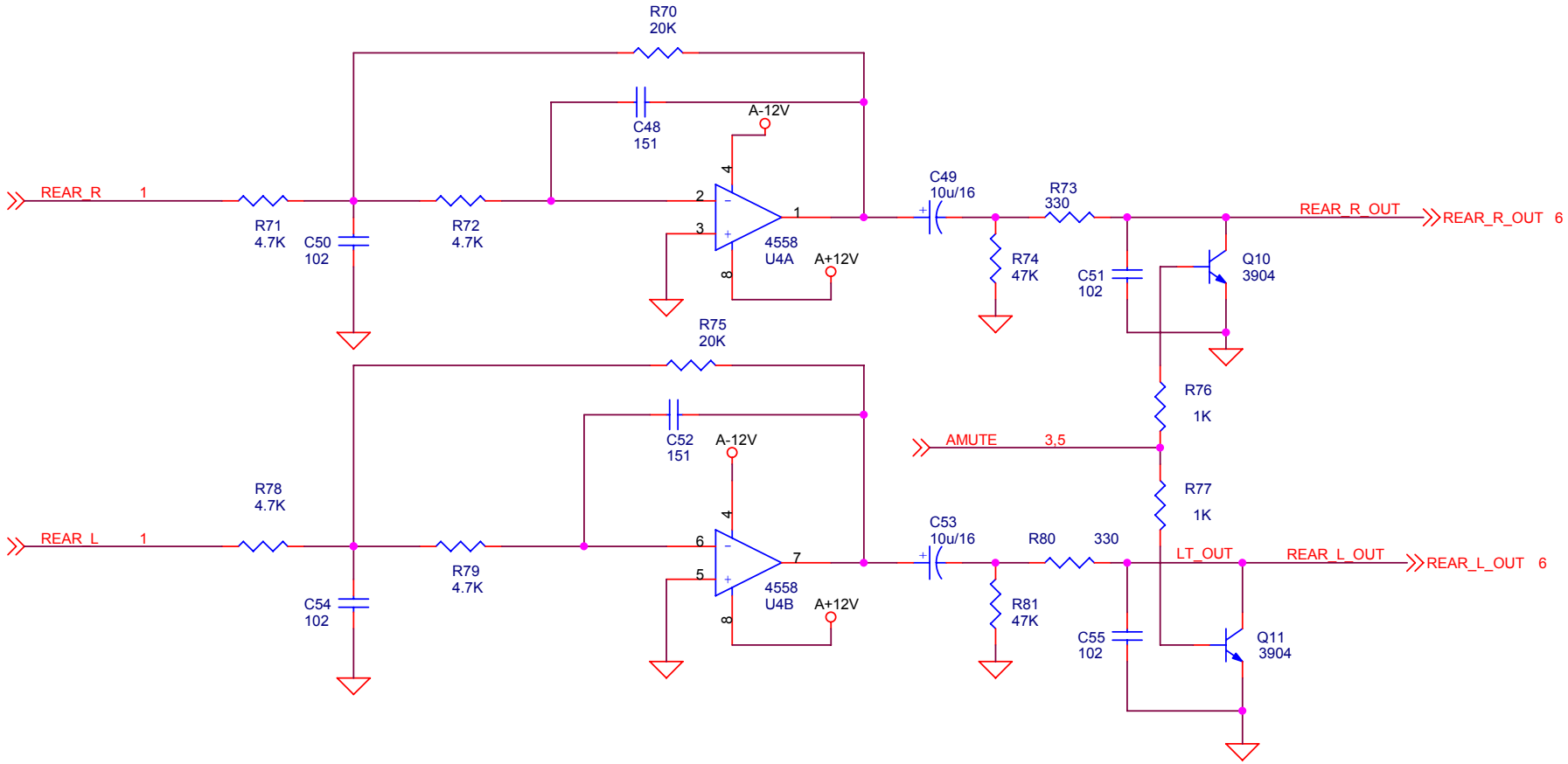

AUDIO IN
S1 AV2-8.4-6G
CVBS/S_VIDEO IN
S2 CS-09
VCR_R_L_IN 9
VCR_R_R_IN 9
SC2_L_IN 7,8
SC2_R_IN 7,8
EXT_AUDIO_IN_L
EXT_AUDIO_IN_R
R_CVBS_IN 8
R_Y_IN
R_C_IN
5V_STB
VCR_F_L_IN 9
VCR_F_R_IN 9
F_AUDIO_IN_R
F_AUDIO_IN_L
F_CVBS_IN
F_C_IN
F_Y_IN
V3_IN
V4_IN
CN3 7P2.0
BTSC_AINL 7
BTSC_AINR 7
IN_L
IN_R
U1 CD4052 DIP
A_L_IN
A_R_IN
+5V
+6.2V
+12V
-6.2V
-12V
D1 6.2V 1/2W
D2 4.7V 1/2W
R7 5.1k
R11 10K
Q1 3904
Q2 3904
R12 3.3K
R15 3.3K
ADC_SEL1
ADC_SEL0
IIC_SCL
IIC_SDA
TUN1 JS-6B2F/L121-D5
VCC1
BT
VCC2
SCL
SDA
AS
AFC
NC
NC
AGC
2nd SIF
Video Out
VCC3
Audio Out
TV_IF 7
V1_IN
TV_CVBS_IN 8,9
TV_MONO
TV_MONO 7,8
BBK LSI
B A ADC_SEL1 ADC_SEL0 SOURCE
0 0 1 1 R_AUDIO N/A
0 1 1 0 TUNER&SCART R_AUDIO
1 0 0 1 F_AUDIO F_AUDIO
1 1 0 0 FM_OR_LOOP TUNER
VCR_L_OUT 9
VCR_R_OUT 9
CN1 24P1.0
OPTICAL 6
SPDIF_OUT 6
SUBWOOFER 5
MUTE 3
CENTER 5
/RST_BTSC 7
REAR_R 4
REAR_L 4
A_R_OUT 3
A_L_OUT 3
SCART1
SCART2
TVP5146_C7 8 SAA7115Pin35
TVP5146_C8 8 SAA7115Pin34
E5_GPIOx2 8 CPUMUTE(for DMN8600)
E5_GPIOx4 8 E5_GPIO3(for DMN8600)
E5_GPIO4 SAA7115Pin49
E5_GPIO5 SAA7115Pin48
IIC_SDA 2,7,9
IIC_SCL 2,7,9
CN2 26P1.0
E5_GPIO1(for DMN8600)
E5_GPIOx1_RTC_INT 2,8
S_Y_OUT 2
S_C_OUT 2
V_OUT 9
R_V_OUT 6
G_Y_OUT 6
B_U_OUT 6
R_C_IN
R_Y_IN
F_Y_IN
V3_IN
R_SC2_SC1_CVBS_IN 8,9
V4_IN
V1_IN
A_L_IN
A_R_IN
Title AV BOARD
Size Document Number 7DW9917-0 Rev 1.0
Date: Friday, January 28, 2005 Sheet 2 of 10



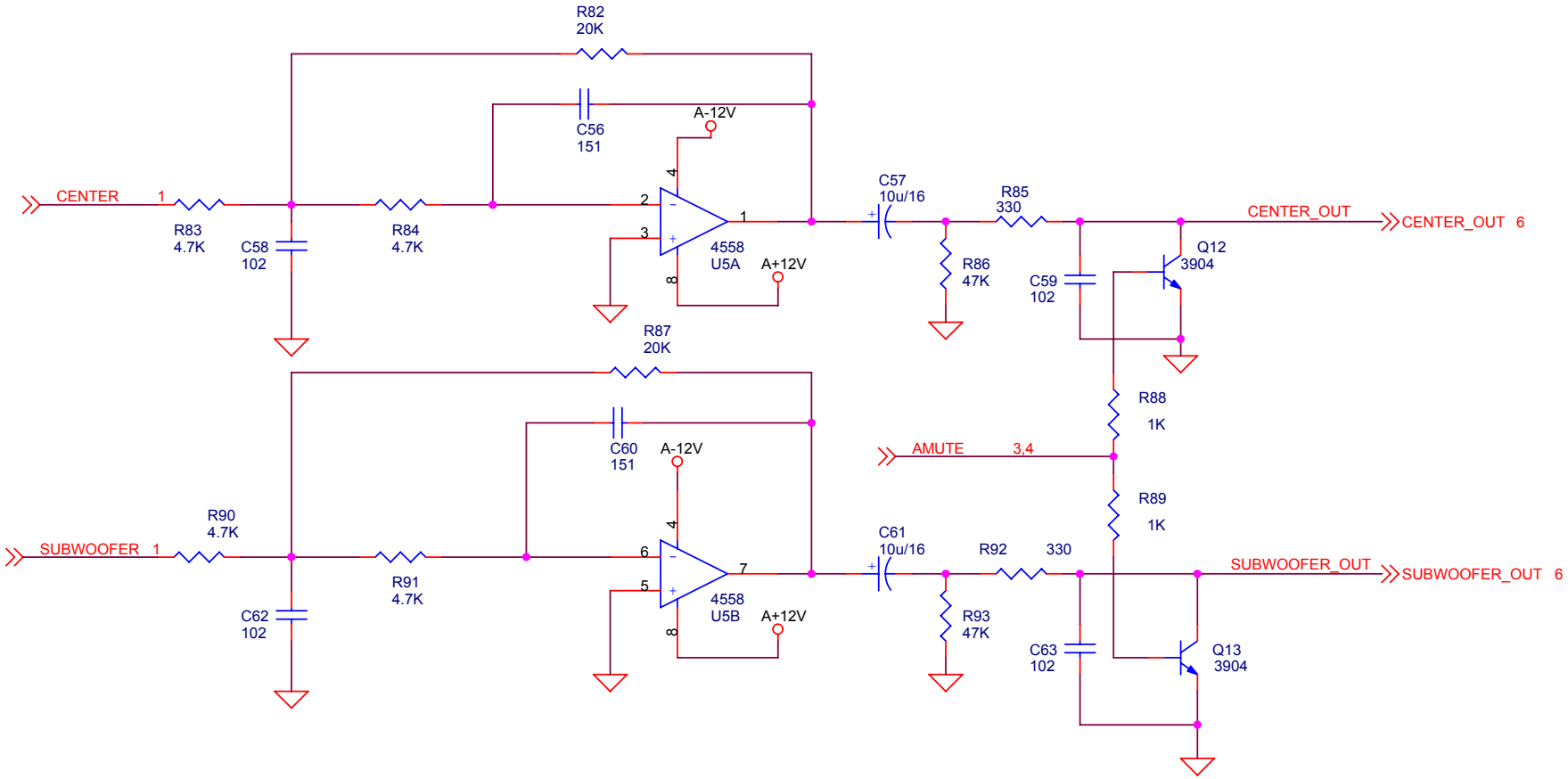
Title	<Title>	
Size A4	Document Number <Doc>	Rev 1.0
Date: Friday, January 28, 2005	Sheet 3 of 10	



Title <Title>		
Size A4	Document Number <Doc>	Rev 1.0
Date: Friday, January 28, 2005	Sheet 4 of 10	



Title <Title>		
Size A4	Document Number <Doc>	Rev 1.0
Date: Friday, January 28, 2005	Sheet 5 of 10	



Title	<Title>	
Size A4	Document Number <Doc>	Rev 1.0
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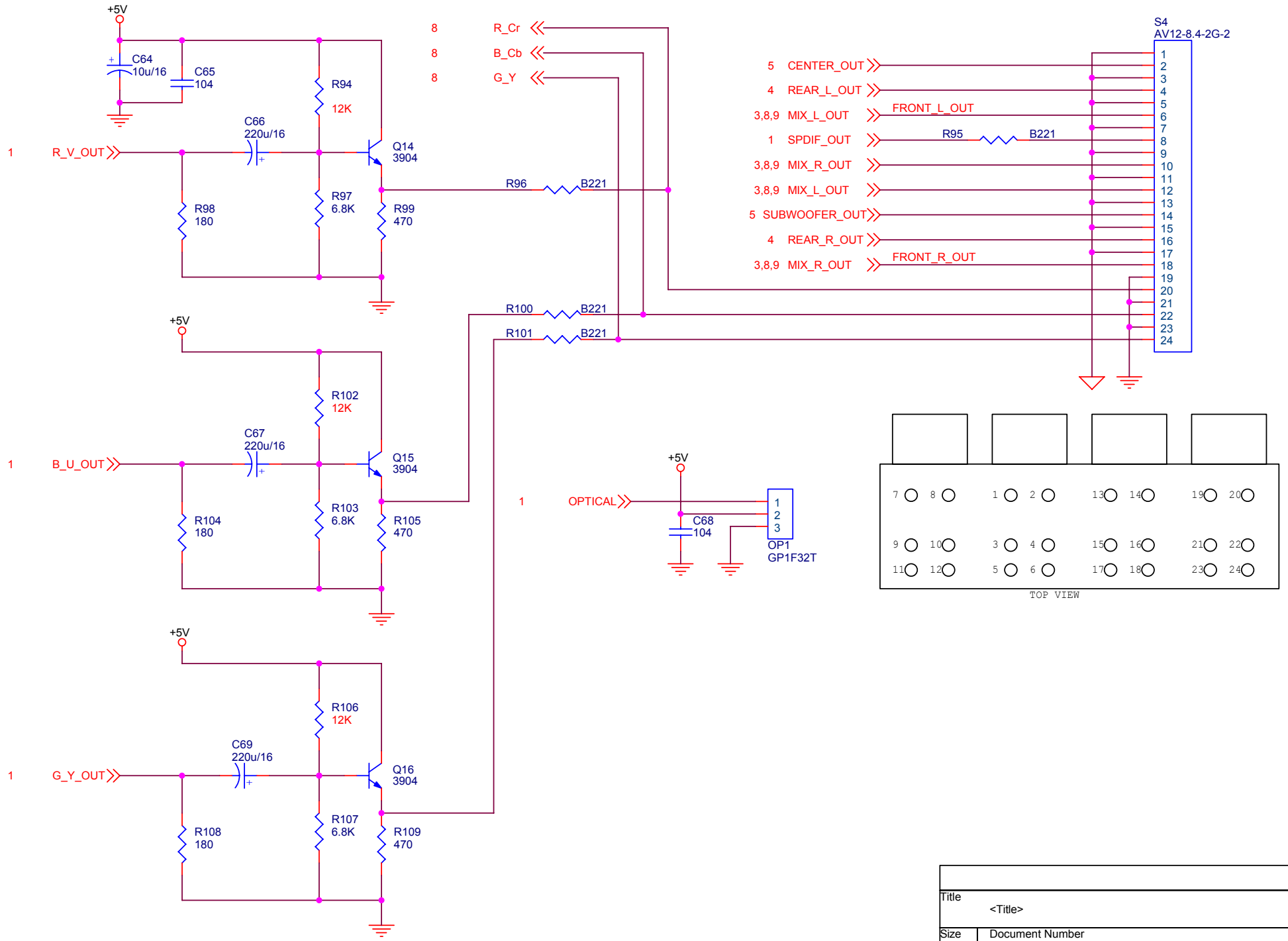
+5V
C64
10u/16
C65
104
R94
12K
C66
220u/16
1
R_V_OUT
Q14
3904
R98
180
R97
6.8K
R99
470
8
R_Cr
8
B_Cb
8
G_Y
R96
B221
R100
B221
R101
B221
S4
AV12-8.4-2G-2
5 CENTER_OUT
4 REAR_L_OUT
3,8,9 MIX_L_OUT
FRONT_L_OUT
1 SPDIF_OUT
R95
B221
3,8,9 MIX_R_OUT
3,8,9 MIX_L_OUT
5 SUBWOOFER_OUT
4 REAR_R_OUT
3,8,9 MIX_R_OUT
FRONT_R_OUT
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
+5V
R102
12K
C67
220u/16
1
B_U_OUT
Q15
3904
R104
180
R103
6.8K
R105
470
+5V
R106
12K
C69
220u/16
1
G_Y_OUT
Q16
3904
R108
180
R107
6.8K
R109
470
+5V
1
OPTICAL
C68
104
1
2
3
OP1
GP1F32T
7 8 1 2 13 14 19 20
9 10 3 4 15 16 21 22
11 12 5 6 17 18 23 24
TOP VIEW
Title
<Title>
Size
A4
Document Number
Rev
1.0
Date:
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7
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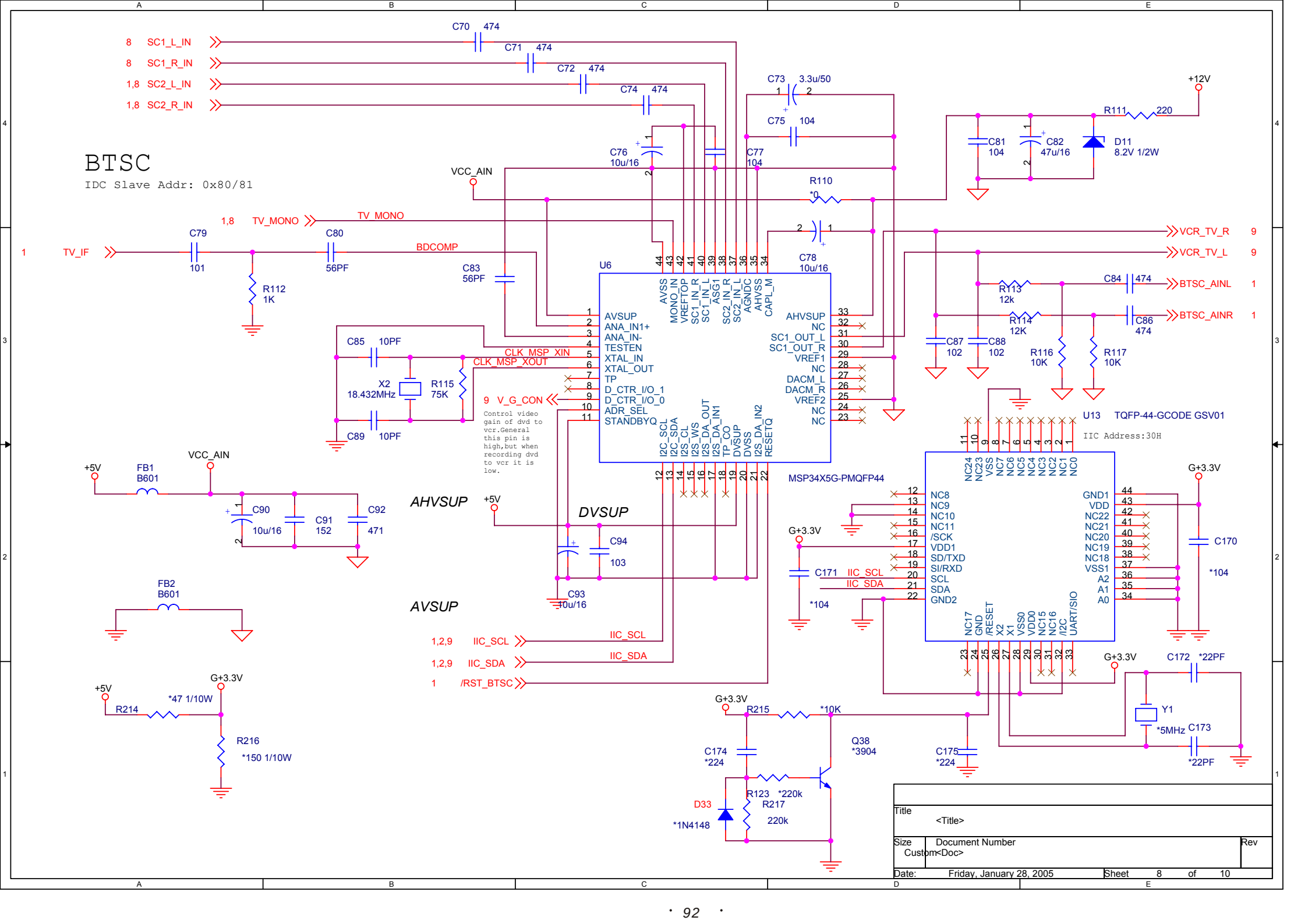
10


BTSC
IDC Slave Addr: 0x80/81
8 SC1_L_IN
8 SC1_R_IN
1,8 SC2_L_IN
1,8 SC2_R_IN
C70 474
C71 474
C72 474
C74 474
C73 3.3u/50
C75 104
C76 10u/16
C77 104
VCC_AIN
R110 *0
+12V
R111 220
C81 104
C82 47u/16
D11 8.2V 1/2W
1,8 TV_MONO
TV_MONO
1 TV_IF
C79 101
C80 56PF
BDCOMP
R112 1K
C83 56PF
U6
C78 10u/16
AVSUP
ANA_IN1+
ANA_IN-
TESTEN
XTAL_IN
XTAL_OUT
TP
D_CTR_I/O_1
D_CTR_I/O_0
ADR_SEL
STANDBYQ
AHVSUP
NC
SC1_OUT_L
SC1_OUT_R
VREF1
NC
DACM_L
DACM_R
VREF2
NC
NC
VCR_TV_R 9
VCR_TV_L 9
BTSC_AINL 1
BTSC_AINR 1
C84 474
C86 474
R113 12k
R114 12K
C87 102
C88 102
R116 10K
R117 10K
C85 10PF
C89 10PF
X2 18.432MHz
R115 75K
CLK_MSP_XIN
CLK_MSP_XOUT
9 V_G_CON
Control video gain of dvd to vcr.General this pin is high,but when recording dvd to vcr it is low.
U13 TQFP-44-GCODE GSV01
IIC Address:30H
MSP34X5G-PMQFP44
+5V
FB1 B601
VCC_AIN
C90 10u/16
C91 152
C92 471
AHVSUP
DVSUP
C94 103
C93 10u/16
AVSUP
FB2 B601
G+3.3V
C170 *104
C171 *104
IIC_SCL
IIC_SDA
1,2,9 IIC_SCL
1,2,9 IIC_SDA
1 /RST_BTSC
C172 *22PF
Y1 *5MHz
C173 *22PF
C175 *224
R214 *47 1/10W
R216 *150 1/10W
R215 *10K
C174 *224
Q38 *3904
D33 *1N4148
R123 *220k
R217 220k
Title <Title>
Size Custom
Document Number <Doc>
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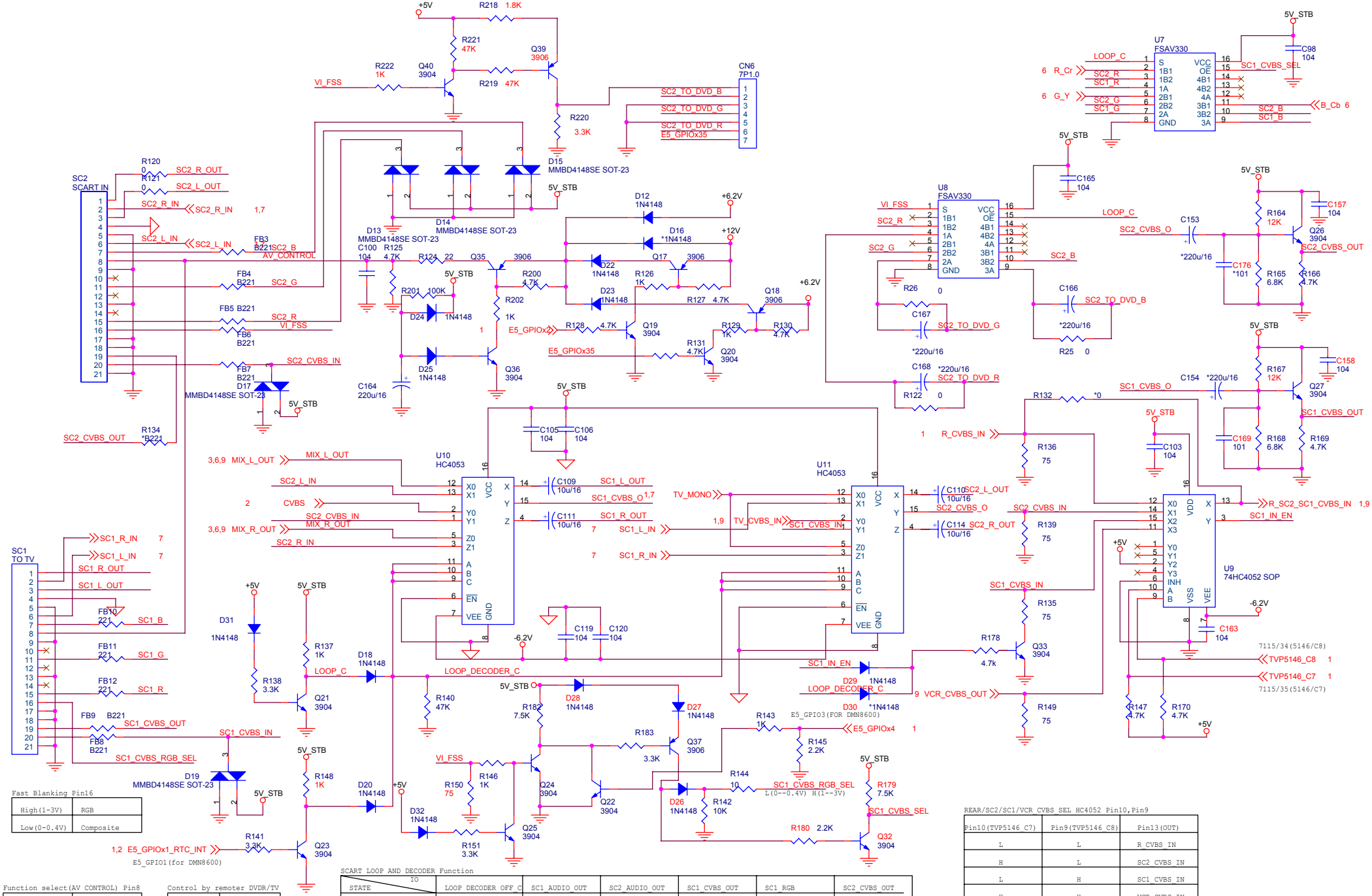

Fast Blanking Pin16

High(1~3V)	RGB
Low(0~0.4V)	Composite

Function select(AV CONTROL) Pin8

High(9.5~12V)	AV mode
Mid(5~8V)	Wide-screen
Low(0~2V)	TV mode

Control by remoter DVDR/TV

E5_GPIOx1	SC1_CVBS_OUT
L	DECODER
H	DVD RW

SCART LOOP AND DECODER Function

STATE \ IO	LOOP DECODER OFF_C	SC1_AUDIO_OUT	SC2_AUDIO_OUT	SC1_CVBS_OUT	SC1_RGB	SC2_CVBS_OUT
STANDBY/DECODER OFF	H	SC2_AUDIO_IN	SC1_AUDIO_IN	SC2_CVBS_IN	SC2_RGB	SC1_CVBS_IN
POWER ON/DECODER ON	L	RW_AUDIO_OUT	SC1_AUDIO_IN	RW_CVBS_OUT	RW_RGB_OUT	TUNER_CVBS_IN
POWER ON/DECODER OFF	H	SC2_AUDIO_IN	SC1_AUDIO_IN	SC2_CVBS_IN	RW_RGB_OUT	SC1_CVBS_IN

REAR/SC2/SC1/VCR_CVBS_SEL HC4052 Pin10,Pin9

Pin10(TVP5146_C7)	Pin9(TVP5146_C8)	Pin13(OUT)
L	L	R_CVBS_IN
H	L	SC2_CVBS_IN
L	H	SC1_CVBS_IN
H	H	VCR_CVBS_IN

Title	<Title>		
Size A3	Document Number <Doc>	<RevCode>	Rev
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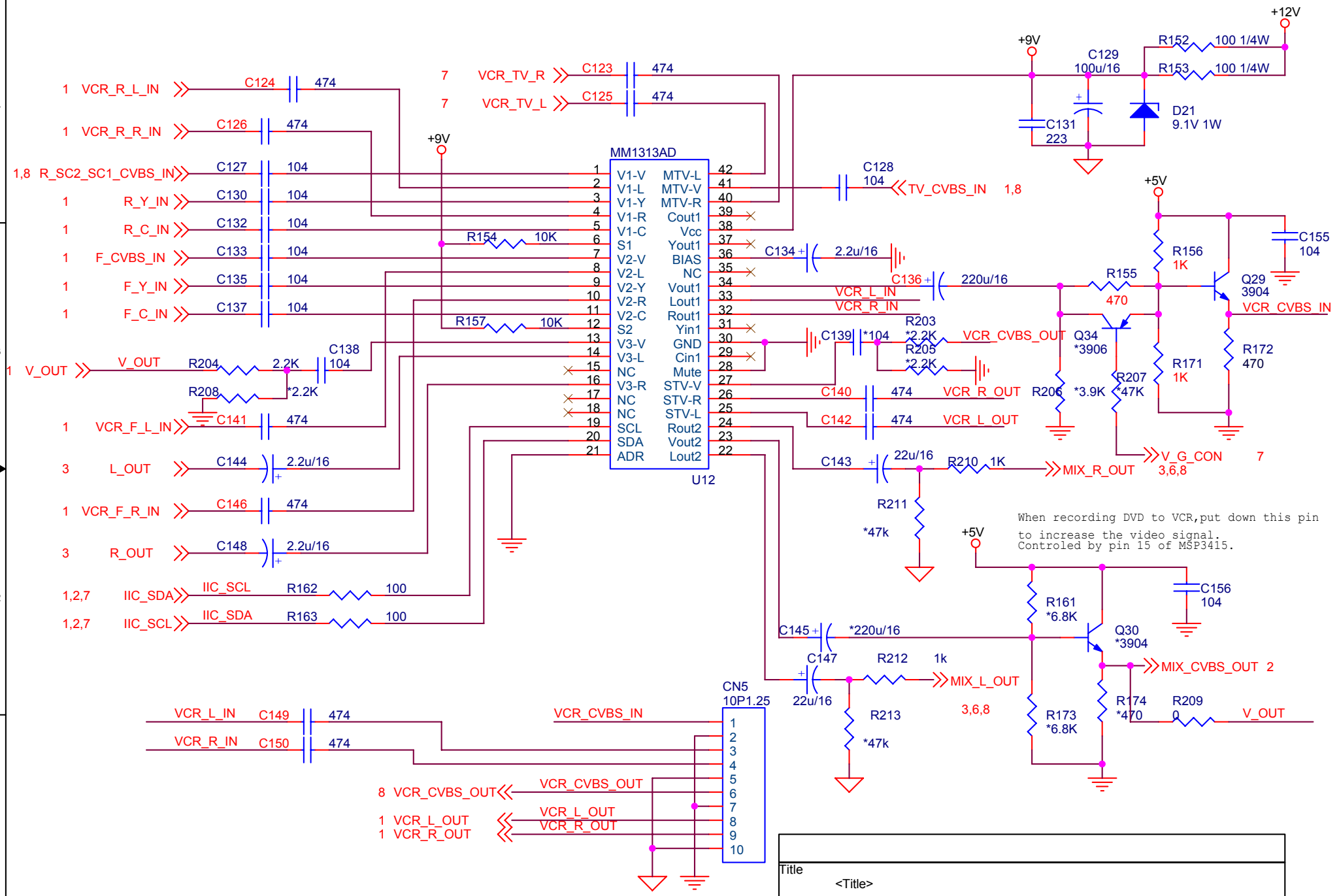
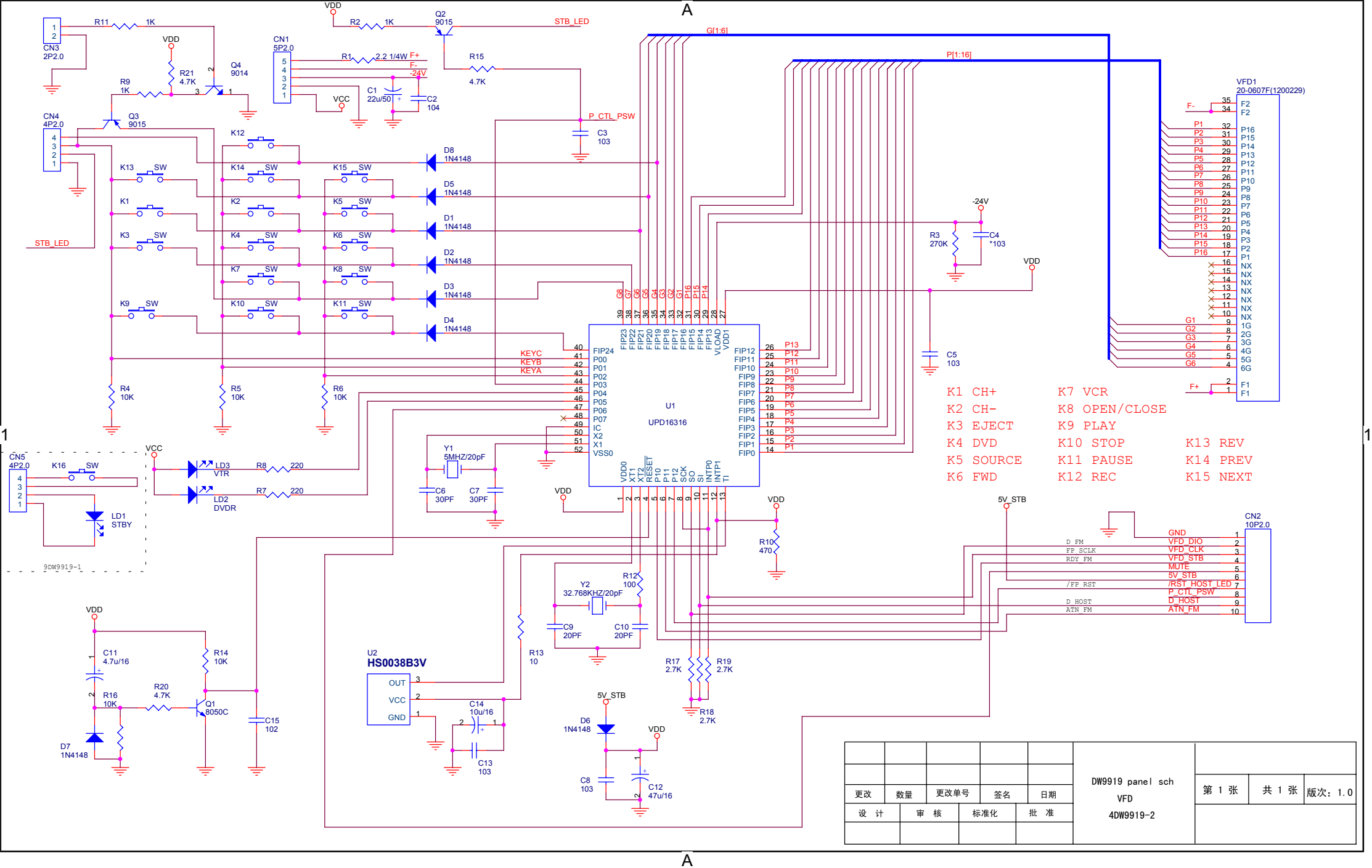
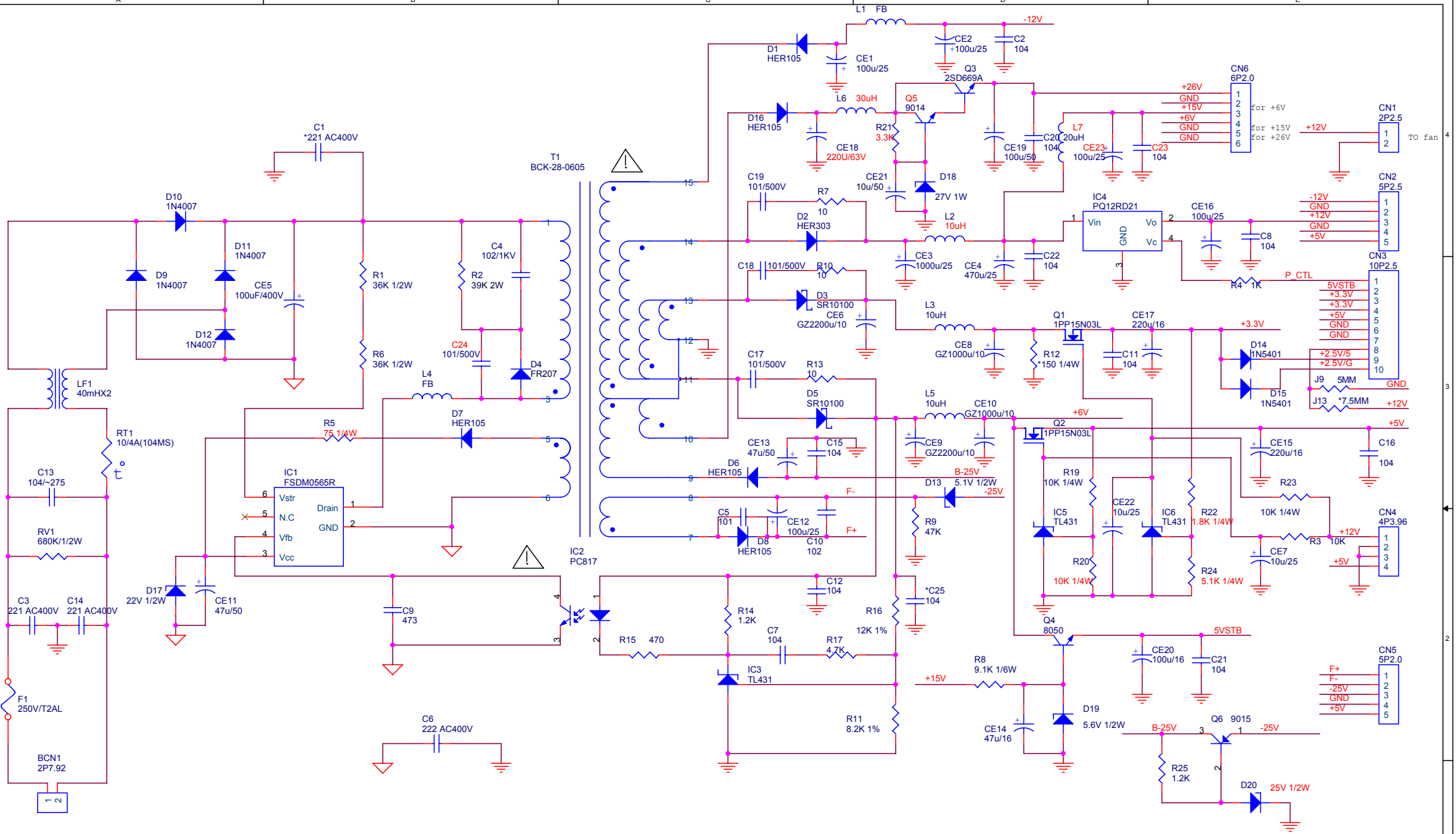

MM1313AD
U12
+12V
+9V
+5V
C129 100u/16
R152 100 1/4W
R153 100 1/4W
D21 9.1V 1W
C131 223
C128 104
TV_CVBS_IN 1,8
C123 474
C125 474
VCR_TV_R
VCR_TV_L
C124 474
C126 474
C127 104
C130 104
C132 104
C133 104
C135 104
C137 104
R154 10K
R157 10K
C134 2.2u/16
C136 220u/16
VCR_L_IN
VCR_R_IN
R155 470
R156 1K
Q29 3904
C155 104
VCR_CVBS_IN
R171 1K
R172 470
Q34 *3906
R207 *47K
R206 *3.9K
C139 *104
R203 *2.2K
R205 *2.2K
VCR_CVBS_OUT
C140 474
VCR_R_OUT
C142 474
VCR_L_OUT
C143 22u/16
R210 1K
MIX_R_OUT
V_G_CON 3,6,8
7
R211 *47k
When recording DVD to VCR,put down this pin
to increase the video signal.
Controled by pin 15 of MSP3415.
C138 104
R204 2.2K
R208 *2.2K
C141 474
C144 2.2u/16
C146 474
C148 2.2u/16
V_OUT
R162 100
R163 100
IIC_SCL
IIC_SDA
C145 *220u/16
C147 22u/16
R212 1k
MIX_L_OUT
3,6,8
R213 *47k
R161 *6.8K
R173 *6.8K
Q30 *3904
C156 104
MIX_CVBS_OUT 2
R174 *470
R209 0
V_OUT
CN5 10P1.25
C149 474
C150 474
VCR_L_IN
VCR_R_IN
VCR_CVBS_OUT
VCR_L_OUT
VCR_R_OUT
Title
<Title>
Size A
Document Number
<Doc>
<RevCode>
Rev
Date: Friday, January 28, 2005
Sheet 10 of 10


K1 CH+
K2 CH-
K3 EJECT
K4 DVD
K5 SOURCE
K6 FWD
K7 VCR
K8 OPEN/CLOSE
K9 PLAY
K10 STOP
K11 PAUSE
K12 REC
K13 REV
K14 PREV
K15 NEXT
U1
UPD16316
U2
HS0038B3V
VFD1
20-0607F(1200229)
CN1
CN2
CN3
CN4
CN5
Q1
8050C
Q2
9015
Q3
9015
Q4
9014
G[1:6]
P[1:16]
STB_LED
P_CTL_PSW
KEYC
KEYB
KEYA
-24V
VDD
VCC
5V_STB
DW9919 panel sch
VFD
4DW9919-2
第 1 张
共 1 张
版次：1.0



更改	数量	更改单号	签名	日期
设 计		审 核	标准化	批 准

开关电源原理图
SWITCH POWER SUPPLY
板号：5DW9919-1

BBK

第 1 张	共 1 张	版次：1.0

广东步步高电子工业有限公司

PV/PH
V_SWP
C_ROT
HEAD_AMP_SW
C_SYNC
COMP_IN
SDA
SCL
VIDEO_ENV_DET
AUDIO_MUTE
REC_H
PB_L

LOGIC 5V
PB CTL IN
REC CTL OUT
REC H
CTL SCHMITT
TU REEL FG
EVER 5V
CAM A
CAM B
CAM C
S610 CAM SW
TP505
RV528 2.2K
RV529 2.2K
RV527 2.2K
TP510 TP503 TP504
RV536 10K
RV597 10K
RV598 10K
START SENSOR
RV571 30K
CV572 B50V/0.01
QV601 PT493F
START SENSOR
RV580 220
Z601
RV577 22K
GP1S566
TAKU UP REEL

BACKUP 5.6V
TP502 TP
DE062
1GW.J43
GJ506 0.6
RV522 220
CE061 16V/470u
TPG02 TP
RV535 47K
RV533 22K
RV534 30K
QV505 BD4725G
VCC NC SUB VOUT GND
CV543 B25V/0.1
CV544 B50V/0.01
CV509 CH 18P
CV510 CH 15P
CV508 CH 8P
CV507 CH 8P
RV537 10K
TP501
XV502 32.768K
RV545 1K
XV501 16M
RV547 1K
RV546 1K
TEST2
TEST1
TEST2
TEST3
CS_CONT
DVD_STROBE
DVD_RESET
OSD/YCA_SCLK
OSD/YCA_SDATA
OSD_STB
OSD_RESET
AUDIO_MUTE
RF_MOD_ON/OFF
MOD.SW
PB(LO)
BUZZER
5X
CAP_F/R
CTL_SCHMITT
CTL_AMP_GAIN
S-SENS
REC_INH
5X_CUE/REV
QV501
TMP93CW76F
TEST1 XTOUT XTIN RESET TEST XOUT XIN DGND CLOCK SU_REEL_FG TU-REEL_FG DVD_CLOCK DVD_DATA_OUT DVD_DATA_IN ADREF AGND CAM_C CAM_B CAM_A VIDEO_ENV_DET HIFI_ENV_DET KEY_IN3 KEY_IN_2 KET_IN_1 ST/SAP/MONO_IN AFT VTR_IIC_CLOCK VTR_IIC_DATA C_COMP_IN CSYN C_FG_IN DPG_IN END_SENSOR REMOTE_IN DFG_IN PB_CTL_IN REC_CTL_OUT SENSOR_CTL HEAD_AMP_SW COROR_ROTARY V-SWP REC_MUTE_H A-SWP REC_H DRUM_PWM CAP_PWM NC4 PV/PH DVCC VKK L-FWD L-REV POWER_GOOD POWER_ON_SIG +B_CTL POWER_ON_SERVO DVD/L2 PWRCNT HMUTE DVD/VTR NC(CP_GRD_INH) AMUTE2 DEW_DET LCD_RESET LCD_STB BACKLIGHT_GRN LCD_DIMMER_GRN BACKLIGHT_AMBE LCD_DIMMER_AMB DVD_POWER_ON VTR_ON POWER_LED REC_LED PLAY_LED EP(LP)_LED DTR_LED RCH_LED LCH_LED YCA_CS VKK

DV504 MTZJ6.2B
LV589 BLM21A601SPT
CV504 5L16V47u
TP509
DV601 GL451V
TP508
RV582 150
RV583 1K
QV581 DTC114EKA
SU REEL FG
COMP IN
SENSOR CTL
RV559 0
RV558 0
RV557 0

V-SWP
C-ROT
HEAD AMP SW
SCL
SDA
VCC
A-SWP
RV247 KETSU
RV248 KETSU
BACKUP_5.6V
LOGIC_5V
EVR_5V
14V
LV507 ELC0607 10uH
26V
DV509 ERA15-02
DV506 ERA15-02
DV503 ERA15-02
DV502 ERA15-02
DV505 MTZJ27B
RV510 330K
CV576 50V47u
CAP_GND
TP511 TP512 TP513 TP514 TP515
HIFI_ENV_DET
AUDIO_MUTE
REC_MUTE_H
A_SWP
SCL
SDA
DV508 0.6
DV510 ERA15-02
RV507 3.9K
RV508 8.2K
CV582 KETSU
P001 TMC-J12P-A2
C-FGA
CAP-VCC
EVER5V
CAP-F/R
CAP-LIMIT
M-GND
S-GND
D/L-VCC
CAP-ERR
L-IN
FG/PG
DM-ERR
LV502 0.6
RV574 10K
CV578 B50V/0.01
CV577 5L10V100u
TP516 TP517
DV507 ERA15-02
CV579 50V47u
CV580 B50V/0.01
TP518
CV581 KETSU
RV579 10K
RV576 470
QV502 DTC144EKA
TP519 TP521 TP522
TP520
RV541 100
RV544 15K
DV543 MTZJ6.2B
LA2 LA1 LA3
RV543 100
QV504
SDA GND SCL A2 WP A1 VCC A0
BR24L04F-WE2
RV545 15K
CV542 B50V/0.01
DV541 MTZJ6.2B
DV542 MTZJ6.2B

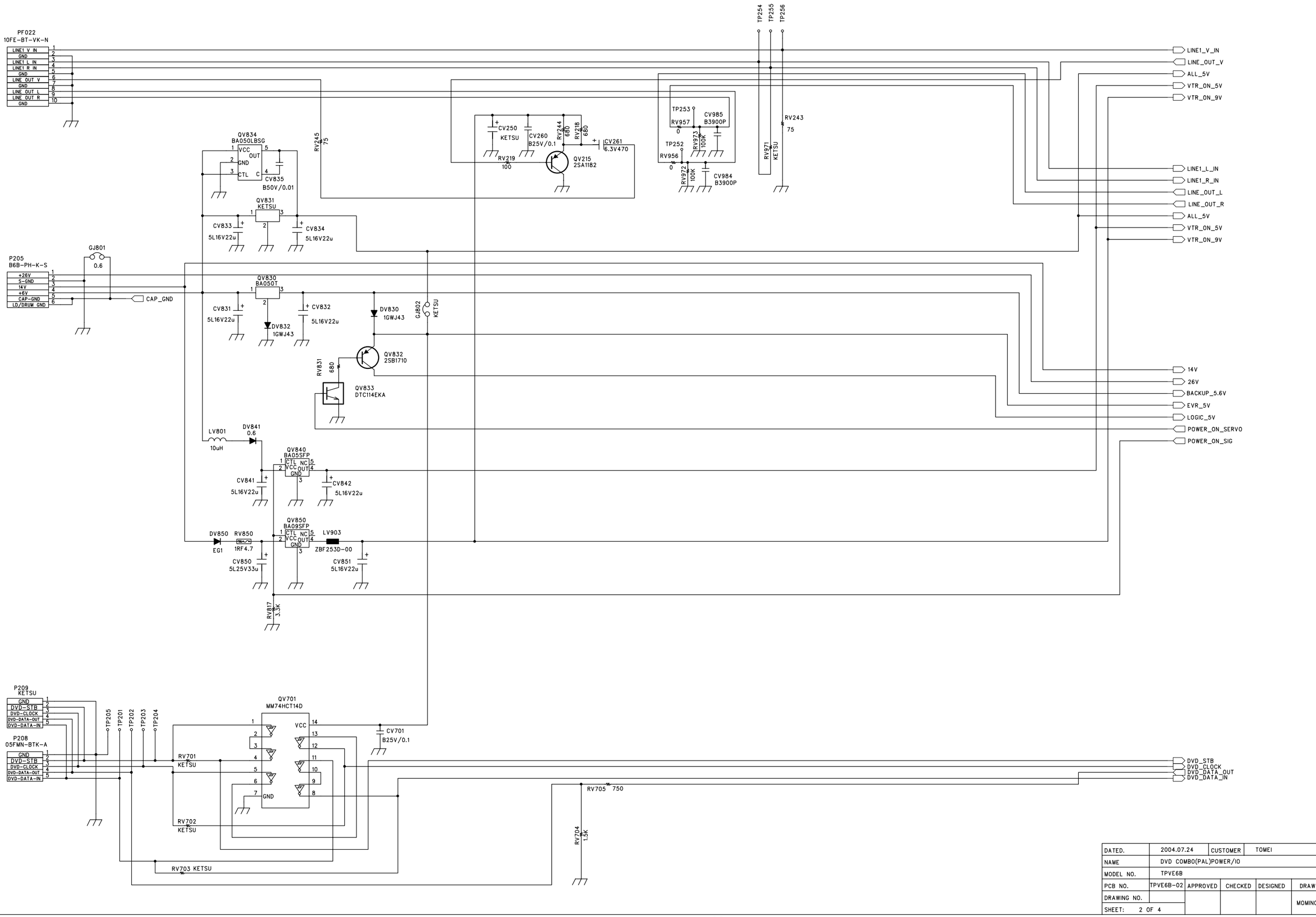
RV575 4.7K
RV532 1.8K
PB_CTL_IN
C_BIAS
CTL_I_O
CTL SCHMITT
PB CTL IN
REC H
S602
REC INH SW
RV564 0
RV565 0
RV538 10K
RV539 10K
CV514 5L16V47u
CTL_OUT VOC2 CTLSCHMT REC_CTL REC_H TRAPE GND2 CTLI/O- CTLI/O+ SW AMP-IN CTLAMP-OUT AGCDET VREF GND1 CREF CR- CR+ IN+ IN- OUT VCC1 CFGA_OUT CFGA_SHARP CFGA_IN CFGB_AMP CFGB_OUT CFGB_IN PG_IN PG_OUT
QV506 LA7123
RV501 KETSU
CV540 KETSU
CV539 KETSU
CV511 B1000P
CV518 B50V/0.01
CV512 5L10V33u
CV513 B1000P
RV504 330
RV505 220K
CV515 KETSU
CV516 CH 470P
RV506 100K
QV512 2SC2412K
QV511 2SA1182
RV512 1/6P220K
RV513 1/6P220K
CV517 5L50V3.3u
RV509 560K
CV522 5L16V22u
CTL AMP GAIN
RV502 1/6P330
RV503 1/6P330
RV4501 0.6
CV545 5L16V47u
CV565 KETSU
CV566 KETSU
RV567 KETSU
RV511 1K
RV566 0
RV562 270
RV563 270
RV568 270
RV569 270
RV570 270
RV560 270
RV561 270
RV530 4.7K
RV589 2.2K
RV519 56K
RV520 56K
RV514 47K
RV515 47K
CV525 B1000P
CV529 B50V/0.01
CV524 B25V/0.015
CV530 B50V/0.01
CV501 5L10V100u
CV502 KETSU
DV530 MTZJ6.2B
LOGIC 5V
PV/PH
DM ERR
CAP ERR
RV304 4.7K
RV301 1K PG
RV305 470K
RV313 4.7K
RV306 13KF
CV302 CH 100P
RV307 12KF
CV301 B25V/0.1
RV309 33KF
RV303 4.7K
QV301 BA10393F
VCC VEE
RV311 10KF
RV302 1K FG
RV308 470K
RV312 20KF
CV304 CH 100P
RV310 8.2KF
CV303 CH 100P
TP523
TP524
POWER_ON_SERVO
POWER_ON_SIG

END SENSOR
RV521 22K
TP506
RV581 220
Z602
QV602 PT493F
TP507
RV578 22K
GP1S566
SUPLY REEL
CV571 B50V/0.01
END SENSOR
REC_H
CV583 KETSU
PV/PH
RV556 1K

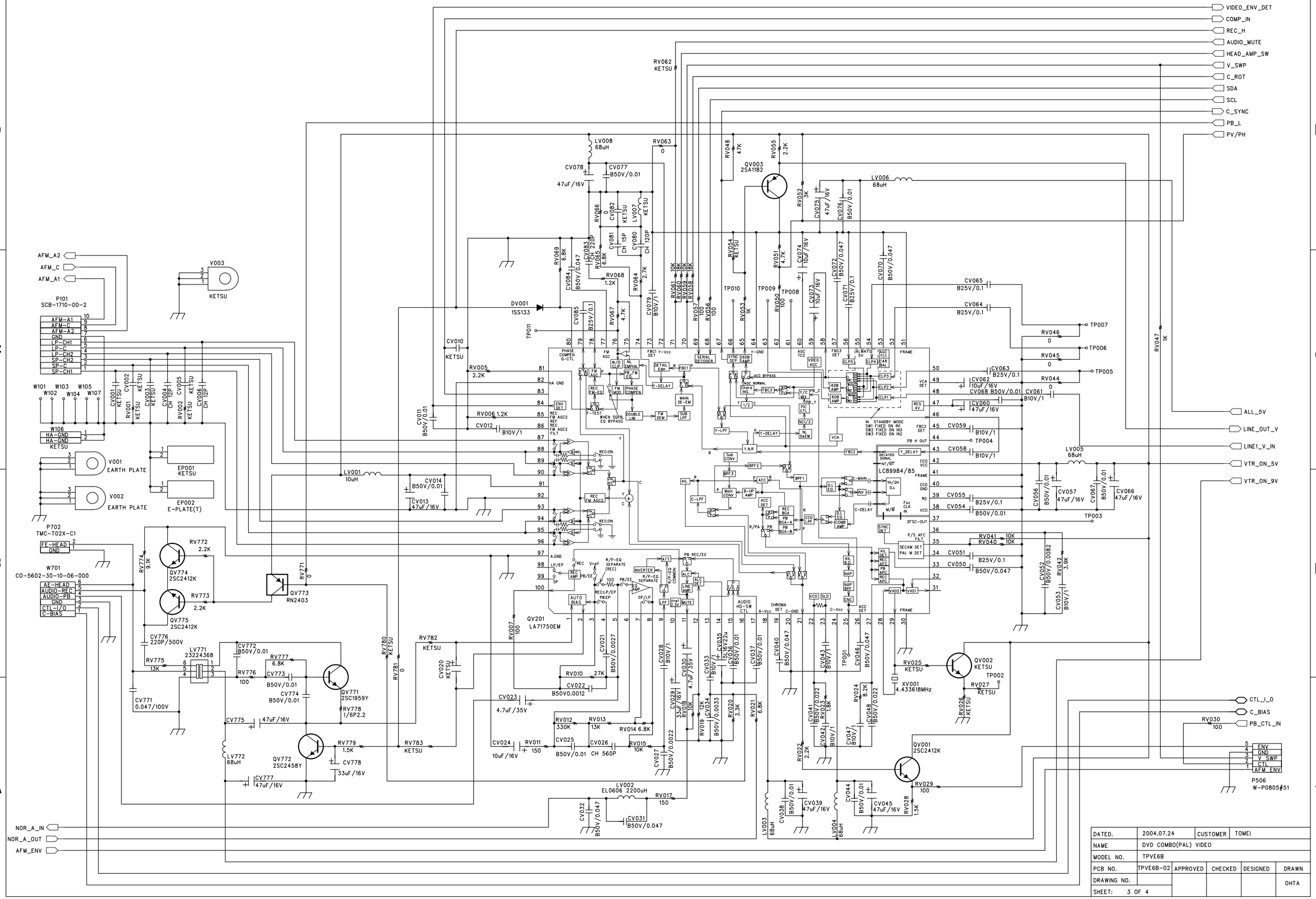
NOT ON MP
OUTSIDE MAIN PCB
DV511 SLR342MC POWER
DV512 SLR342YC REC
DV513 SLR342MC PLAY
DV514 SLR342VC LP
DV515 SLR342MC DTR
DV517 SLR342VC Rch
DV516 SLR342MC Lch
P503 B7B-PH-K-S Lch LED Rch LED DTR LED LP LED PB LED REC LED POWER LED
P502 B3B-XH-A REMOTE IN GND EVER5V
S501 RPM-7138-V4
P204 VTR ON IL-S-2P-S2T2-EF
OUTSIDE MAIN PCB
P501 03JQ-BT REMOTE IN GND EVER5V
P203 B7B-PH-K-S Lch LED Rch LED DTR LED LP LED PB LED REC LED POWER LED
P215 B3B-XH-A REMOTE IN GND EVER5V
TP525
CV541 B25V/0.1

DVD_STB
DVD_CLOCK
DVD_DATA_IN
DVD_DATA_OUT

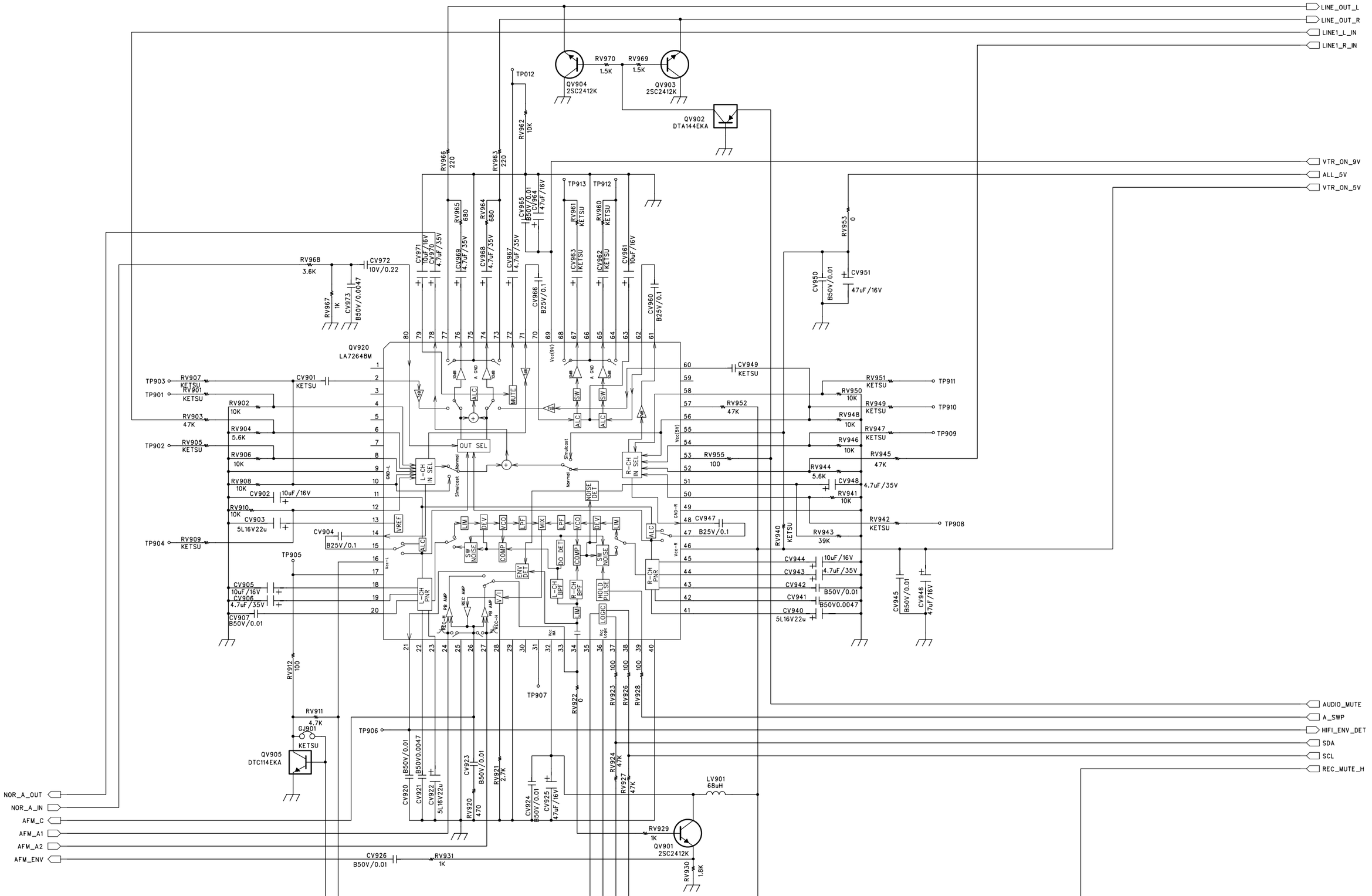
DATED.	2004.07.24	CUSTOMER	TOMEI		
NAME	DVD COMBO(PAL)LOGIC/SERVO				
MODEL NO.	TPVE6B				
PCB NO.	TPVE6B-02	APPROVED	CHECKED	DESIGNED	DRAWN
DRAWING NO.					MOMINO
SHEET: 1 OF 4					



DATED.	2004.07.24	CUSTOMER	TOMEI		
NAME	DVD COMBO(PAL)POWER/IO				
MODEL NO.	TPVE6B				
PCB NO.	TPVE6B-02	APPROVED	CHECKED	DESIGNED	DRAWN
DRAWING NO.					MOMINO
SHEET: 2 OF 4					



DATED.	2004.07.24	CUSTOMER	TOMEI		
NAME	DVD COMBO(PAL) VIDEO				
MODEL NO.	TPVE6B				
PCB NO.	TPVE6B-02	APPROVED	CHECKED	DESIGNED	DRAWN
DRAWING NO.					OHTA
SHEET:	3 OF 4				



DATED.	2004.07.24	CUSTOMER	TOMEI		
NAME	DVD COMBO(PAL) HI-FI				
MODEL NO.	TPVE6B				
PCB NO.	TPVE6B-02	APPROVED	CHECKED	DESIGNED	DRAWN
DRAWING NO.					OHTA
SHEET: 4 OF 4					

PARTS LIST — MAIN BOARD

ITEM		DESCRIPTION			QTY	LOCATION
1		0090001	CHIP RESISTOR	1/16W 0Ω ±5% 0603	11	L5,R70,R72,R83,R84,R90,R101,R115,R137,R140,R148
2		0090296	CHIP RESISTOR	1/16W 18Ω ±5% 0603	10	R151,R154,R156,R158,R160,R164,R166,R168,R170,R172
3		0090004	CHIP RESISTOR	1/16W 22Ω ±5% 0603	28	R19,R20,R21,R23,R24,R26,R27,R28,R29,R30,R31,R32,R33,R34,R35,R52,R53,R55,R57,R65,R119,R122,R123,R124,R125,R134,R139,R214
4		0090005	CHIP RESISTOR	1/16W 33Ω ±5% 0603	8	R76,R162,R163,R174,R175,R219,R220,R221
5		0090220	CHIP RESISTOR	1/16W 51Ω ±5% 0603	21	R44,R45,R46,R47,R48,R49,R50,R51,R54,R56,R58,R59,R60,R61,R62,R63,R64,R66,R67,R68,R117
6		0090291	CHIP RESISTOR	1/16W 56Ω ±5% 0603	13	R120,R121,R126,R127,R153,R155,R157,R159,R161,R165,R167,R169,R171
7		0090273	CHIP RESISTOR	1/16W82Ω±5% 0603	3	R102,R103,R104
8		0090181	CHIP RESISTOR	1/16W 100Ω ±5% 0603	1	R176
9		0090221	CHIP RESISTOR	1/16W 120Ω ±5% 0603	1	R79
10		0090232	CHIP RESISTOR	1/16W 150Ω ±5% 0603	2	R212,R213
11		0090007	CHIP RESISTOR	1/16W 180Ω ±5% 0603	1	R188
12		0090009	CHIP RESISTOR	1/16W 330Ω ±5% 0603	1	R78
13		0090011	CHIP RESISTOR	1/16W 470Ω ±5% 0603	1	R184
14		0090013	CHIP RESISTOR	1/16W 680Ω ±5% 0603	4	R105,R135,R138,R141
15		0090014	CHIP RESISTOR	1/16W 1K ±5% 0603	3	R132,R133,R223
16		0090175	EXACTITUDE CHIP RESISTOR	1/10W 1.18K ±1% 0805	1	R43
17		0090017	CHIP RESISTOR	1/16W 2.2K ±5% 0603	10	R88,R89,R128,R218,R222,R228,R230,R231,R232,C221
18		0090019	CHIP RESISTOR	1/16W 4.7K ±5% 0603	2	R91,R106
19		0090020	CHIP RESISTOR	1/16W 5.1K ±5% 0603	1	R130
20		0090225	CHIP RESISTOR	1/16W 5.6K ±5% 0603	6	R190,R191,R192,R193,R194,R195
21		0090185	CHIP RESISTOR	1/16W 6.2K ±5% 0603	1	R116
22		0090021	CHIP RESISTOR	1/16W 6.8K ±5% 0603	2	R185,R189
23		0090023	CHIP RESISTOR	1/16W 10K ±5% 0603	35	R1,R2,R3,R4,R5,R7,R8,R9,R11,R12,R13,R14,R15,R18,R22,R25,R36,R37,R38,R39,R40,R41,R69,R71,R73,R82,R92,R131,R136,R142,R173,R177,R210,R211,R215
24		0090024	CHIP RESISTOR	1/16W 15K ±5% 0603	2	R143,R144
25		0090034	CHIP RESISTOR	1/16W 100K ±5% 0603	1	R226
26		0090109	CHIP RESISTOR	1/16W 1MΩ ±5% 0603	1	R118
27		0100028	CHIP RESISTOR	1/16W22Ω ±5% 8P	6	RP16,RP18,RP20,RP22,RP24,RP26
28		0100019	CHIP RESISTOR	1/16W33Ω ±5% 8P	8	RP27,RP28,RP29,RP30,RP31,RP32,RP33, RP34
29		0100030	CHIP RESISTOR	1/16W51Ω±5% 8P	20	RP1,RP2,RP3,RP4,RP5,RP6,RP7,RP8,RP9,RP10,RP11,RP12,RP13,RP14,RP15,RP17,RP19,RP21,RP23,RP25
30		0260190	ELEC.CAP	CD110 50V1U±20%5×11 2	1	C164
31		0260033	ELEC.CAP	CD11 25V3.3U±20%5×11 2	2	C265,C266
32		0260019	ELEC.CAP	CD11 16V10U±20%5×11 2	15	C102,C144,C168,C193,C210,C215,C253,C254,C255,C256,C257,C258,C287,C295,C270
33		0260025	ELEC.CAP	CD11 16V47U±20%5×11 2	2	C169,C188
34		0260570	ELEC.CAP	CD11T 16V47U±20%5×11 2	8	C4,C23,CA5,C103,C131,C170,CA1,CA2
35		0260027	ELEC.CAP	CD11 16V100U±20%6×12 2.5	4	C178,C179,C222,C223
36		0260028	ELEC.CAP	CD11 16V220U±20%6×12 2.5	6	CA3,CA4,C184,C186,C196,C250
37		0260214	ELEC.CAP	CD11 16V330U±20%8×12 3.5	5	C182,C194,C296,C298,C299
38		0310043	CHIP CAP	50V 22P ±5% NPO 0603	1	C159
39		0310190	CHIP CAP	50V 27P ±5% NPO 0603	4	C1,C2,C160,C161
40		0310044	CHIP CAP	50V 33P ±5% NPO 0603	2	C198,C200
41		0310045	CHIP CAP	50V 47P ±5% NPO 0603	5	C290,C291,C292,C293, C294
42		0310192	CHIP CAP	50V 56P ±5% NPO 0603	1	C163
43		0310047	CHIP CAP	50V 101 ±5% NPO 0603	6	C237,C239,C243,C245,C248,C252
44		0310049	CHIP CAP	50V 221 ±5% NPO 0603	1	C166
45		0310066	CHIP CAP	50V 102 ±10% 0603	38	C14,C15,C16,C33,C34,C35,C46,C47,C48,C56,C82,C83,C84,C87,C88,C95,C96,C97,C100,C101,C111,C112,C113,C120,C121,C122,C123,C128,C129,C130,C137,C138,C139,C140,C145,C155,C281,C282
46		0310231	CHIP CAP	50V 122 ±10% 0603	6	C259,C260,C261,C262,C263,C264

PARTS LIST						MAIN BOARD
ITEM		DESCRIPTION			QTY	LOCATION
47		0310072	CHIP CAP	50V 103 ±10% 0603	24	C7,C10,C36,C37,C49,C51,C53,C54,C59,C60,C63,C66,C67,C72,C73,C78,C79,C91,C92,C171,C172,C173,C191,C269
48		0310207	CHIP CAP	50V104 ±20% 0603	135	C3,C5,C6,C8,C9,C12,C13,C17~C22,C27~C32,C40~C45,C50,C52,C55,C57,C58,C61,C62,C64,C65,C68~C71,C74~C77,C80,C81,C85,C86,C89,C90,C93,C94,C98,C99,C104~C110,C115~C119,C125,C126,C127,C132~C136,C146,C147,C153,C154,C156,C157,C162,C167,C174~C177,C180,C181,C183,C185,C187,C189,C190,C192,C195,C197,C199,C201~C209,C211~C214,C216~C220,C224~C233,C267,C268,C271,C272,C273,C285,C286,C288,C289,C297,C300,C301
49		0310505	CHIP CAP	25V 224 +80%-20% 0603	1	C165
	49.1	0310112	CHIP CAP	16V 224 ±10% 0603	1	C165
50		0310216	CHIP CAP	10V 105 +80%-20% 0603	2	C283,C284
51		0310219	CHIP CAP	16V 106 +80%-20% 1206	10	C11,C24,C25,C26,C38,C39,C114,C124,C141,C152
52		0390052	FERRITE BEAD	FB	2	L21,L22
53		0390096	CHIP INDUCTOR	1.8UH ±10% 1608	6	L15,L16,L17,L18,L19,L20
54		0390142	CHIP BEAD	FCM1608-601T02	45	FB1,FB2,FB5,FB6,FB7,FB8,FB9,FB10,FB11,FB12,FB13,FB14,FB15,FB16,FB17,FB18,FB19,FB20,FB21,FB22,FB23,FB24,FB25,FB26,FB27,FB28,FB29,FB30,FB31,FB32,FB33,FB34,FB35,L6,L7,L8,L10,L11,L12,L13,L14,L1,L2,L3,L4
55		0700007	CHIP DIODE	1N4148	5	D2,D3,D5,D6,D8
56		0780041	CHIP TRANSISTOR	3906	1	Q1
57		0780040	CHIP TRANSISTOR	3904	1	Q2
58		0881935	IC	DMN-8602 BGA	1	U1
59		0881814	IC	LP2995 SOP	1	U2
60		0881815	IC	M13S128168A-6T TSOP	2	U3,U4
61		0881816	IC	SN74HCT14PWR TSSOP	1	U5
62		0881818	IC	SN74ALVCH16373 TSSOP	1	U7
63		0881819	IC	TSB41AB1PHP QFP	1	U10
64		0881820	IC	PQ018EZ02ZP	1	U11
65		0881127	IC	RT9164-33CG SOT-223	1	U12
66		0881821	IC	PQ025EZ01ZP	1	U13
67		0881936	IC	TVP5146 PQFP	1	U14
68		0881057	IC	CS4360 SSOP	1	U15
69		0881059	IC	CS5333 SSOP	1	U17
70		0960171	CRYSTAL	13.50MHZ 49-S	1	Y1
71		0960169	CRYSTAL	24.576MHz 49-S	1	Y2
72		0960229	CRYSTAL	14.31818MHZ 49-S	1	Y3
73		1631645	PCB	2DW9916-3	1	
74		1940005	SOCKET	6P 2.0mm	1	CN1
75		1940046	SOCKET	10P 2.0mm	1	CN4
76		1940030	SOCKET	10P 2.5mm	1	CN6
77		1940224	SOCKET	4/3P1.0mm	1	CN2
78		1940161	SOCKET	12/12P1.0mm	1	CN3
79		1940120	SOCKET	13/13P1.0mm	1	CN5
80		1940062	SOCKET	20/20P 2.5mm	1	J3
81		3580117	RADIATOR	28×28×12 BBK9906(HK)	1	FOR U1

MAIN PANEL BOARD

No.		DESCRIPTION			QUALITY	LOCATION
1		0000268	Carbon Resistor	1/4W2.2Ω±5%	1	R1
2		0000118	Carbon Resistor	1/6W10Ω±5%	1	R13
3		0000122	Carbon Resistor	1/6W100Ω±5%	1	R12
5		0000133	Carbon Resistor	1/6W4.7K±5%	3	R20,R15,R21
6		0000129	Carbon Resistor	1/6W1K±5%	3	R2,R11,R9
7		0000137	Carbon Resistor	1/6W10K±5%	5	R4,R5,R6,R14,R16
8		0000488	Carbon Resistor	1/6W220Ω±5%	2	R7,R8
9		0000475	Carbon Resistor	1/6W2.7K±5%	3	R17,R18,R19
10		0000667	Carbon Resistor	1/6W270K±5%	1	R3
11		0200124	CER.CAP	50V 102 ±20% 5mm	1	C15
12		0200131	CER.CAP	50V 103 ±10% 5mm	4	C3,C5,C8,C13
	12.1	0200132	CER.CAP	50V 103 ±20% 5mm	4	C3,C5,C8,C13
13		0200138	CER.CAP	50V 104 ±20% 5mm	1	C2
14		0200167	CER.CAP	50V 20P ±10% NPO 2.5mm	2	C9,C10
15		0200212	CER.CAP	50V 30P ±5% NPO 2.5mm	2	C6,C7
16		0260209	CD	CD11 50V22U±20%5×11 2	1	C1
17		0260241	CD	CD11C 16V4.7U±20%4×7 1.5	1	C11
18		0260196	CD	CD11C 16V10U±20%4×7 1.5	1	C14
19		0260200	CD	CD11C 16V47U±20%5×7 2	1	C12
20		0570006	Diode	1N4148	8	D1~D8
21		0620151	led	2B 53SD blue 2×5×7	2	LD2,LD3
22		0780033	Diode	9015C	2	Q2,Q3
23		0780032	Diode	9014C	2	Q4,Q1
	23.1	0780050	Transistor	S8050D	2	Q4,Q1
24		0881013	IC	D16316 QFP	1	U1
25		0960017	Crystal	32.768KHz 3×9	1	Y2
26		0960114	Crystal	5.00MHZ 49-S	1	Y1
27		1200639	VFD	HNV-06SC29 blue	1	VFD1
	27.1	1200633	VFD	GTD-637B	1	VFD1
28		1340003	Switch	6×6×1	15	K1~K15
29		1563255	PCB	4DW9919-2	1	
30		2100003	Line	Φ0.6 7.5mm	9	J9~J17

MAIN PANEL BOARD

No.		DESCRIPTION			QUALITY	LOCATION
31		2100010	Line	Φ0.6 5mm	5	J4,J5,J6,J7,J8
32		2100004	Line	Φ0.6 10mm	3	J1,J2,J3
33		2121546	Line	10P150 2.0	1	CN2 (connect to main board CN4)
34		2121626	Line	5P450 2.0	1	CN1 (connect to power boardCN5)
35		2121548	Line	2P100 2.0	1	CN3 (connect to VCR PCB)
36		2121545	Line	4P140 2.0	1	CN4
37		2110336	Line	20# 150mm	1	GND
38		2110429	Line	20# 90mm	1	GND1
39		2360016	Remote Receiving	HS0038B3V	1	U2

POWER BOARD

No.		DESCRIPTION			QUALITY	LOCATION
1		0000368	Carbon Resistor	1/4W1.8K±5%	1	R22
2		0000163	Carbon Resistor	1/4W10Ω±5%	3	R7,R10,R13
3		0000208	Carbon Resistor	1/4W4.7K±5%	1	R17
4		0000209	Carbon Resistor	1/4W5.1K±5%	1	R24
5		0000215	Carbon Resistor	1/4W9.1K±5%	1	R8
6		0000172	Carbon Resistor	1/4W75Ω±5%	1	R5
7		0000279	Carbon Resistor	1/4W470Ω±5% shape10	1	R15
8		0000283	Carbon Resistor	1/4W1K±5%shape10	1	R4
9		0000213	Carbon Resistor	1/4W7.5K±5%	1	R21
10		0000294	Carbon Resistor	1/4W10K±5%shape10	4	R3,R23,R19,R20
11		0000301	Carbon Resistor	1/4W47K±5%shape10	1	R9
12		0000361	Carbon Resistor	1/4W1.2K±5%	2	R14,R25
13		0010101	Metal Film Resistor	1/4W12K±1%	1	R16
14		0010103	Metal Film Resistor	1/4W8.2K±1%	1	R11
15		0010132	Metal Oxide Resistor	2W39K±5%	1	R2
16		0010235	Metal Oxide Resistor	1/2W36K±5%	2	R1,R6
17		0070001	High Voltage Resistor	1/2W680K±5%	1	RV1
18		0200100	CER.CAP	50V 473 ±20% 2.5mm	1	C9
19		0200123	CER.CAP	50V 102 ±10% 5mm	1	C10
20		0200139	CER.CAP	50V 104 +80%-20% 5mm	12	C2,C7,C8,C11,C12,C15,C16,C20, C21, C22 ,C23,C25
21		0200143	瓷片电容	1000V 102 ±10% 7.5mm	1	C4
22		0200225	CAP	400VAC 222 ±20% 10mm	1	C6
23		0200232	CER.CAP	500V 101 ±10% 5mm	4	C17,C18,C19,C24
24		0200268	CAP	CT81 400V221±10% 10mm	2	C3,C14
25		0210066	CAP	275V 104 ±20% 15mm	1	C13
	25.1	0210070	CAP	275V 104 ±10% 15mm	1	C13
26		0260581	CD	CD11T 25V100U±20%6×12 2.5	6	CE1,CE2,CE12,CE16,CE20,CE23
27		0260564	CD	CD11T 50V10U±20%5×11 2	1	CE21
28		0260622	CD	CD11T 50V100U±20%8×12 3.5	1	CE19
29		0260558	CD	CD11T 25V470u±20%10×16 5	1	CE4
30		0260582	CD	CD11T 25V10U±10%5×11 2	2	CE7,CE22

POWER BOARD

No.		DESCRIPTION			QUALITY	LOCATION
31		0260559	CD	CD11T 50V47u±20%6×12 2.5	3	CE11,CE13,CE14
32		0260400	CD	GZ 25V1000U±20%10×25 5	1	CE3
33		0260583	CD	CD11T 16V220U±20%6×12 2.5	2	CE15,CE17
34		0260442	CD	GZ 10V2200U±20%10×24 5	2	CE6,CE9
35		0260443	CD	GZ 10V1000U±20%8×16 3.5	2	CE8,CE10
36		0260621	CD	CD11T 63V220U±20％10×20 5	1	CE18
37		0260584	CD	LT 400V100U±20%22×30 10	1	CE5
38		0390052	Ferrite bead	FB	2	L1,L4
39		0410077	Inductor	10UH 3A 5mm	3	L2,L3,L5
40		0410171	Inductor	30uH 3A 5mm	1	L6
41		0410065	Inductor	20UH 3A 5mm	1	L7
42		0570005	Diode	1N4007	4	D9,D10,D11,D12
43		0570007	Diode	1N5401	2	D14,D15
44		0570013	Diode	HER105	5	D1,D6,D7,D8,D16
45		0570018	Diode	HER303	1	D2
46		0570053	Diode	FR207 DO-15	1	D4
47		0580006	Zener	5.1V 1/2W	1	D13
48		0580033	Zener	5.6V 1/2W	1	D19
49		0580048	Zener	22V 1/2W	1	D17
50		0580025	Zener	27V 1W	1	D18
51		0680047	Diode	PBYR10100 TO-220	2	D3,D5
	51.1	0680056	Diode	SR10A0 TO-220	2	D3,D5
52		0580014	Zener	25V 1/2W	1	D20
53		0780138	Diode	8050D	1	Q4
54		0780286	Diode	2SD669A TO-92	1	Q3
55		0780033	Diode	9015C	1	Q6
56		0780032	Diode	9014C	1	Q5
	56.1	0780023	Diode	2N3904	1	Q5
57		0790024	Mosfet	1PP14N03L TO-220	2	Q1,Q2
	57.1	0790025	Mosfet	AP40N03P TO-220	2	Q1,Q2
	57.2	0790028	Mosfet	1PP15N03L TO-220	2	Q1,Q2
58		0880553	IC	LM431ACZ TO-92	3	IC3,IC5,IC6
	58.1	0880581	IC	TL431C TO-226AA(LP)	3	IC3,IC5,IC6

POWER BOARD

No.		DESCRIPTION			QUALITY	LOCATION
	58.2	0880800	IC	431L TO-92	3	IC3,IC5,IC6
59		0881326	IC	PQ12RD21 TO-220	1	IC4
60		0881934	IC	FSDM0565R TO-220F-6L	1	IC1
61		1000004	Power Net Filter	UT-20 40mH ±20% 10×13	1	LF1
62		1050002	Therm Resistor	NTC SCK-104MS±20%	1	RT1
63		1080005	Opto Coupling	NEC2561	1	IC2
	63.1	1080006	Opto Coupling	PC817	1	IC2
	63.2	1080007	Opto Coupling	NEC2501	1	IC2
	63.3	1080011	Opto Coupling	HS817	1	IC2
	63.4	1080016	Opto Coupling	K1010 C	1	IC2
64		1940001	Socket	2pin 2.5mm	1	CN1
65		1940004	Socket	5pin 2.5mm	1	CN2
66		1940005	Socket	6pin 2.0mm	1	CN6
67		1940024	Socket	5pin 2.0mm	1	CN5
68		1940030	Socket	10pin 2.5mm	1	CN3
69		1940037	Socket	4pin 3.96mm	1	CN4
70		1940045	Socket	2芯 8.0mm 2#	1	BCN1
80		0460427	Power Switch transforme	BCK-28-0534	1	T1
81		1563252	PCB	5DW9919-1	1	

AV BOARD

No.		PART		DESCRIPTION		LOCATION
1		0000276	Carbon Resistor	1/4W100Ω±5% Shape10	2	R153,R152
2		0090001	Chip Resistor	1/16W 0Ω ±5%	5	R16,R22,R209,R120,R121
3		0090003	Chip Resistor	1/16W 10Ω ±5%	3	R66,R67,R144
4		0090004	Chip Resistor	1/16W 22Ω ±5%	1	R124
5		0090006	Chip Resistor	1/16W 75Ω ±5% 0603	5	R136,R139,R149,R150,R135
6		0090007	Chip Resistor	1/16W 180Ω ±5%	5	R39,R47,R98,R104,R108
7		0090008	Chip Resistor	1/16W 220Ω ±5%	3	R1,R65,R111
8		0090009	Chip Resistor	1/16W 330Ω ±5%	6	R52,R61,R73,R80,R85,R92
9		0090011	Chip Resistor	1/16W 470Ω ±5%	6	R40,R48,R99,R105,R109,R172
10		0090014	Chip Resistor	1/16W 1K ±5%	10	R57,R58,R76,R77,R88,R89,R112,R155,R202,R148
11		0090223	Chip Resistor	1/16W 2K ±5% 0603	2	R156,R171
12		0090017	Chip Resistor	1/16W 2.2K ±5%	4	R68,R145,R180,R204,R141
13		0090018	Chip Resistor	1/16W 3.3K ±5%	5	R12,R15,R138,R151,R183
14		0090019	Chip Resistor	1/16W 4.7K ±5%	19	R50,R51,R59,R60,R71,R72,R78,R79,R83,R84,R90,R91,R125 ,R147,R170,R200,R169,R166,R178
15		0090020	Chip Resistor	1/16W 5.1K ±5%	3	R7,R146,R143
16		0090021	Chip Resistor	1/16W 6.8K ±5%	9	R36,R38,R44,R46,R97,R103,R107,R168,R165
17		0090186	Chip Resistor	1/16W 7.5K ±5% 0603	2	R182,R179
18		0090023	Chip Resistor	1/16W 10K ±5%	10	R11,R14,R23,R116,R117,R118,R137,R142,R154,R157
19		0090187	Chip Resistor	1/16W 12K ±5% 0603	13	R94,R102,R106,R113,R114,R164,R167,R4,R5,R19,R21,R33, R34
20		0090024	Chip Resistor	1/16W 15K ±5%	6	R2,R3,R17,R20,R28,R29
21		0090025	Chip Resistor	1/16W 20K ±5%	6	R49,R55,R70,R75,R82,R87
22		0090026	Chip Resistor	1/16W 22K ±5%	1	R62
23		0090028	Chip Resistor	1/16W 33K ±5%	2	R54,R63
24		0090029	Chip Resistor	1/16W 47K ±5%	7	R53,R64,R74,R81,R86,R93,R140
25		0090034	Chip Resistor	1/16W 100K ±5%	2	R56,R201
26		0090181	Chip Resistor	1/16W 100Ω ±5%	3	R119,R162,R163
27		0090189	Chip Resistor	1/16W 30K ±5%	1	R69
28		0090242	Chip Resistor	1/16W 75K ±5%	1	R115
29		0260019	CD	CD11 16V10U±20%5×11	16	C29,C34,C49,C53,C57,C61,C64,C76,C78,C90,C93,C109, C110,C111,C114,C25
30		0260025	CD	CD11 16V47U±20%5×11	10	C1,C7,C9,C38,C43,C82,C99,C102,C104,C118

AV BOARD

No.		PART		DESCRIPTION		LOCATION
31		0260027	CD	CD11 16V100U±20%6×1	3	C11,C37,C129
32		0260028	CD	CD11 16V220U±20%6×1	10	C16,C22,C23,C66,C67,C69,C136,C153,C154,C164
33		0260067	CD	CD11 50V2.2U±20%5×11	13	C123,C124,C125,C126,C134,C140,C141,C142,C144,C146,C148,C149,C150
34		0260127	CD	CD11 16V4.7U±20%5×11	9	C3,C4,C5,C6,C13,C14,C15,C19,C20
35		0260001	CD	CD11 16V22U±20%5×11	2	C143,C147
36		0260211	CD	CD11 50V3.3U±20%5×11	1	C73
37		0310047	Chip Capasitor	50V 101 ±5% NPO 0603	1	C79
38		0310048	Chip Capacitor	50V 151 ±5% NPO 0603	6	C28,C33,C48,C52,C56,C60
39		0310066	Chip Capasitor	50V 102 ±10% 0603	15	C18,C30,C31,C35,C36,C50,C51,C54,C55,C58,C59,C62,C63,C87,C88
40		0310067	Chip Capacitor	50V 152 ±10% 0603	1	C91
41		0310072	Chip Capasitor	50V 103 ±10% 0603	5	C10,C12,C17,C32,C94
42		0310188	Chip Capacitor	50V 10P ±5% NPO 0603	2	C85,C89
44		0310192	Chip Capasitor	50V 56P ±5% NPO 0603	2	C80,C83
45		0310196	Chip Capacitor	50V 471 ±10% 0603	1	C92
46		0310202	Chip Capacitor	50V 223 ±10% 0603	1	C131
47		0310207	Chip Capasitor	50V104 ±20% 0603	38	C2,C8,C21,C39,C40,C41,C42,C44,C45,C46,C47,C65,C68,C75,C77,C81,C98,C100,C103,C105,C106,C119,C120,C127,C128,C130,C132,C133,C135,C137,C138,C139,C155,C157,C158,C163,C165,C24
48		0310379	Chip Capacitor	25V 474 +80%-20% 0603	6	C70,C71,C72,C74,C84,C86
	48.1	0310542	Chip Capacitor	16V 474±10% 0603	6	C70,C71,C72,C74,C84,C86
49		0390095	Chip Bead	FCM1608K-221T05	24	FB3~FB12,R6,R10,R13,R24,R27,R31,R35,R37,R42,R95,R96,R100,R101,R134
50		0390142	Chip Bead	FCM1608-601T02	2	FB1,FB2
51		0580007	Zener	6.2V 1/2W	2	D1,D2
52		0580008	Zener	8.2V 1/2W	1	D11
53		0680057	ChipSchottky	LL60P MINI-MELF	1	D24
54		0580054	Zener	9.1V 1W	1	D21
55		0700007	Chip Diode	1N4148	10	D16,D18,D20,D25~D28,D30,D31,D32
56		0700056	Chip Double Diode	MMBD4148SE SOT-23	5	D13,D14,D15,D17,D19
57		0780040	Chip Transistor	3904	25	Q1~Q5,Q8~Q16,Q21~Q27,Q29,Q32,Q33,Q36

AV BOARD

No.		PART		DESCRIPTION		LOCATION
	57.1	0780062	Chip Transistor	9014C	25	Q1~Q5,Q8~Q16,Q21~Q27,Q29,Q32,Q33,Q36
58		0780041	Chip Transistor	3906	5	Q6,Q7,Q28,Q35,Q37
	58.1	0780063	Chip Transistor	9015C	5	Q6,Q7,Q28,Q35,Q37
59		0880443	IC	CD4052BCN DIP	1	U1
	59.1	0881429	IC	CD4052BE DIP	1	U1
60		0881226	IC	RC4558D SOP	3	U3,U4,U5
61		0881693	IC	TL 74HC4052D SOP	1	U9
62		0881842	IC	MSP3415G QFP	1	U6
63		0881992	IC	74HC4053D SOP	2	U10,U11
65		0882267	IC	FSAV330 TSSOP	2	U7,U8
66		0882304	IC	MM1313AD SDIP	1	U12
67		0960238	Crystal	18.432MHz ±10PPM 49-S	1	X2
69		1020023	Tuner	JS-6B2F/L121-D5	1	TUN1
70		1090009	Optical Output	GP1F32T	1	OP1
	70.1	1090024	Optical Output	TX179AT	1	OP1
71		1631956	PCB	7DW9919-3	1	
72		1860051	SCART Socket	0	1	SC1
73		1910059	Socket	CS-09	2	S2,S3
74		1910062	Socket	AV2-8.4--6G	1	S1
75		1910063	Socket	AV12-8.4--2G-2	1	S4
76		1940004	Socket	5pin 2.5mm	1	CN4
77		1940057	Socket	5pin 1.25mm	1	CN5
78		1940023	Socket	7pin 2.0mm	1	CN3
79		1940120	Socket	13pin 1.0mm	1	CN2
80		1940161	Socket	12pin 1.0mm	1	CN1
81		1940224	Socket	4/3pin 1.0mm	1	CN6