

Advance Information Supplement

Subject:	Additional Information for the VCT 49xxI
Data Sheet Concerned:	VCT 49xxI 6251-573-1AI, Edition Jan. xx, 2003
Supplement:	No. 1/ 6251-573-3AIS
Edition:	Mar. 27, 2003

VCT 49xxI-C0

27.03.2003

The VCT 49xxI-C0 is pin- and hardware-compatible to VCT 49xxI-B0. Problem 21 has been corrected in this version. Problem 16 has been slightly improved in this version.

VCT 49xxI-C0 includes functionality of DRX396xA-G6.

Problem list for VCT 49xxI-C0

No.	Problem	Description	Comment	OK
1	PLL reset	The internal clock PLL remains in reset mode.	solved by metalfix	B0
2	Clamping windows swapped	The clamping measurement and clamping pulse windows are swapped.	hardware redesign C1 workaround: swap I ² C settings (start position and duration) for measurement and pulse	
3	Clamp current swapped	Chroma and CVBS/RGB clamp currents are swapped. Thus, the clamping performance (e.g. 50/60Hz suppression) is reduced for all input signals.	solved by metalfix	B0
4	SVM	SVM uses wrong input signal. Thus, the SVM signal doesn't fully match to the corresponding RGB signal	hardware redesign C1	
5	LSE	The combination of peaked and LTied signals doesn't work for LMIXOFS > 15	hardware redesign C1 workaround: select LMIXOFS 0...15	
6	Peaking filter overflow	In case of PKCF=2,3, the peaking filter output overflows.	hardware redesign C1 workaround: select PKCF=0,1 only	

No.	Problem	Description	Comment	OK
7	NCE	Gamma correction and white shaping performed by NCE are incorrect	hardware redesign C1	
8	BLE/DCI	sometimes a channel change corrupts the BLE and/or DCI picture content measurement, which results in a very dark picture	hardware redesign C1 workaround: re-write DCION=0 and BLEM-ODE=0	
9	Testpattern & picture frame generator color multiplex swapped	The CrCb color multiplex of the testpattern and picture frame generator is swapped.	hardware redesign C1 workaround: swap corresponding CrCb I ² C settings	
10	color noise on RGB	depending on supply voltage VSUP1.8FE and VSUP3.3xx color noise may be visible	partly solved by metalfix hardware redesign C1	
11	supply current on VSUP3.3FE is too high	short in internal supply net causes increased supply current	solved by metalfix	B0
12	Deflection & Tube Measurement	XDFP firmware not fully functional: – cutoff & whitedrive – EHT & BCL – H/V protection – H/V blanking	firmware change C1 workaround: firmware update via flash	
13	DRX/MSP: Korean Stereo-Sound not working properly	Limited Stereo Performance in TV-Sound Standard Korea due to mis-configured SIF-filtering in DRX-part	firmware change C1 Workaround: s. DRX-VI2C	
14	MSP: MODUS[11] for FM-Radio US/EU not working, if standard 40h is selected	MODUS[11] = 1 is not accepted if standard 40h is selected. Instead of FM-Radio Europe the US-Standard is set.	firmware change C1 Workaround: use automatic Standard detection or set deemph=50µs manually	
15	MSP: Virtual Processing not working with NICAM-Input	Noise, as soon as Virtual Processing is switched on with NICAM-Input	firmware change C1 Workaround: Set DSP Reg. 2Dh (MBASS-Cutoff) Value #0	
16	Crosstalk on IF Signal	20.25Mhz crystal oscillator causes interference on IF input signal	metal fix C0 hardware redesign C1	
17	Wrong Interlace	H/V display raster disturbed by wrong synchronisation	hardware redesign C1 workaround: XDFP firmware update via flash after final investigation	
18	Vertical Synchronisation	Vertical pull-in after channel change takes too long	hardware redesign C1 workaround: increase LPFOPOFF	
19	DRX Output Level	DRX delivers only 0.7V video output level.	hardware redesign C1	

No.	Problem	Description	Comment	OK
20	Video Output Level	VOUTx pins deliver only 0.9V video output level instead of 1.0V	hardware redesign C1	
21	CADC reset	CADC stays in reset mode	metal fix C0 hardware redesign C1	C0
22	MPS: RDS	RDS firmware not functional	firmware change C1	
23	Bootloader	Bootloader cannot program flash address range 0xC000-0xFFFF because of wrong XDATA mapping.	firmware change C1 workaround: modified download via VI2C tool	
24	Italics Font	Italics ROM font cannot be displayed completely because of DRCS boundary=384.	hardware redesign C1	
25	Testpattern 3	Testpattern 3 (Y ramp) increment is too high.	hardware redesign C1	
26	Picture Frame Blanked	Left side of picture frame is blanked if HORPOSG<180.	hardware redesign C1	
27	Port3	SFR P3 (hA0) is mapped to Port1. The alternate functions of P3x pins are still available via Port Mux.	hardware redesign C1 workaround: don't use Port3	
28	Tube Measurement Interface	Interface to XDFP not fully functional: – dynamic EHT & peak BCL – cutoff & whitedrive – static EHT & average BCL	hardware redesign C1	
29	I2C Interface	– no software reset possible – SDA,SCL cannot be addressed directly as port pins	hardware redesign C1	
30	Contrast Reduction	Activ contrast reduction causes OSD contrast to be reduced as well.	hardware redesign C1 workaround: set CORLEV=0	
31	Vertical Peaking	Vertical Peaking mode in Comb filter causes sync problems	hardware redesign C1	
32	missing HOUT pulse	If VSUP1.8Dig < 1.7V HOUT pulses are sporadically missing.	hardware redesign C1	
33	Standard I and L: FM/AM-mono distorted	in absence of any NICAM carrier after reset the analog sound is distorted.	firmware change C1 workaround: write after reset <8C 10 04 98 00 03>	

No.	Problem	Description	Comment	OK
DRX_S_10	Carrier Recovery	The DRX396xA-F5 has been sensible against modulator imbalance. The value range of internal registers has been changed to enable more robustness. Tests with several very critical configurations concerning residual carrier and modulator imbalance has led to the following recommendation for G6 version:	firmware change C1 workaround: change the following DRX register to the recommended values: 0x1017 = 0x0002 # CR_AMP_TH 0x1015 = 0x00fa # CR_OVM_TH 0x1014 = 0x009b # CR_P/F/I	
DRX_2	Moire	Moire is visible at different input levels, caused by intermodulation of picture carrier and sound carrier, especially at L-standard or unmodulated sound carrier.	Moire is caused by the INL of the ADC. Nonlinearity of the ADC will be further improved by the next step.	
DRX_4a	Video SNR	Video SNR below limits in standard I and L/L'.		
DRX_4b	AM Sound SNR	AM Sound SNR below limits.		
DRX_4c	FM Sound SNR	FM Sound SNR below limits.	Reduction of CR_P from 4 to 3 causes reduction of FM sound SNR	

VCT 49xxI-B0**11.03.2003**

The VCT 49xxI-B0 is pin- and hardware-compatible to VCT 49xxI-A0. Problems 1, 3 and 11 have been corrected in this version.

VCT 49xxI-B0 includes functionality of DRX396xA-G6.

Problem list for VCT 49xxI-B0

No.	Problem	Description	Comment	OK
1	PLL reset	The internal clock PLL remains in reset mode.	solved by metalfix	B0
2	Clamping windows swapped	The clamping measurement and clamping pulse windows are swapped.	hardware redesign C1 workaround: swap I ² C settings (start position and duration) for measurement and pulse	
3	Clamp current swapped	Chroma and CVBS/RGB clamp currents are swapped. Thus, the clamping performance (e.g. 50/60Hz suppression) is reduced for all input signals.	solved by metalfix	B0
4	SVM	SVM uses wrong input signal. Thus, the SVM signal doesn't fully match to the corresponding RGB signal	hardware redesign C1	
5	LSE	The combination of peaked and LTied signals doesn't work for LMIXOFS > 15	hardware redesign C1 workaround: select LMIXOFS 0...15	
6	Peaking filter overflow	In case of PKCF=2,3, the peaking filter output overflows.	hardware redesign C1 workaround: select PKCF=0,1 only	
7	NCE	Gamma correction and white shaping performed by NCE are incorrect	hardware redesign C1	
8	BLE/DCI	sometimes a channel change corrupts the BLE and/or DCI picture content measurement, which results in a very dark picture	hardware redesign C1 workaround: re-write DCION=0 and BLEM-ODE=0	
9	Testpattern & picture frame generator color multiplex swapped	The CrCb color multiplex of the testpattern and picture frame generator is swapped.	hardware redesign C1 workaround: swap corresponding CrCb I ² C settings	
10	color noise on RGB	depending on supply voltage VSUP1.8FE and VSUP3.3xx color noise may be visible	partly solved by metalfix hardware redesign C1	

No.	Problem	Description	Comment	OK
11	supply current on VSUP3.3FE is too high	short in internal supply net causes increased supply current	solved by metalfix	B0
12	Deflection & Tube Measurement	XDFP firmware not fully functional: – cutoff & whitedrive – EHT & BCL – H/V protection – H/V blanking	firmware change C1 workaround: firmware update via flash	
13	DRX/MSP: Korean Stereo-Sound not working properly	Limited Stereo Performance in TV-Sound Standard Korea due to mis-configured SIF-filtering in DRX-part	firmware change C1 Workaround: s. DRX-VI2C	
14	MSP: MODUS[11] for FM-Radio US/EU not working, if standard 40h is selected	MODUS[11] = 1 is not accepted if standard 40h is selected. Instead of FM-Radio Europe the US-Standard is set.	firmware change C1 Workaround: use automatic Standard detection or set deemph=50µs manually	
15	MSP: Virtual Processing not working with NICAM-Input	Noise, as soon as Virtual Processing is switched on with NICAM-Input	firmware change C1 Workaround: Set DSP Reg. 2Dh (MBASS-Cutoff) Value #0	
16	Crosstalk on IF Signal	20.25Mhz crystal oscillator causes interference on IF input signal	metal fix C0 hardware redesign C1	
17	Wrong Interlace	H/V display raster disturbed by wrong synchronisation	hardware redesign C1 workaround: XDFP firmware update via flash after final investigation	
18	Vertical Synchronisation	Vertical pull-in after channel change takes too long	hardware redesign C1 workaround: increase LPFOPOFF	
19	DRX Output Level	DRX delivers only 0.7V video output level.	hardware redesign C1	
20	Video Output Level	VOUTx pins deliver only 0.9V video output level instead of 1.0V	hardware redesign C1	
21	CADC reset	CADC stays in reset mode	metal fix C0 hardware redesign C1	
22	MPS: RDS	RDS firmware not functional	firmware change C1	
23	Bootloader	Bootloader cannot program flash address range 0xC000-0xFFFF because of wrong XDATA mapping.	firmware change C1 workaround: modified download via VI2C tool	
24	Italics Font	Italics ROM font cannot be displayed completely because of DRCS boundary=384.	hardware redesign C1	
25	Testpattern 3	Testpattern 3 (Y ramp) increment is too high.	hardware redesign C1	

No.	Problem	Description	Comment	OK
26	Picture Frame Blanked	Left side of picture frame is blanked if HORPOSG<180.	hardware redesign C1	
27	Port3	SFR P3 (hA0) is mapped to Port1. The alternate functions of P3x pins are still available via Port Mux.	hardware redesign C1 workaround: don't use Port3	
28	Tube Measurement Interface	Interface to XDFP not fully functional: – dynamic EHT & peak BCL – cutoff & whitedrive – static EHT & average BCL	hardware redesign C1	
29	I2C Interface	– no software reset possible – SDA,SCL cannot be addressed directly as port pins	hardware redesign C1	
30	Contrast Reduction	Activ contrast reduction causes OSD contrast to be reduced as well.	hardware redesign C1 workaround: set CORLEV=0	
31	Vertical Peaking	Vertical Peaking mode in Comb filter causes sync problems	hardware redesign C1	
32	missing HOUT pulse	If VSUP1.8Dig < 1.7V HOUT pulses are sporadically missing.	hardware redesign C1	
33	Standard I and L: FM/AM-mono distorted	in absence of any NICAM carrier after reset the analog sound is distorted.	firmware change C1 workaround: write after reset <8C 10 04 98 00 03>	
DRX_S_10	Carrier Recovery	The DRX396xA-F5 has been sensible against modulator imbalance. The value range of internal registers has been changed to enable more robustness. Tests with several very critical configurations concerning residual carrier and modulator imbalance has led to the following recommendation for G6 version:	firmware change C1 workaround: change the following DRX register to the recommended values: 0x1017 = 0x0002 # CR_AMP_TH 0x1015 = 0x00fa # CR_OVM_TH 0x1014 = 0x009b # CR_P/F/I	
DRX_2	Moire	Moire is visible at different input levels, caused by intermodulation of picture carrier and sound carrier, especially at L-standard or unmodulated sound carrier.	Moire is caused by the INL of the ADC. Nonlinearity of the ADC will be further improved by the next step.	
DRX_4a	Video SNR	Video SNR below limits in standard I and L/L'.		
DRX_4b	AM Sound SNR	AM Sound SNR below limits.		
DRX_4c	FM Sound SNR	FM Sound SNR below limits.	Reduction of CR_P from 4 to 3 causes reduction of FM sound SNR	

VCT 49xxl-A0

13.01.2003

Problem list for VCT 49xxl-A0

No.	Problem	Description	Comment	OK
1	PLL reset	The internal clock PLL remains in reset mode.	hardware redesign B0 workaround: Send I2C telegram <BC F0 00 81> by VI2C tool to start clock PLL after power up. Load "monitor.hex" into flash to avoid that on-chip boot-loader turns off PLL again.	
2	Clamping windows swapped	The clamping measurement and clamping pulse windows are swapped.	hardware redesign C1 workaround: swap I ² C settings (start position and duration) for measurement and pulse	
3	Clamp current swapped	Chroma and CVBS/RGB clamp currents are swapped. Thus, the clamping performance (e.g. 50/60Hz suppression) is reduced for all input signals.	hardware redesign B0 workaround: reduce size of clamp capacitor for CVBS/RGB and/or increase size for C signals	
4	SVM	SVM uses wrong input signal. Thus, the SVM signal doesn't fully match to the corresponding RGB signal	hardware redesign C1	
5	LSE	The combination of peaked and LTied signals doesn't work for LMIXOFS > 15	hardware redesign C1 workaround: select LMIXOFS 0...15	
6	Peaking filter overflow	In case of PKCF=2,3, the peaking filter output overflows.	hardware redesign C1 workaround: select PKCF=0,1 only	
7	NCE	Gamma correction and white shaping performed by NCE are incorrect	hardware redesign C1	
8	BLE/DCI	sometimes a channel change corrupts the BLE and/or DCI picture content measurement, which results in a very dark picture	hardware redesign C1 workaround: re-write DCION=0 and BLEM-ODE=0	
9	Testpattern & picture frame generator color multiplex swapped	The CrCb color multiplex of the testpattern and picture frame generator is swapped.	hardware redesign C1 workaround: swap corresponding CrCb I ² C settings	

No.	Problem	Description	Comment	OK
10	color noise on RGB	depending on supply voltage VSUP1.8FE and VSUP3.3xx color noise may be visible	hardware redesign B0	
11	supply current on VSUP3.3FE is too high	short in internal supply net causes increased supply current	hardware redesign B0	
12	Deflection & Tube Measurement	XDFP firmware not fully functional no control of following features: – soft start – angle & bow – cutoff & whitedrive – e/w pwm output – EHT compensation	firmware change C1 workaround: firmware update via flash after final investigation	
13	DRX/MSP: Korean Stereo-Sound not working properly	Limited Stereo Performance in TV- Sound Standard Korea due to mis- configured SIF-filtering in DRX- part	firmware change C1 Workaround: s. DRX-VI2C	
14	MSP: MODUS[11] for FM-Radio US/EU not working, if standard 40h is selected	MODUS[11] = 1 is not accepted if standard 40h is selected. Instead of FM-Radio Europe the US-Stan- dard is set.	firmware change C1 Workaround: use automatic Stan- dard detection or set deemph=50µs manually	
15	MSP: Virtual Process- ing not working with NICAM-Input	Noise, as soon as Virtual Process- ing is switched on with NICAM- Input	firmware change C1 Workaround: Set DSP Reg. 2Dh (MBASS-Cutoff) Value #0	
16	Crosstalk on IF Signal	20.25Mhz crystal oscillator causes interference on IF input signal	hardware redesign C1	
17	Wrong Interlace	H/V display raster disturbed by wrong synchronisation	hardware redesign C1 workaround: XDFP firmware update via flash after final investigation	
18	Vertical Synchronisa- tion	Vertical pull-in after channel change takes too long	hardware redesign C1 workaround: increase LPFOPOFF	
19	DRX Output Level	DRX delivers only 0.7V video out- put level.	hardware redesign C1	
20	Video Output Level	VOUtx pins deliver only 0.9V video output level instead of 1.0V	hardware redesign C1	
21	CADC reset	CADC stays in reset mode	hardware redesign C1	
22	MPS: RDS	RDS firmware not functional	firmware change C1	
23	Bootloader	Bootloader cannot program flash address range 0xC000-0xFFFF because of wrong XDATA map- ping.	firmware change C1 workaround: modified download via VI2C tool	
24	Italics Font	Italics ROM font cannot be dis- played completely because of DRCS boundary=384.	hardware redesign C1	

No.	Problem	Description	Comment	OK
25	Testpattern 3	Testpattern 3 increment too high	hardware redesign C1	
26	Picture Frame Blanked	Left side of picture frame is blanked.	hardware redesign C1	