

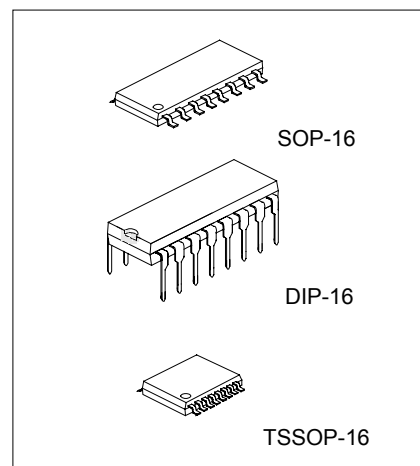
ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

DESCRIPTION

The UTC **4053** are Triple SPDT analog multiplexers for application as digitally-controlled analog switches.

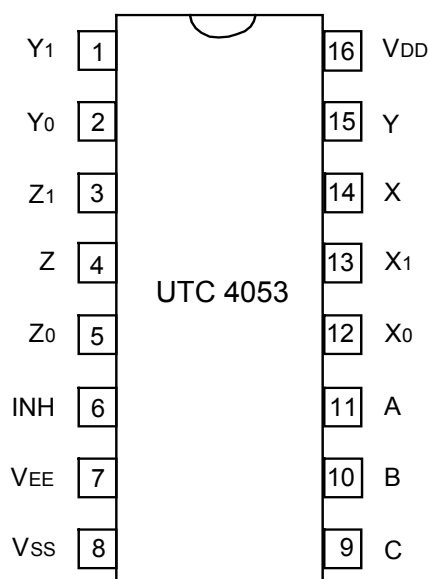
FEATURES

- * Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 ~ 18 V
Note: V_{EE} must be $\leq V_{SS}$
- * Linearized Transfer Characteristics
- * Pin-to-Pin Replacement for CD4053

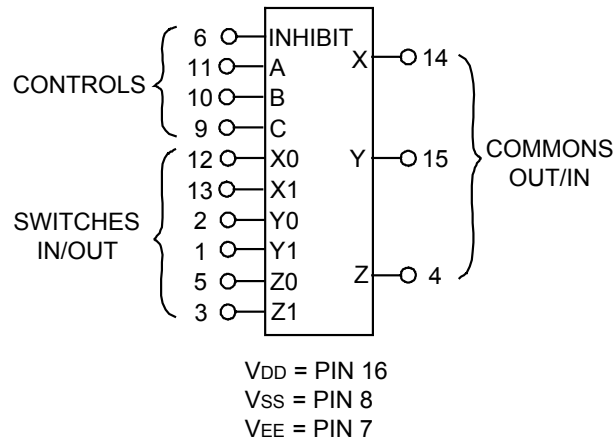


*Pb-free plating product number: 4053L

PIN CONFIGURATIONS



UTC 4053 Triple 2-Channel Analog Multiplexer/Demultiplexer



Note: Control Inputs referenced to V_{SS} , Analog Inputs and Outputs reference to V_{EE} . V_{EE} must be $\leq V_{SS}$.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE} , $V_{SS} \geq V_{EE}$)	V_{DD}	-0.5 ~ +18.0	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{in} , V_{out}	-0.5 ~ $V_{DD} + 0.5$	V
Input Current (DC or Transient), per Control Pin	I_{in}	± 10	mA
Switch Through Current	I_{SW}	± 25	mA
Power Dissipation. Per Package**	P_D	500	mW
Storage Temperature	T_{stg}	-65 ~ +150	$^{\circ}\text{C}$
Lead Temperature (8 - Second Soldering)	T_{Lead}	260	$^{\circ}\text{C}$

* Maximum Ratings are those values beyond which damage to the device may occur.

** Temperature Derating: "DIP and SOP" Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ ~ 125 $^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

($T_a = 25^{\circ}\text{C}$, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})						
Power Supply Voltage Range	V_{DD}	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0		18	V
Quiescent Current per Package	I_{DD}	Control Inputs: $V_{in} = V_{SS}$ or V_{DD} Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500\text{mV}^*$ $V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0.005 0.010 0.015	5.0 10 20	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	$T_a = 25^{\circ}\text{C}$ only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.) $V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		(0.07 $\mu\text{A}/\text{kHz}$) $f + I_{DD}$ Typical (0.20 $\mu\text{A}/\text{kHz}$) $f + I_{DD}$ (0.36 $\mu\text{A}/\text{kHz}$) $f + I_{DD}$		μA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})						
Low – Level Input Voltage	V _{IL}	Ron= per spec, Ioff = per spec V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		2.25 4.50 6.75	1.5 3.0 4.0	V
High – Level Input Voltage	V _{IH}	Ron= per spec, Ioff = per spec V _{DD} =5.0V V _{DD} =10V V _{DD} =15V	3.5 7.0 11	2.75 5.50 8.25		V
Input Leakage Current	I _{in}	V _{in} = 0 or V _{DD} , V _{DD} =15V		±0.00001	±0.1	μA
Input Capacitance	C _{in}			5.0	7.5	pF
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})						
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{IO}	Channel On or Off	0		V _{DD}	V _{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV _{switch}	Channel On	0		600	mV
Output Offset Voltage	V _{OO}	V _{in} = 0V, No Load		10		μV
ON Resistance	Ron	ΔV _{switch} ≤ 500mV* V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch) V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		250 120 80	1050 500 280	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	ΔRon	V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		25 10 10	70 50 45	Ω
Off-Channel Leakage Current (Figure 8)	Ioff	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel, V _{DD} =15V		±0.05	±100	nA
Capacitance, Switch I/O	C _{I/O}	Inhibit = V _{DD}		10		pF
Capacitance, Common O/I	C _{O/I}	Inhibit = V _{DD}		17		pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	Pins Not Adjacent Pins Adjacent		0.15 0.47		pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

* For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See second page of this data sheet.)

ELECTRICAL CHARACTERISTICS*(C_L = 50pF, T_a=25°C, V_{EE} ≤ V_{SS}, unless otherwise indicated.)

PARAMETER	SYMBOL	V _{DD} - V _{EE} Vdc	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
Propagation Delay Times (Figure 4) Switch Input to Switch Output (R _L = 10 kΩ)	t _{PLH} , t _{PHL}	5.0 10 15	t _{PLH} , t _{PHL} = (0.17 ns/pF) C _L + 16.5 ns t _{PLH} , t _{PHL} = (0.08 ns/pF) C _L + 4.0 ns t _{PLH} , t _{PHL} = (0.06 ns/pF) C _L + 3.0 ns		25 8.0 6.0	65 20 15	ns
Inhibit to Output	t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5.0 10 15	(R _L =10kΩ, V _{EE} =V _{SS})Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level		275 140 110	550 280 220	ns
Control Input to Output	t _{PLH} , t _{PHL}	5.0 10 15	R _L = 10 kΩ, V _{EE} = V _{SS}		300 120 80	600 240 160	ns
Second Harmonic Distortion		10	R _L = 10KΩ, f = 1 kHz, Vin = 5 V _{PP}		0.07		%
Bandwidth (Figure 5)	BW	10	R _L = 1kΩ, Vin = 1/2 (V _{DD} -V _{EE}) p-p, C _L = 50pF, 20 Log (Vout/Vin) = -3dB		17		MHz
Off Channel Feedthrough Attenuation (Figure 5)		10	R _L = 1KΩ, Vin = 1/2 (V _{DD} - V _{EE}) p-p fin = 55 MHz		-50		dB
Channel Separation (Figure 6)		10	R _L = 1 kΩ, Vin = 1/2 (V _{DD} -V _{EE}) p-p fin = 3.0 MHz		-50		dB
Crosstalk, Control Input to Common O/I (Figure 7)		10	R ₁ = 1 kΩ, R _L = 10 kΩ Control t _{TLH} = t _{THL} = 20 ns, Inhibit = V _{SS})		75		mV

* The formulas given are for the typical characteristics only at 25°C.

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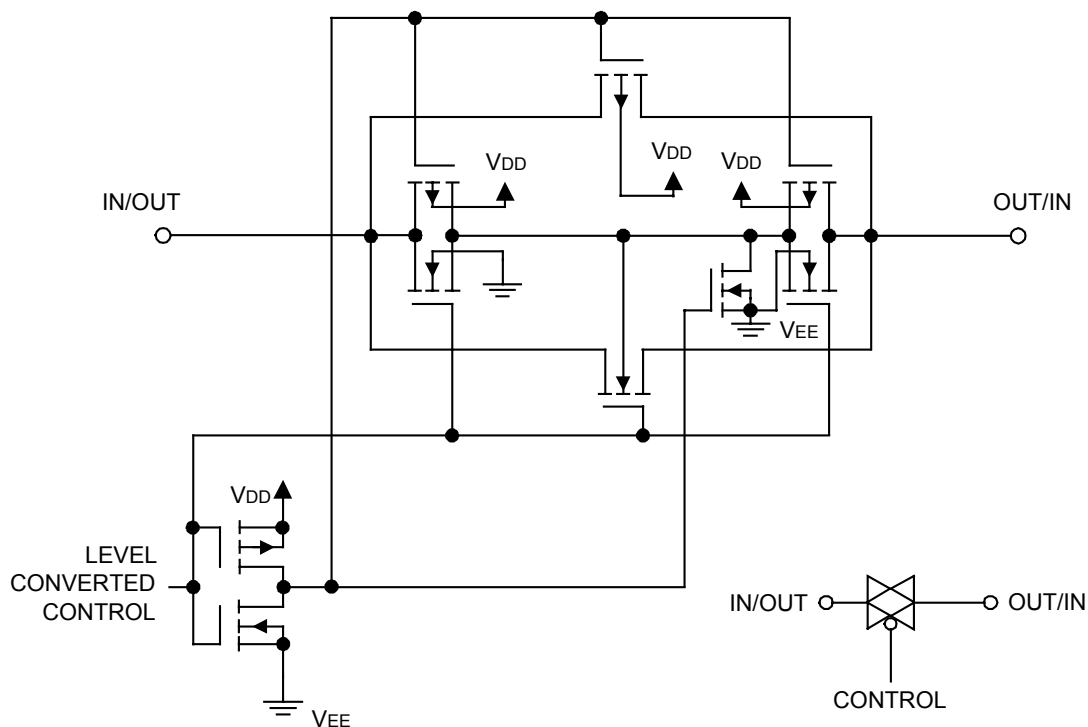


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches		
Inhibit	Select					
	C	B	A	UTC 4053		
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	None		

x = Don't Care

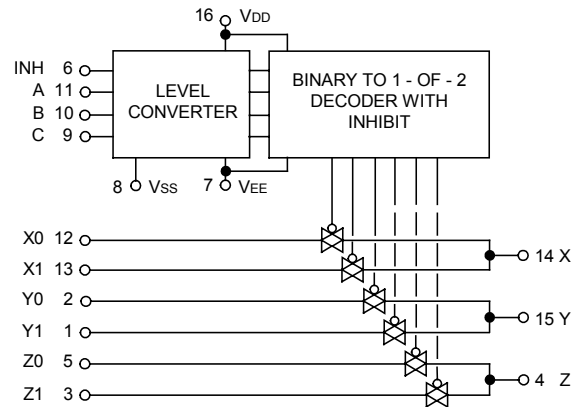
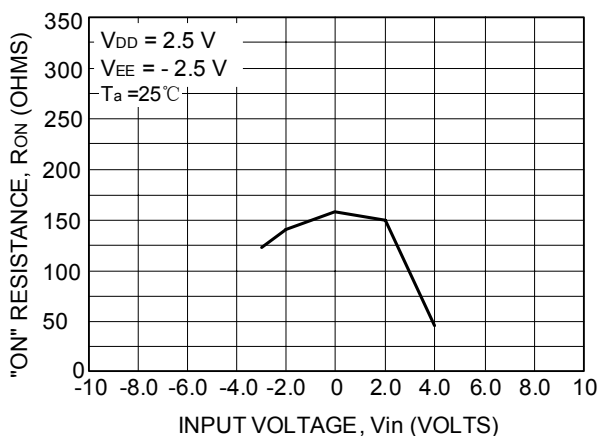
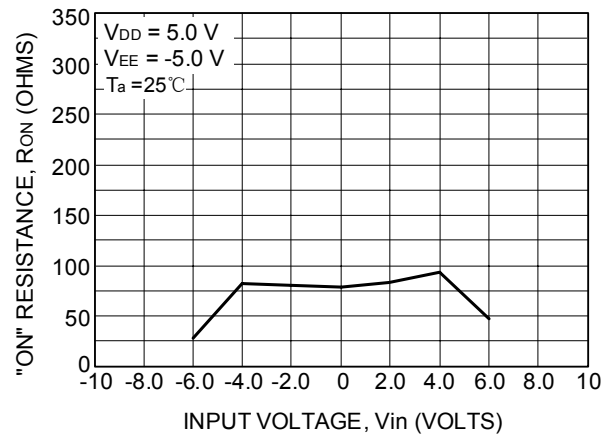
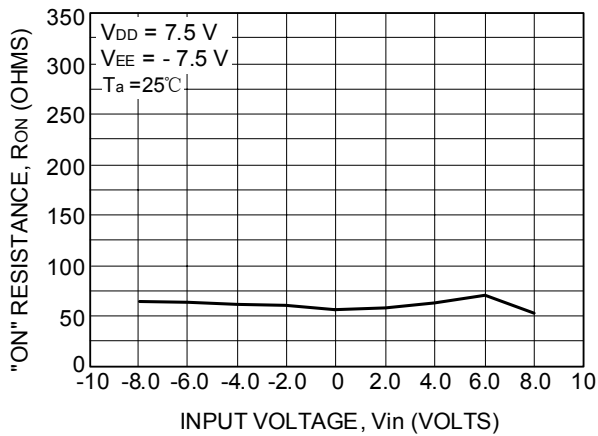


Figure 2. UTC 4053 Functional Diagram



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